SH67P51

OTP 4-bit Microcontroller with LCD driver & Remote control carrier synthesizer

Preliminary

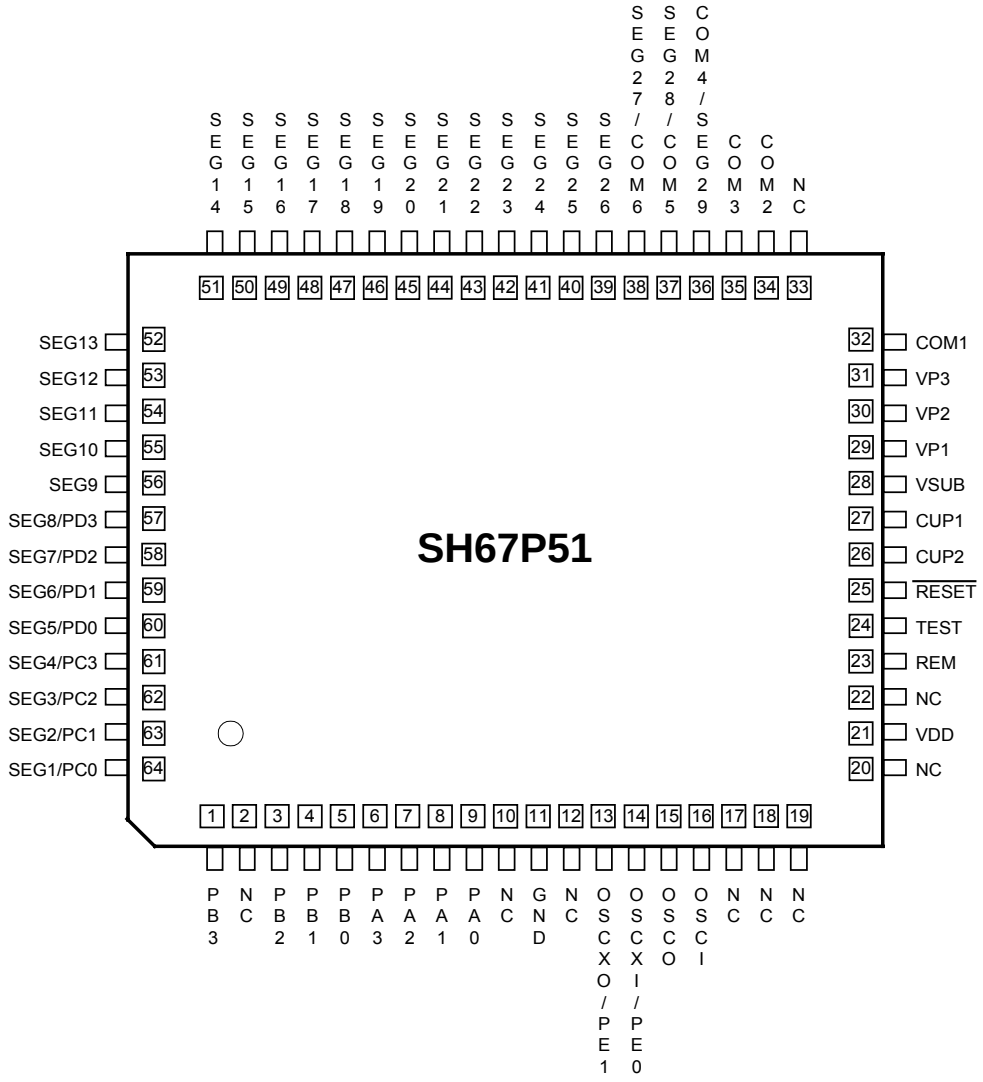
Features

- SH6610C-based single-chip 4-bit micro-controller
- ROM: 2048 X 16 bits OTP ROM
- RAM: 128 X 4 bits Data RAM
- Operation voltage: 1.8V – 3.6V (Typically 3.0V)
- 18 CMOS bi-directional I/O pins
  - PortA,PortB
  - PortC: shared with LCD SEG1-4
  - PortD: shared with LCD SEG5-8
  - PortE: shared with OSCXI, OSCXO
- 4-level subroutine nesting (including interrupts)
- One 8-bit auto re-load timer/counter
- One 8-bit base timer
- Warm-up timer for power-on reset
- Powerful interrupt sources:
  - Internal interrupt (Timer0).
  - Internal interrupt (Base Timer)
  - External interrupts: PortB & PortC (falling edge).
- Built-in remote control programmable carrier synthesizer
- Build in LCD voltage regulator
- Pull-up resistor for reset pin (OTP option)
- LCD driver:
  - 3X29 dots (1/3 duty 1/3 bias)
  - 4X28 dots (1/4 duty 1/3 bias)
  - 5X27 dots (1/5 duty 1/3 bias)
  - 6X26 dots (1/6 duty 1/3 bias)
- Dual Clock Source
  - OSC(OTP option):
  - Crystal oscillator: 32.768 kHz
  - RC oscillator: 131 kHz
  - OSCX:
  - Ceramic/Crystal oscillator: 400k~4MHz
  - Build in RC: (4MHz±2%)
- Instruction cycle time:
  - 4/4MHz (= 1μs) for 4MHz OSCX clock
  - 4/455kHz(=8.79μs) for 455kHz
  - 4/32.768kHz(=122.07μs) for 32.768kHz OSC clock
  - 4/131kHz(=30.52μs) for 131kHz OSC clock
- Two low power operation modes: HALT and STOP
- Built-in watchdog timer
- Built-in Low Voltage Reset Circuit (1.7±0.1V)
- Low Power Detect (2.3±0.1V)

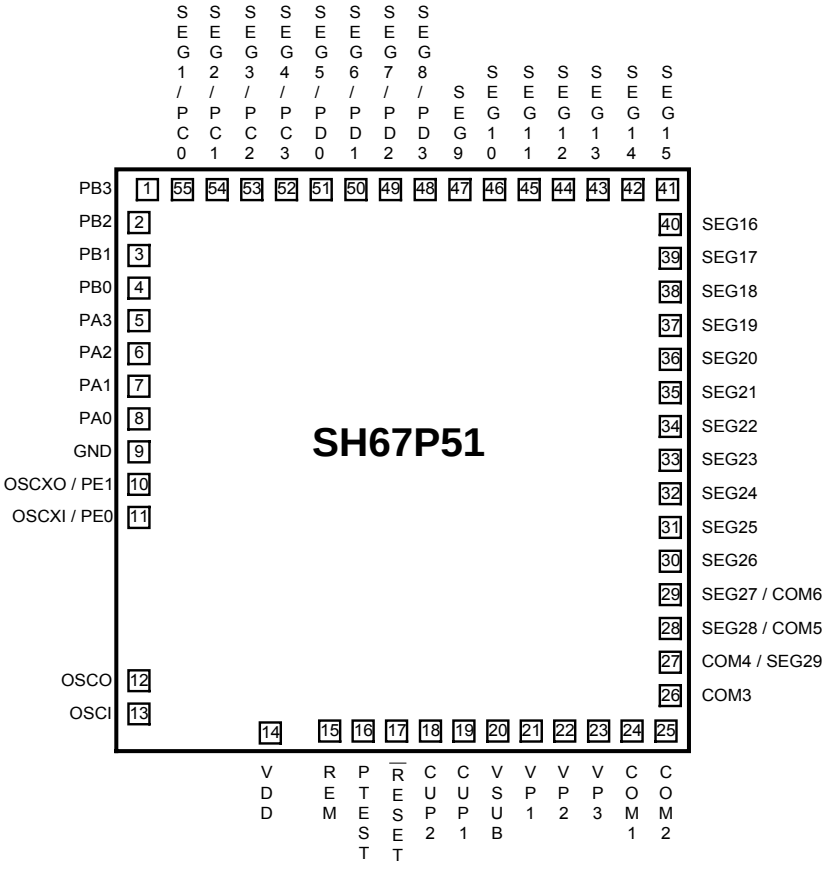
General Description

SH67P51is dedicated to infrared remote control transmitter with LCD applications. This chip integrates the SH6610C 4-bit CPU core with SRAM, OTP ROM, one 8-bit timer, one base timer, LCD driver, programmable input/output driving buffers, carrier synthesizer, and voltage regulator. This chip builds in a dual-oscillator to enhance the total chip performance.

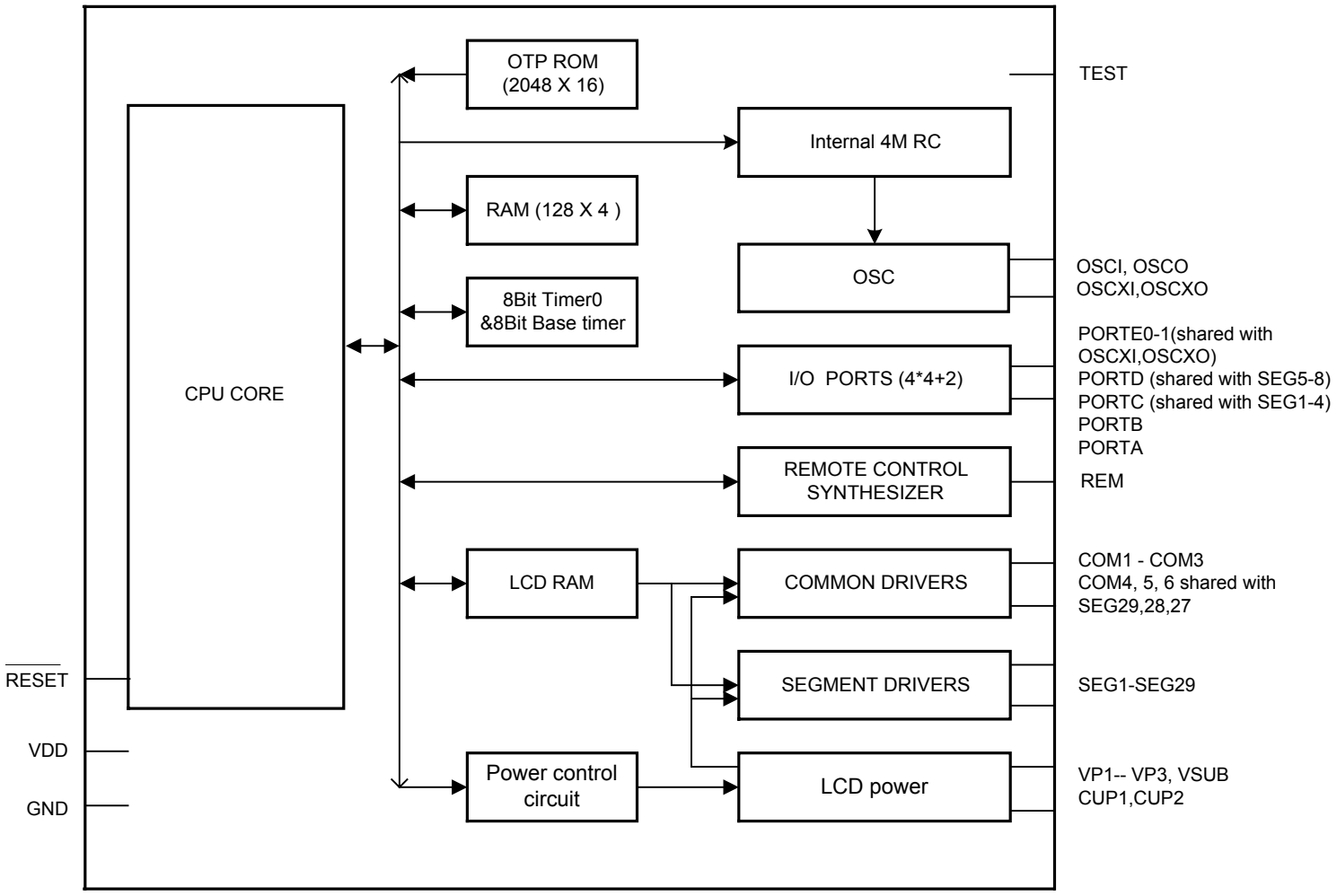
Pin Configuration



Pad Configuration



Block Diagram



Pin Descriptions

Pin No.	Designation	I/O	Descriptions
29 - 31	VP1-VP3	P	Power supply pin for LCD,
27 - 26	CUP1-2	P	Connection for LCD bias capacitor
28	VSUB	P	Power supply pin, connected to external capacitor
25	$\overline{\text{RESET}}$	I	Reset input (Optional internal pull-up)
24	TEST	I	Test pin (Internal pull-low).
23	REM	O	Carrier synthesizer for infrared or RF output pin.
21	V_{DD}	P	Power supply.
16	OSCI	I	Oscillator input pin.
15	OSCO	O	Oscillator output pin
14	OSCXI / PE0	I/O	Oscillator X input pin connected to ceramic oscillator. Shared with bit programmable I/O pin.
13	OSCXO / PE1	I/O	Oscillator X output pin connected to ceramic oscillator. Shared with bit programmable I/O pin.
11	GND	P	Ground pin.
9 - 6	PA0 – PA3	I/O	Bit programmable I/O.
5,4,3,1	PB0 – PB3	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge).
64 - 61	SEG1 – SEG4 / PC0 – PC3	I/O	LCD segment 1-4. Shared with bit programmable I/O pins, Vector Interrupt (Active falling edge),
60 - 57	SEG5 – SEG8 / PD0 – PD3	I/O	LCD segment 5-8. Shared with bit programmable I/O pins, Vector Interrupt (Active falling edge),
56 - 39	SEG9 – SEG26	O	LCD driver Segment 9 – 26
38 – 37	SEG27-SEG28 / COM6–COM5	O	LCD driver Segment 27, 28. Shared with LCD driver Common 6, 5.
32,34,35	COM1-COM3	O	LCD driver Common 1- 3
36	COM4 / SEG29	O	LCD driver Common 4 . Shared with LCD driver Segment 29.

OTP Programming Pin Description (OTP program mode)

Pin No.	Symbol	I/O	Shared by	Description
21	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
24	VPP	P	TEST	Programming high voltage Power supply (+10.5V)
11	GND	P	GND	Ground
16	SCK	I	OSCI	Programming Clock input pin
9	SDA	I/O	PA[0]	Programming Data pin

Pad Descriptions (Total 55 pad)

Pad No.	Designation	I/O	Descriptions
21 - 23	VP1-VP3	P	Power supply pin for LCD,
19 - 18	CUP1-2	P	Connection for LCD bias capacitor
20	VSUB	P	Power supply pin, connected to external capacitor
17	$\overline{\text{RESET}}$	I	Reset input (Optional internal pull-up)
16	TEST	I	Test pin (Internal pull-low).
15	REM	O	Carrier synthesizer for infrared or RF output pin.
14	V_{DD}	P	Power supply.
13	OSCI	I	Oscillator input pin.
12	OSCO	O	Oscillator output pin
11	OSCXI / PE0	I/O	Oscillator X input pin connected to ceramic oscillator. Shared with bit programmable I/O pin.
10	OSCXO / PE1	I/O	Oscillator X output pin connected to ceramic oscillator. Shared with bit programmable I/O pin.
9	GND	P	Ground pin.
8 - 5	PA0 – PA3	I/O	Bit programmable I/O .
4 - 1	PB0 – PB3	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge).
55 – 52	SEG1 – SEG4 / PC0 – PC3	I/O	LCD segment 1-4. Shared with bit programmable I/O pins, Vector Interrupt (Active falling edge),
51 – 48	SEG5 – SEG8 / PD0 – PD3	I/O	LCD segment 5-8. Shared with bit programmable I/O pins, Vector Interrupt (Active falling edge),
47 – 30	SEG9 – SEG26	O	LCD driver Segment 9 – 26
29 – 28	SEG27-SEG28 / COM6–COM5	O	LCD driver Segment 27 ,28. Shared with LCD driver Common 6 ,5.
24 – 26	COM1-COM3	O	LCD driver Common 1- 3
27	COM4 / SEG29	O	LCD driver Common 4 . Shared with LCD driver Segment 29.

OTP Programming Pad Description (OTP program mode)

Pad No.	Symbol	I/O	Shared by	Description
14	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
16	VPP	P	TEST	Programming high voltage Power supply (+10.5V)
9	GND	P	GND	Ground
13	SCK	I	OSCI	Programming Clock input pin
8	SDA	I/O	PA [0]	Programming Data pin

Functional Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 1K program ROM. It consists of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1 and PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:
(1) When executing a jump instruction (such as JMP, BA0, BC);
(2) When executing a subroutine call instruction (CALL) ;
(3) When an interrupt occurs;
(4) When the chip is at the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

1.2. ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjustment for addition/subtraction (DAA, DAS) Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)

Decision (BA0, BA1, BA2, BA3, BAZ, BC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow, which the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and restored back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Stack

A group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. It is organized 13 bits × 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of stack will be shifted out.

2. ROM

The SH67P51can address 2048 X 16 bit of program area from $000 to $7FF.

Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000H	JMP	Jump to RESET
$001H	NOP	Reserved
$002H	JMP	Jump to TIMER0 ISR
$003H	JMP	Jump to Base Timer ISR
$004H	JMP	Jump to PBC ISR

3. RAM

Built-in RAM consists of general purpose data memory and system registers.

Direct addressing in one instruction can access data memory and the system register.

The following is the memory allocation map:

$000 - $027: System register and I/O; $028 - $0A7: Data memory (128 × 4 bits). $300~$33A: LCD RAM;

Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Description
$00	-	IET0	IEBT	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register
$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base Timer Mode register
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit
$06				LPD	R	Bit0: 2.3v LPD flag
$07		LCDON			R/W	Bit2: Set to turn on LCD
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C			PE.1	PE.0	R/W	PORTE
$0D				REMO REM	W R	Bit0: REMO output data. Bit0: REM pin output status.
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	PULLEN	CPS2	CPS1	CPS0	R/W	Bit2-0: Carrier counter source pre-divider Bit3: Port pull high enable control
$14	OXS		OXM	OXON	R/W	Bit0: Turn on OSCX oscillator Bit1: CPU clocks select (1: OSCX/0: OSC) Bit3: OSCX type selection
$15	O/S1	O/S0	DUTY1	DUTY0	R/W	Bit0,1: Select LCD DUTY(1/3 or 1/4 or 1/5 or 1/6) Bit2: Set PortC as LCD Segment1 – 4 Bit3: Set PortD as LCD Segment5 – 8
$16	PAIN	PBIN	PCIN	PDIN	R/W	Control PORTA~PORTD input and output access enable or disable. Used in key matrix's application.
$17				PEIN	R/W	Control PORTE input and output access enable or disable. Used in key matrix's application.
$18	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	Set PORTA to be output port

The configuration of system register (continue)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Description
$19	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	Set PORTB to be output port
$1A	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	Set PORTC to be output port
$1B	PD3OUT	PD2OUT	PD1OUT	PD0OUT	R/W	Set PORTD to be output port
$1C	-	-	PE1OUT	PE0OUT	R/W	Set PORTE to be output port
$1D						Reserved
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit0 – 2: Watch dog timer control WDF: Watchdog timer overflow flag.
$1F						Reserved
$20	CFL3	CFL2	CFL1	CFL0	R/W	Carrier low level timer load data register
$21	CFL7	CFL6	CFL5	CFL4	R/W	Carrier low level timer load data register
$22	CFH3	CFH2	CFH1	CFH0	R/W	Carrier high level timer load data register
$23	CFH7	CFH6	CFH5	CFH4	R/W	Carrier high level timer load data register
$24~27						Reserved

(b). system register initial state

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset / Low Voltage Reset	WDT Reset
$00	-	IET0	IEBT	IEP	-000	-000
$01	-	IRQT0	IRQBT	IRQP	-000	-000
$02	-	TM0.2	TM0.1	TM0.0	-000	-uuu
$03	BTM.3	BTM.2	BTM.1	BTM.0	0000	uuuu
$04	TL0.3	TL0.2	TL0.1	TL0.0	xxxx	xxxx
$05	TH0.3	TH0.2	TH0.1	TH0.0	xxxx	xxxx
$06				LPD	---0	---0
$07		LCDON			-0--	-u--
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C			PE.1	PE.0	--00	--00

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset / Low Voltage Reset	WDT Reset
$0D				REM	---0	---0
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	PULLEN	CPS2	CPS1	CPS0	0000	0uuu
$14	OXS		OXM	OXON	0-00	u-0u
$15	O/S1	O/S0	DUTY1	DUTY0	1100	uuuu
$16	PAIN	PBIN	PCIN	PDIN	0000	uuuu
$17				PEIN	---0	---u
$18	PA3OUT	PA2OUT	PA1OUT	PA0OUT	0000	0000
$19	PB3OUT	PB2OUT	PB1OUT	PB0OUT	0000	0000
$1A	PC3OUT	PC2OUT	PC1OUT	PC0OUT	0000	0000
$1B	PD3OUT	PD2OUT	PD1OUT	PD0OUT	0000	0000
$1C	-	-	PE1OUT	PE0OUT	--00	--00
$1D					-	-
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	1000
$1F					-	-
$20	CFL3	CFL2	CFL1	CFL0	0000	uuuu
$21	CFL7	CFL6	CFL5	CFL4	0000	uuuu
$22	CFH3	CFH2	CFH1	CFH0	0000	uuuu
$23	CFH7	CFH6	CFH5	CFH4	0000	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented.

4. Oscillator circuit

4.1. Circuit Configuration

SH67P51 has two on-chip oscillation circuits OSC and OSCX.

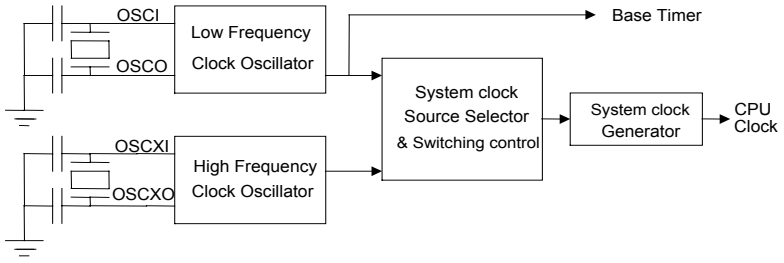
OSC is a low frequency oscillator (32.768kHz crystal or 131kHz RC, selected by OTP option). This is designed for low frequency operation. OSCX is a high frequency oscillator (internal RC oscillator (4MHz ± 2%) or external ceramic/crystal oscillator, selected by Register OXS). It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock.

When $\overline{\text{RESET}}$ pad is pulled low or $V_{DD} \leqq V_{LVR}$, the OSC and OSCX will stop oscillation. And after the $\overline{\text{RESET}}$ pad returns to high and $V_{DD} > V_{LVR}$, OSC will starts oscillation and OSCX will be turned off. The OSC clock is automatically selected as the system clock input source.

After WDT reset initialization, the OSC starts oscillation and OSCX remains the original state. The OSC clock is automatically selected as the system clock input source.

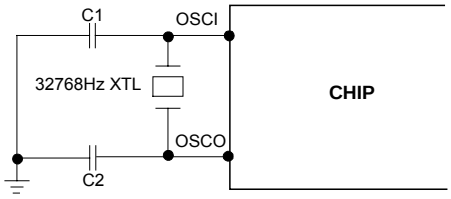
Oscillator Block Diagram



4.2. OSC oscillation

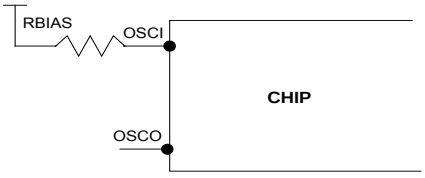
The OSC generates the basic clock pulses that provide the CPU and peripherals (Base timer, LCD) with an operating clock.

OSC Crystal oscillator type



C1, C2: 12pF for reference. (Please refer to the oscillator spec)

OSC RC oscillator type

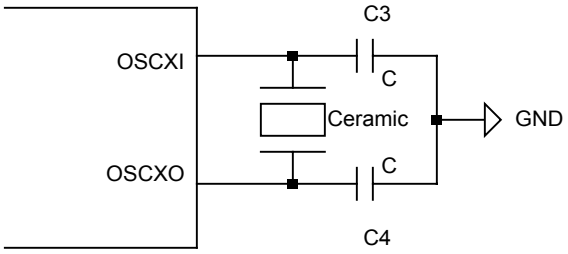


RBIAS: 1.5MΩ for reference

4.3. OSCX oscillation

The OSCX is an internal 4MHz RC or external ceramic/crystal oscillator. The software options select the ceramic or internal RC as the CPU's clock.

(1) Ceramic/Crystal resonator: 400kHz – 4MHz.



C3, C4: 20~200pF. (Please refer to the oscillator spec)

(2) Internal oscillator: 4MHz.

When the internal 4MHz RC is selected, the OSCXI pin and OSCXO pin is also set as PortE0,1.

4.4. Control of oscillator

The oscillator control register configuration is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0
$14	OXS	-	OXM	OXON

OXON: OSCX oscillation on/off.
0: Turn-off OSCX oscillation 1: Turn-on OSCX oscillation

OXM: switching system clock.
0: select OSC as system clock 1: select OSCX as system clock

OXS: OSCX oscillator type selection
0: OSCX set as ceramic oscillator 1: OSCX set as RC oscillator, and set OSCXI/OSCXO as PortE

4.5. Programming notes

It takes at least 5 ms for the OSCX oscillation circuit to turn on until the oscillation stabilizes. When switching the CPU system clock from OSC to OSCX, the user must wait a minimum of 5ms since the OSCX oscillation is running. However, the start time varies with respect to oscillator characteristics and the condition of use. Thus the wait time depends on the application. When switching from OSCX to OSC, the user should switch clock first then turn off OSCX. If switching from OSCX to OSC and turning off OSCX in one instruction, the OSCX turn off control will be delayed for one instruction cycle automatically to prevent CPU operation error. Following is the timing of system clock switching.

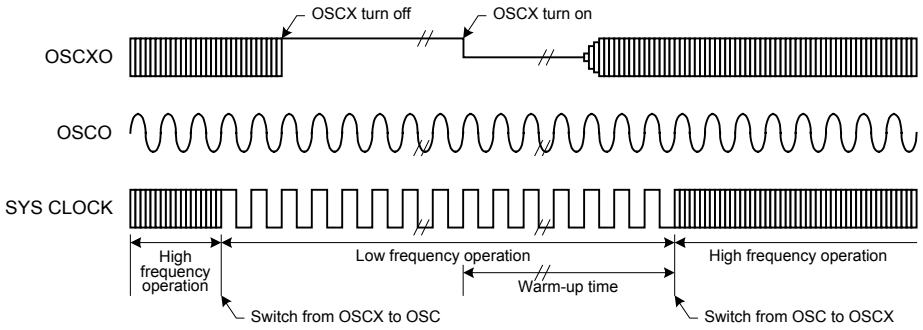


Figure 1. Timing of system Clock Switching

4.6. System clock

The system clock varies as the clock source changes. The following table shows the instruction execution time according to each frequency of the system clock source.

	32.768kHz Crystal (OSC)	131kHz RC (OSC)	455kHz Ceramic (OSCX)	4MHz RC (OSCX)
Cycle time	122.07 μs	30.52μs	8.79 μs	1μs

5. Timer 0

SH6636 has one 8-bit timer. The timer/counter has the following features:

. 8-bit up-counting timer/counter

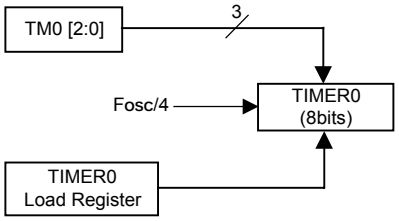
. Automatically re-loads counter

. 8-bit pre-scaler

. Interrupt on overflow from $FF to $00

The following is a simplified timer block diagram.

Timer block Diagram



(a) Configuration and Operation

Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

Load register programming: Write the low-order digit first and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FF to $00.

Timer Load Register: Since register H will control the physical READ and WRITE operations.

Follow these steps:

Write Operation:

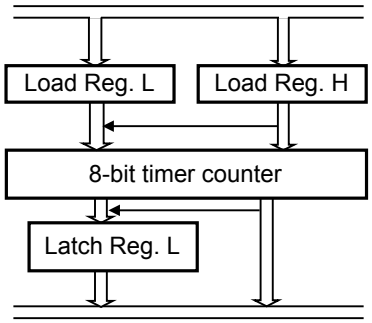
Low nibble first,

High nibble to update the counter

Read Operation:

High nibble first,

Followed by Low nibble.



Timer Load register Configure

(b) Timer mode register

The timer can be programmed in several different prescaler ratios by setting the Timer Mode register (TM0).

The 8-bit counter prescaler overflow output pulses. The timer mode registers (TM0) are 3-bit registers used for timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Register

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^{9}$	512
0	1	0	$/2^{7}$	128
0	1	1	$/2^{5}$	32
1	0	0	$/2^{3}$	8
1	0	1	$/2^{2}$	4
1	1	0	$/2^{1}$	2
1	1	1	$/2^{0}$	1

5.3. Warm-up counter

The device builds in oscillator warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:
(1) After Pad reset/ Power on reset / Low voltage reset
(2) Watch Dog reset
(3) Wake-up from stop mode
Warm-up time interval:
(1) If RC oscillator (OSC or OSCX) is selected as system clock, the warm-up counter pre-scaler is 2^7 (128).
Example: 131kHz RC is system clock, warm-up time interval is 2^7 x (1/131kHz)=977 μs.
Example: 4MHz RC is system clock, warm-up timer interval is 2^7 x (1/4MHz)=32μs
(2) If Crystal/Ceramic oscillator is selected as system clock, the warm-up counter pre-scaler is 2^{13} (8192).
Example: 32.768kHz crystal is system clock, warm-up time interval is 2^{13} x (1/32.768kHz)=250ms.
Example: 455kHz ceramic is system clock, warm-up time interval is 2^{13} x (1/455kHz)=18ms
So warm-up time wake from stop status is different for different system clock source.

6. Base Timer

The MCU has a base timer that is shared with the warm-up timer and the clock source is base timer pre-scaler output pulse (scaled from OSC clock, X'Tal 32.768kHz or RC 131kHz). After MCU is reset, it counts at every clock-input signal. When it counts to $FF, right after next clock input, counter counts to $00 and generates an overflow. This causes the interrupt flag of base timer to be set to 1. Therefore, the base timer can function as an interval timer periodically, generating overflow output as every 256th clock signal input.

The timer accepts 4096Hz or 16KHz clock, and base timer generates an accurate timing interrupt. This base time pre-scaler can be reset by the program for accurate timing.

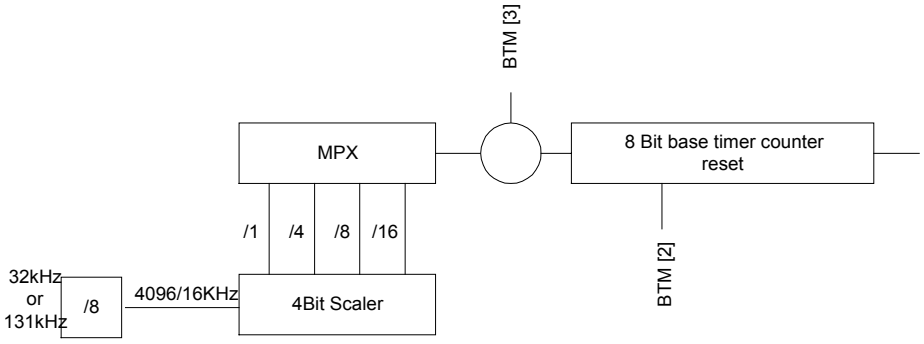
This clock-input source is selected by BTM register.

Address	Bit3	Bit2	Bit1	Bit0	Function
$03	BTM.3	BTM.2	BTM.1	BTM.0	Base timer mode register

BTM.3 = 0: Disable the base timer BTM.3 = 1: Enable the base timer

BTM.2 = 0: Non reset the base timer BTM.2 = 1: reset the base timer

BTM.1	BTM.0	Prescaler Ratio	Clock source
0	0	/1	Fosc/8
0	1	/4	Fosc/32
1	0	/8	Fosc/64
1	1	/16	Fosc/128



7. I/O PORT

The SH67P51 provides 18 I/O pins. Each I/O pin contains pull-high MOS controllable by the program. Sections below show the circuit configuration of I/O ports.

PORTA, PORTB, PORTC, PORTD, PORTE

Each of these ports contains 4 bits or 2bits I/O pins (PortC,D are shared with LCD SEG1~8, PortE are shared with OSCXI/OSCXO) . The port control register can control ON/OFF of the output buffer for port. Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C			PE.1	PE.0	R/W	PORTE

The following sections show the circuit configuration of the I/O ports.

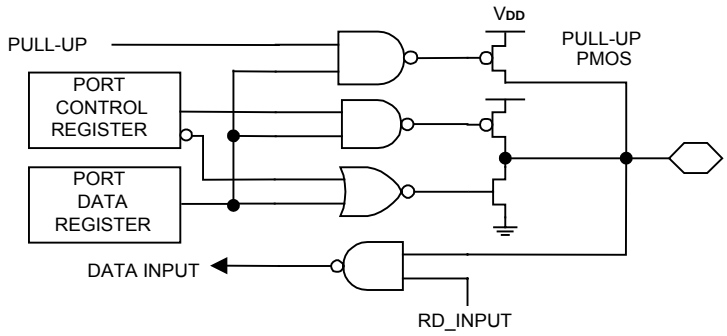


Figure. 2 Port Configuration Function Block Diagram

Port I/O Control Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$18	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	Set PORTA as output port
$19	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	Set PORTB as output port
$1A	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	Set PORTC as output port
$1B	PD3OUT	PD2OUT	PD1OUT	PD0OUT	R/W	Set PORTD as output port
$1C			PE1OUT	PE0OUT	R/W	Set PORTE as output port

I/O control register: PAXOUT, PBXOUT, PCXOUT, PDXOUT, PEXOUT (X = 0, 1, 2, 3)

1: Set I/O as an output buffer.

0: Set I/O as an input buffer (power-on initial).

I/O share control register

Add.	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$14	OXS		OXM	OXON	R/W	Bit0: Turn on OSCX oscillator Bit1: CPU clocks select (1: OSCX/0: OSC) Bit3: OSCX type selection
$15	O/S1	O/S0	DUTY1	DUTY0	R/W	Bit0, 1: Select LCD DUTY (1/3 or 1/4 or 1/5 or 1/6) Bit2: Set PortC as LCD Segment1 – 4 Bit3: Set PortD as LCD Segment5 – 8

OXS: 0: OSCX set as ceramic oscillator (Default)

1: OSCX set as RC oscillator, and set OSCXI/OSCXO as PortE

O/S0: 0: select PortC as I/O ports

1: select PortC as LCD Segment 1-4 (Default)

O/S1: 0: select PortD as I/O ports

1: select PortD as LCD Segment 5-8 (Default)

The default value of O/S0, O/S1 is “1”, after Power on / Pad / LVR reset. It means that the PortC,D is shared to Segment 1-8 and output GND after Power on / Pad / LVR reset. So, the PortC,D shouldn’t be pulled high by external signal source to avoid the additional leakage current when reset.

Controlling the pull-high MOS

These ports contain pull-high MOS controlled by the program. PULLEN register controls On/Off of all pull-high MOS simultaneously. Pull-high MOS is controlled by the port data registers (PA, PB, PC, PD, PE) of each port also. Thus, the pull-high MOS can be turned on and off individually.

To turn on the pull up resister, user must set PULLEN to 1,and write 1 to the port data register.

Port Function Control is below:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PULLEN	CPS2	CPS1	CPS0	R/W	Bit2-0: Carrier counter source pre-divider Bit3: Port pull high enable control

PULLEN Port Pull-low MOS enables control

1 = Enable PORT pull-high MOS

0 = Disable PORT pull-high MOS (power-on initialization)

Ports as key matrix

SH67P51’s I/O can make up of key matrix and PortC~PortD can use as LCD segment output as same time. In this application, user should control that scanning key matrix share the timing of LCD display. Only when user scan key matrix, all of Ports are used as I/O; otherwise PortC,D use as LCD segment output to drive LCD panel. The Ports used as I/O or segment is controlled by software.

In scan key application, when user doesn’t execute operation of scan key, Ports which don’t share as LCD segment output should be set as I/O, disabled it’s pull high resistor and input/output access by write system register ($16H~$1CH)’s corresponding bit. Execute above operation can prevent LCD voltage input to the general I/O Ports and Port’s pull high or output affect the LCD segment’s waveform.

When user wants to scan key, all ports, which make up of the key matrix should be used as general I/O, the ports’ pull high resistor and input access should be enabled by clear the system register ($16H, $17H)’s corresponding bit.

Key matrix's IO ports control register

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$16	PAIN	PBIN	PCIN	PDIN	R/W	Control PORTA~PORTD input and output access enable or disable. Used in key matrix's application.
$17				PEIN	R/W	Control PORTE input and output access enable or disable. Used in key matrix's application.

PAIN…PFIN: In the key matrix's application, control PORTA~F input and output access.

0: Enable PA~PE pull high resistor and I/O access, Ports in normal state

1: Disable PA~PE pull high resistor and it's I/O access

Port Interrupt

The PORTB and PORTC are used as port interrupt sources. Since PORT I/O is bit programmable I/O, so only the input port can generate an external interrupt. Any one of the PORTB and PORTC input pin transitions from V_{DD} to GND will generate an interrupt request . Further falling edge transition would not be able to make an interrupt request until all of the input pins have returned to V_{DD}. The following is the port interrupt function block-diagram.

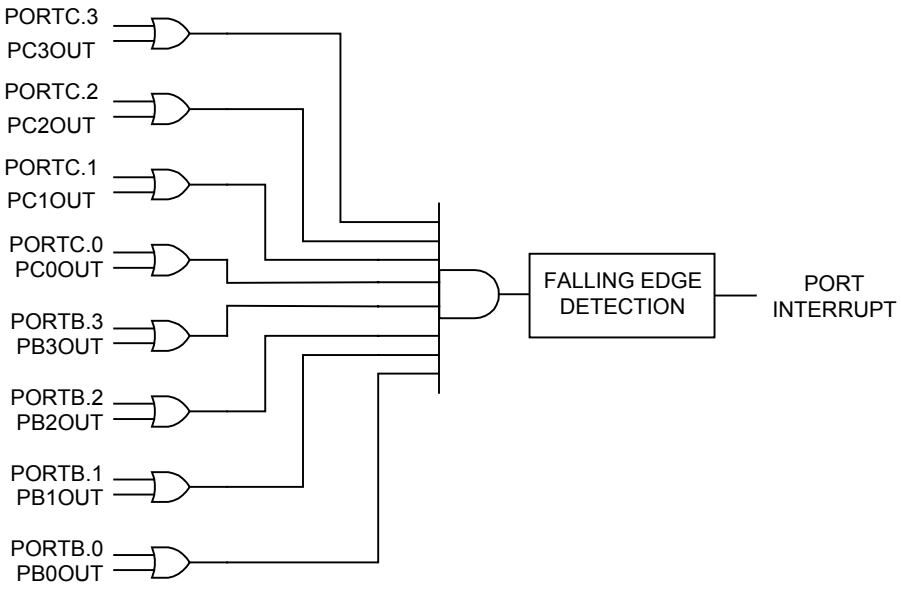


Figure. 3 PORT Interrupt Block Diagram

8.Remote Control Carrier Synthesizer

SH67P51 builds-in a carrier synthesizer for infrared or RF remote control circuits.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$13	PULLEN	CPS2	CPS1	CPS0	R/W	Bit2-0: Carrier counter source pre-divider Bit3: Port pull high enable control
$0D				REMO REM	W R	Bit0: REMO output data. Bit0: REM pin output status.

REMO: Remote output data control. The REM pin output status can be read by instruction.

CPS2~0: Carrier counter source pre-divider control Register
The carrier synthesizer can be programmed in several different pre-scaler ratios by setting CPS2~0.

Carrier count source pre-divider control Register

CPS2	CPS1	CPS0	Pre-scaler Divide Ratio	Ratio N
0	0	0	System clock /2^{11}	2048
0	0	1	System clock /2^{9}	512
0	1	0	System clock /2^{7}	128
0	1	1	System clock /2^{5}	32
1	0	0	System clock /2^{3}	8
1	0	1	System clock /2^{2}	4
1	1	0	System clock /2^{1}	2
1	1	1	System clock /2^{0}	1

The carrier generating counter is a 8 bit count-up counter and it has two reload data register. The counter and load registers both have low order digits and high order digits. Writing data into the timer load registers ($20,$21,$22,$23) can initialize the counter.

After system reset, the counter is automatically loaded with the contents of high level timer load data register ($22,$23)and output high level at the same time. Following when counter counts overflow from $FF to $00,the counter is automatically loaded with the contents of low level timer load data register ($20,$21) and output low level at the same time. When counter counts overflow again from $FF to $00 again, the counter will be loaded with the contents of high level timer load data register again. The above sequences make up a complete loop. So the carrier synthesizer can output continuous carrier wave of certain duties and certain period.

If bit0 of $0D(REMO) is set to 1from 0,the carrier counter will be initialized to load high level timer load data register and output high level whatever states the counter is.

Load register programming: User can modify low level timer load data register ($20,$21) to change the width of the low level. User can also modify high level timer load data register ($22,$23)to change the width of high level. In the way the carrier synthesizer can output carrier wave of different duties and different period.

Carrier load data register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$20	CFL3	CFL2	CFL1	CFL0	R/W	Carrier low level timer load data register
$21	CFL7	CFL6	CFL5	CFL4	R/W	Carrier low level timer load data register
$22	CFH3	CFH2	CFH1	CFH0	R/W	Carrier high level timer load data register
$23	CFH7	CFH6	CFH5	CFH4	R/W	Carrier high level timer load data register

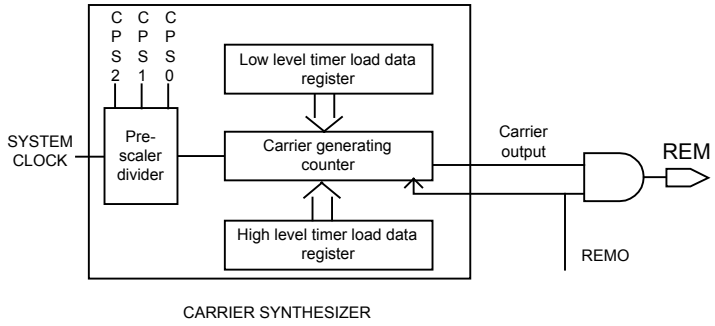


Figure. 4 Remote Control Functional Block Diagram

For example:

System clock	CPS2, CPS1, CPS0	CFL	CFH	Carrier Duty	Carrier Frequency
4M/4	1,1,1	$EF	$F8	8/25 ≈ 1/3	40.00kHz
4M/4	1,1,1	$EF	$F7	9/26 ≈ 1/3	38.46kHz
4M/4	1,1,1	$F2	$F3	13/27 ≈ 1/2	37.04kHz
4M/4	1,1,1	$EB	$F9	7/28 =1/4	35.71kHz
480k/4	1,1,1	$FE	$FF	1/3 = 1/3	40.00kHz
455k/4	1,1,1	$FE	$FF	1/3 = 1/3	37.92kHz
432k/4	1,1,1	$FE	$FF	1/3 = 1/3	36.00kHz

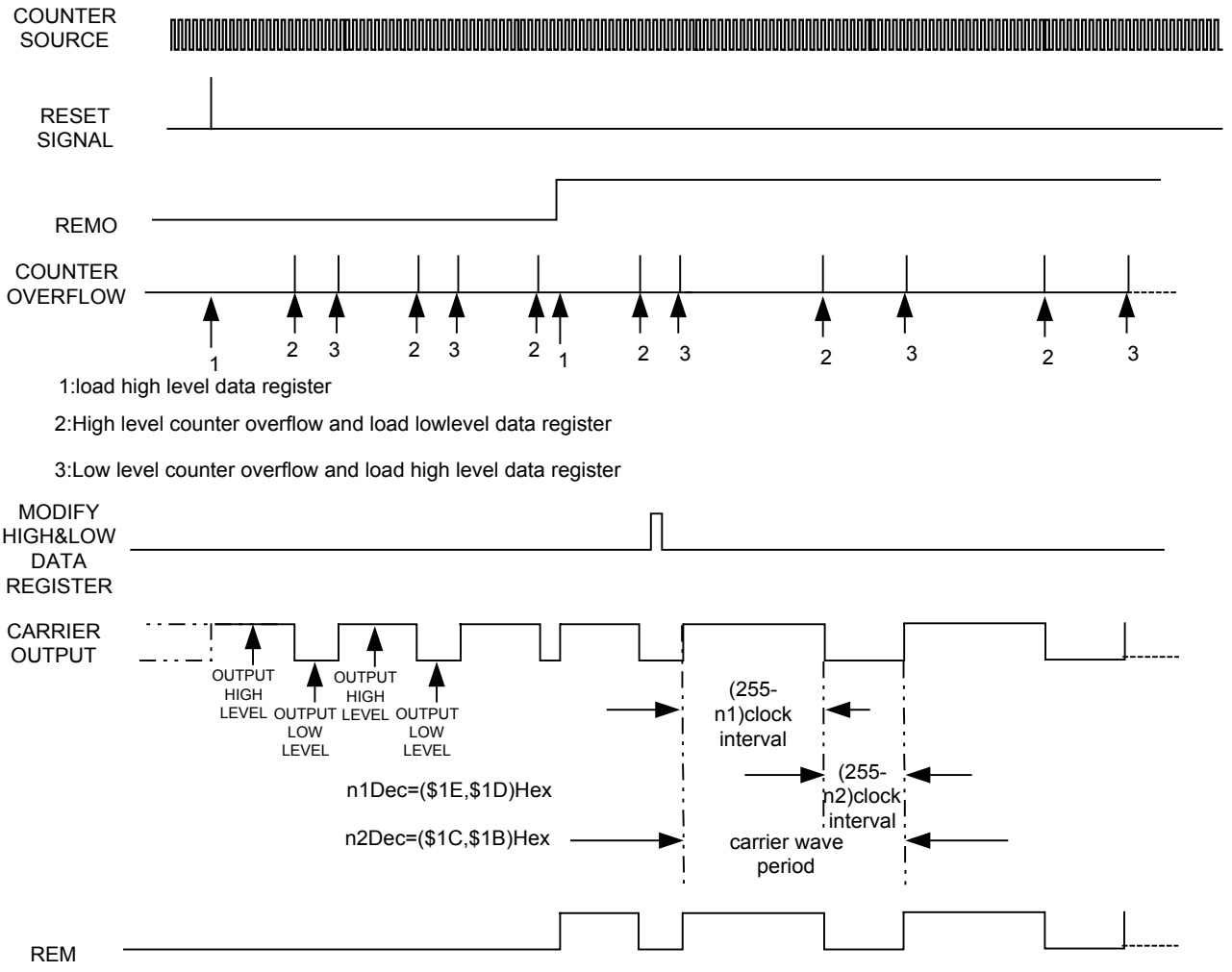


Figure.5 CARRIER SYNTHESIZE WAVE

9. LCD Driver

The LCD driver contains a controller, a voltage regulator generator, 3~6 common signal pins and 26~29 segment driver pins. There are seven different driving modes programmable: 1/3 duty and 1/3 bias, 1/4 duty and 1/3 bias , 1/5 duty and 1/3 bias and 1/6 duty and 1/3 bias. The driving mode is controlled by the system register $15 and the power-on initialization status is 1/4 duty, 1/3 bias.

When the “STOP” instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the same value before executing the “STOP” instruction.

When LCD off, both COMMON and SEGMENT output 0V.

9.1. LCD Control Register

Add.	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$07		LCDON			R/W	Bit2: Set to turn on LCD
$15	O/S1	O/S0	DUTY1	DUTY0	R/W	Bit0, 1: Select LCD DUTY (1/3 or 1/4 or 1/5 or 1/6) Bit2: Set PortC as LCD Segment1 – 4 Bit3: Set PortD as LCD Segment5 – 8

LCD Segment:

Register $15 bit2,3 can control the LCD segment number.

O/S0: 0: select PortC as I/O ports

1: select PortC as LCD Segment 1-4

O/S1: 0: select PortD as I/O ports

1: select PortD as LCD Segment 5-8

The default value of O/S0, O/S1 is “1”, after Power on / Pad / LVR reset. It means that the PortC,D is shared to Segment 1-8 and output GND after Power on / Pad / LVR reset. So, the PortC,D shouldn’t be pulled high by external signal source to avoid the additional leakage current when reset.

LCD Duty:

$15 bit1, 0(DUTY1, DUTY0) can control the LCD duty

DUTY1, 0: LCD duty control

00: 1/4 duty, 1/3 bias, LCD Segment29 shared to Common 4

01: 1/3 duty, 1/3 bias

10: 1/5 duty, 1/3 bias, LCD Segment28, 29 shared to Common 5,4

11: 1/6 duty, 1/3 bias, LCD Segment27, 28,29 shared to Common 6,5,4

LCD clock:

LCDCLK = OSC/32(32.768k crystal) or OSC/128(131k RC) = 1024 Hz

Frame frequency =	LCDCLK/(4X8) = 32Hz	1/4 duty
	LCDCLK/(4X6) = 42.7Hz	1/3 duty
	LCDCLK/(3X10) = 34.1Hz	1/5 duty
	LCDCLK/(2X12) = 42.7Hz	1/6 duty

LCD power

The program can turn off or turn on the LCD by writing 0 or 1 to $07 bit2.

LCDON: LCD on/off switch.
1: LCD on.
0: LCD off.

*When LCD is off, COM & SEG output GND in LCD application.

The SH67P51 build in a voltage regulator for LCD power. When the VDD is unstable or too low for LCD (VDD = 2.0~3.6), the internal voltage regulator can generate a stable voltage as LCD power.

*The following diagram is the application diagram for LCD power circuit

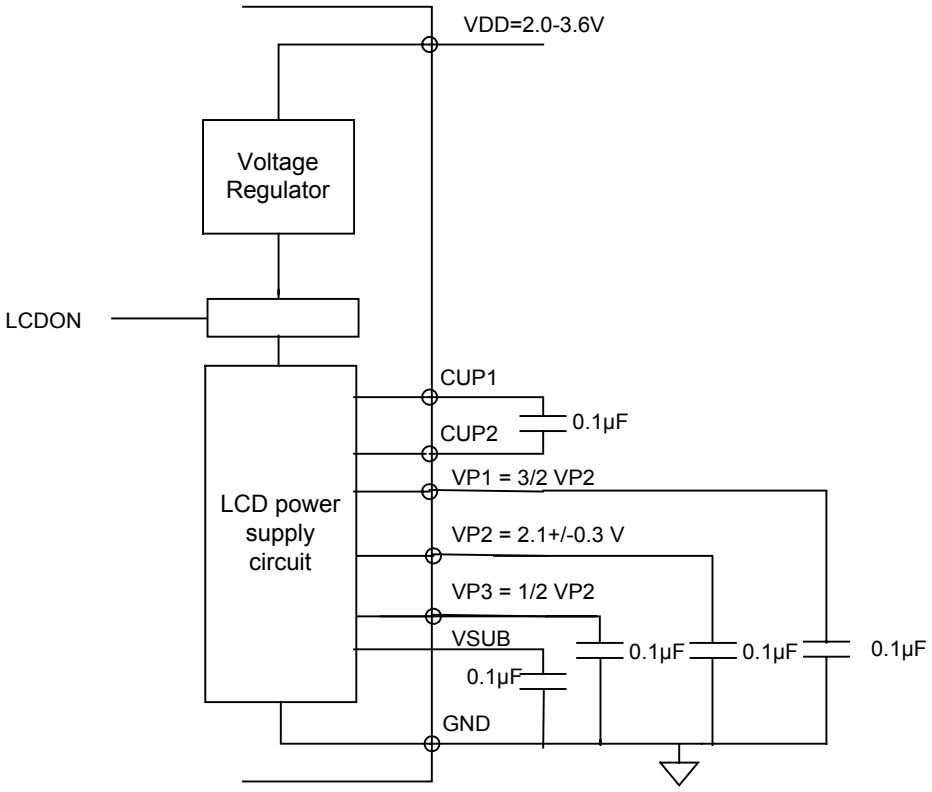


Figure.6 LCD power circuit diagram

9.2. Configuration of LCD RAM

LCD 1/4 duty 1/3 bias (4X28)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1	30EH	SEG15	SEG15	SEG15	SEG15
301H	SEG2	SEG2	SEG2	SEG2	30FH	SEG16	SEG16	SEG16	SEG16
302H	SEG3	SEG3	SEG3	SEG3	310H	SEG17	SEG17	SEG17	SEG17
303H	SEG4	SEG4	SEG4	SEG4	311H	SEG18	SEG18	SEG18	SEG18
304H	SEG5	SEG5	SEG5	SEG5	312H	SEG19	SEG19	SEG19	SEG19
305H	SEG6	SEG6	SEG6	SEG6	313H	SEG20	SEG20	SEG20	SEG20
306H	SEG7	SEG7	SEG7	SEG7	314H	SEG21	SEG21	SEG21	SEG21
307H	SEG8	SEG8	SEG8	SEG8	315H	SEG22	SEG22	SEG22	SEG22
308H	SEG9	SEG9	SEG9	SEG9	316H	SEG23	SEG23	SEG23	SEG23
309H	SEG10	SEG10	SEG10	SEG10	317H	SEG24	SEG24	SEG24	SEG24
30AH	SEG11	SEG11	SEG11	SEG11	318H	SEG25	SEG25	SEG25	SEG25
30BH	SEG12	SEG12	SEG12	SEG12	319H	SEG26	SEG26	SEG26	SEG26
30CH	SEG13	SEG13	SEG13	SEG13	31AH	SEG27	SEG27	SEG27	SEG27
30DH	SEG14	SEG14	SEG14	SEG14	31BH	SEG28	SEG28	SEG28	SEG28

LCD 1/3 duty 1/3 bias (3X29)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	-	COM3	COM2	COM1		-	COM3	COM2	COM1
300H	-	SEG1	SEG1	SEG1	30FH	-	SEG16	SEG16	SEG16
301H	-	SEG2	SEG2	SEG2	310H	-	SEG17	SEG17	SEG17
302H	-	SEG3	SEG3	SEG3	311H	-	SEG18	SEG18	SEG18
303H	-	SEG4	SEG4	SEG4	312H	-	SEG19	SEG19	SEG19
304H	-	SEG5	SEG5	SEG5	313H	-	SEG20	SEG20	SEG20
305H	-	SEG6	SEG6	SEG6	314H	-	SEG21	SEG21	SEG21
306H	-	SEG7	SEG7	SEG7	315H	-	SEG22	SEG22	SEG22
307H	-	SEG8	SEG8	SEG8	316H	-	SEG23	SEG23	SEG23
308H	-	SEG9	SEG9	SEG9	317H	-	SEG24	SEG24	SEG24
309H	-	SEG10	SEG10	SEG10	318H	-	SEG25	SEG25	SEG25
30AH	-	SEG11	SEG11	SEG11	319H	-	SEG26	SEG26	SEG26
30BH	-	SEG12	SEG12	SEG12	31AH	-	SEG27	SEG27	SEG27
30CH	-	SEG13	SEG13	SEG13	31BH	-	SEG28	SEG28	SEG28
30DH	-	SEG14	SEG14	SEG14	31CH	-	SEG29	SEG29	SEG29
30EH	-	SEG15	SEG15	SEG15					

LCD 1/5 duty 1/3 bias (5X27)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	-	COM5
300H	SEG1	SEG1	SEG1	SEG1	320H	-	-	-	SEG1
301H	SEG2	SEG2	SEG2	SEG2	321H	-	-	-	SEG2
302H	SEG3	SEG3	SEG3	SEG3	322H	-	-	-	SEG3
303H	SEG4	SEG4	SEG4	SEG4	323H	-	-	-	SEG4
304H	SEG5	SEG5	SEG5	SEG5	324H	-	-	-	SEG5
305H	SEG6	SEG6	SEG6	SEG6	325H	-	-	-	SEG6
306H	SEG7	SEG7	SEG7	SEG7	326H	-	-	-	SEG7
307H	SEG8	SEG8	SEG8	SEG8	327H	-	-	-	SEG8
308H	SEG9	SEG9	SEG9	SEG9	328H	-	-	-	SEG9
309H	SEG10	SEG10	SEG10	SEG10	329H	-	-	-	SEG10
30AH	SEG11	SEG11	SEG11	SEG11	32AH	-	-	-	SEG11
30BH	SEG12	SEG12	SEG12	SEG12	32BH	-	-	-	SEG12
30CH	SEG13	SEG13	SEG13	SEG13	32CH	-	-	-	SEG13
30DH	SEG14	SEG14	SEG14	SEG14	32DH	-	-	-	SEG14
30EH	SEG15	SEG15	SEG15	SEG15	32EH	-	-	-	SEG15
30FH	SEG16	SEG16	SEG16	SEG16	32FH	-	-	-	SEG16
310H	SEG17	SEG17	SEG17	SEG17	330H	-	-	-	SEG17
311H	SEG18	SEG18	SEG18	SEG18	331H	-	-	-	SEG18
312H	SEG19	SEG19	SEG19	SEG19	332H	-	-	-	SEG19
313H	SEG20	SEG20	SEG20	SEG20	333H	-	-	-	SEG20
314H	SEG21	SEG21	SEG21	SEG21	334H	-	-	-	SEG21
315H	SEG22	SEG22	SEG22	SEG22	335H	-	-	-	SEG22
316H	SEG23	SEG23	SEG23	SEG23	336H	-	-	-	SEG23
317H	SEG24	SEG24	SEG24	SEG24	337H	-	-	-	SEG24
318H	SEG25	SEG25	SEG25	SEG25	338H	-	-	-	SEG25
319H	SEG26	SEG26	SEG26	SEG26	339H	-	-	-	SEG26
31AH	SEG27	SEG27	SEG27	SEG27	33AH				SEG27

LCD 1/6 duty 1/3 bias (6X26)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	COM6	COM5
300H	SEG1	SEG1	SEG1	SEG1	320H	-	-	SEG1	SEG1
301H	SEG2	SEG2	SEG2	SEG2	321H	-	-	SEG2	SEG2
302H	SEG3	SEG3	SEG3	SEG3	322H	-	-	SEG3	SEG3
303H	SEG4	SEG4	SEG4	SEG4	323H	-	-	SEG4	SEG4
304H	SEG5	SEG5	SEG5	SEG5	324H	-	-	SEG5	SEG5
305H	SEG6	SEG6	SEG6	SEG6	325H	-	-	SEG6	SEG6
306H	SEG7	SEG7	SEG7	SEG7	326H	-	-	SEG7	SEG7
307H	SEG8	SEG8	SEG8	SEG8	327H	-	-	SEG8	SEG8
308H	SEG9	SEG9	SEG9	SEG9	328H	-	-	SEG9	SEG9
309H	SEG10	SEG10	SEG10	SEG10	329H	-	-	SEG10	SEG10
30AH	SEG11	SEG11	SEG11	SEG11	32AH	-	-	SEG11	SEG11
30BH	SEG12	SEG12	SEG12	SEG12	32BH	-	-	SEG12	SEG12
30CH	SEG13	SEG13	SEG13	SEG13	32CH	-	-	SEG13	SEG13
30DH	SEG14	SEG14	SEG14	SEG14	32DH	-	-	SEG14	SEG14
30EH	SEG15	SEG15	SEG15	SEG15	32EH	-	-	SEG15	SEG15
30FH	SEG16	SEG16	SEG16	SEG16	32FH	-	-	SEG16	SEG16
310H	SEG17	SEG17	SEG17	SEG17	330H	-	-	SEG17	SEG17
311H	SEG18	SEG18	SEG18	SEG18	331H	-	-	SEG18	SEG18
312H	SEG19	SEG19	SEG19	SEG19	332H	-	-	SEG19	SEG19
313H	SEG20	SEG20	SEG20	SEG20	333H	-	-	SEG20	SEG20
314H	SEG21	SEG21	SEG21	SEG21	334H	-	-	SEG21	SEG21
315H	SEG22	SEG22	SEG22	SEG22	335H	-	-	SEG22	SEG22
316H	SEG23	SEG23	SEG23	SEG23	336H	-	-	SEG23	SEG23
317H	SEG24	SEG24	SEG24	SEG24	337H	-	-	SEG24	SEG24
318H	SEG25	SEG25	SEG25	SEG25	338H	-	-	SEG25	SEG25
319H	SEG26	SEG26	SEG26	SEG26	339H	-	-	SEG26	SEG26

10. Interrupt

Three interrupt sources are available on SH67P51:

- Timer0 overflow interrupt
- Base timer overflow interrupt
- Port's falling edge detection interrupt (PBC)

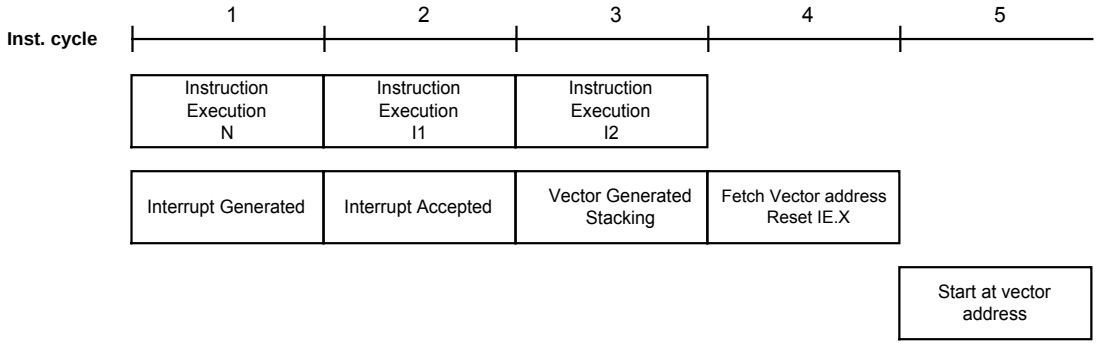
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 through $01 of the system register. They can be accessed or tested by the program. These flags are cleared to 0 at initialization by chip reset.

Address	Bit3	Bit2	Bit1	Bit0	Remarks
$00	-	IET0	IEBT	IEP	interrupt enable flags
$01	-	IRQT0	IRQBT	IRQP	interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1) , the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, thus, when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

11. HALT and STOP mode

After the execution of HALT instruction, SH67P51 will enter HALT mode. In HALT mode, the CPU will stop operating; however, the peripheral circuit (timer) will keep operating.

After the execution of STOP instruction, SH67P51 will enter STOP mode.
In STOP mode, the entire chip (including oscillator) will stop operating.
In HALT mode, SH67P51 can be woken up if an interrupt occurs.
In STOP mode, SH67P51 can be woken up if a port interrupt occurs.

12. Low Power Detect (LPD)

The LPD function monitors the supply voltage of the battery

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$06				LPD	R	Bit0: 2.3v LPD flag

Functions of LPD Circuit:
The LPD circuit has the following functions:

LPD bit =1 when $V_{DD} \leq V_{LPD}$ (= 2.3±0.1V)
LPD bit=0 when $V_{DD} > V_{LPD}$ (= 2.3±0.1V)

13. Low Voltage Reset (LVR)

The LVR function monitors the supply voltage and applies an internal reset in the micro-controller at battery replacement. If the applied circuit satisfies the following conditions, the LVR can be incorporated by the software control.

Functions of LVR Circuit:
The LVR circuit has the following functions:

Generates an internal reset signal when $V_{DD} \leq V_{LPD}$ (= 1.7±0.1V).

14. Watch Dog Timer

Watchdog timer is a down-count counter, and its clock source is OSC clock (32.768k X'tal or 131k RC). The watchdog timer automatically generates a device reset when it overflows. OTP option can enable and disable this function. The watchdog timer control registers (WDT bit0 – 2) select different overflow frequency. WDT bit3 is watchdog timer overflow flag.

System Register $1E (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power ON
$1E	WDF	WDT.2	WDT.1	WDT.0	R/W R	Bit0 – 2: Watch dog timer control WDF: Watchdog timer overflow flag. (Read only)	0000
	X	0	0	0		Watch dog timer-out period = 2^{17}/Fosc	Yes
	X	0	0	1		Watch dog timer-out period = 2^{15}/Fosc	
	X	0	1	0		Watch dog timer-out period = 2^{13}/Fosc	
	X	0	1	1		Watch dog timer-out period = 2^{11}/Fosc	
	X	1	0	0		Watch dog timer-out period = 2^{10}/Fosc	
	X	1	0	1		Watch dog timer-out period = 2^{9}/Fosc	
	X	1	1	0		Watch dog timer-out period = 2^{8}/Fosc	
	X	1	1	1		Watch dog timer-out period = 2^{7}/Fosc	
	0	X	X	X		No watchdog timer overflow reset	Yes
	1	X	X	X		Watchdog timer overflow	

For example:

When Fosc = 32.768kHz Crystal and WDT2-0 = 000, Watch dog timer-out period = 2^{17}/Fosc = 4s

When Fosc = 131kHz RC and WDT2-0 =000, Watch dog timer-out period = 2^{17}/Fosc = 1s

CPU will be reset when watchdog timer overflows. And read $1E will clear WDF bit to 0. In normal operation, read or write $1E, the watchdog timer should re-count before overflow happens.

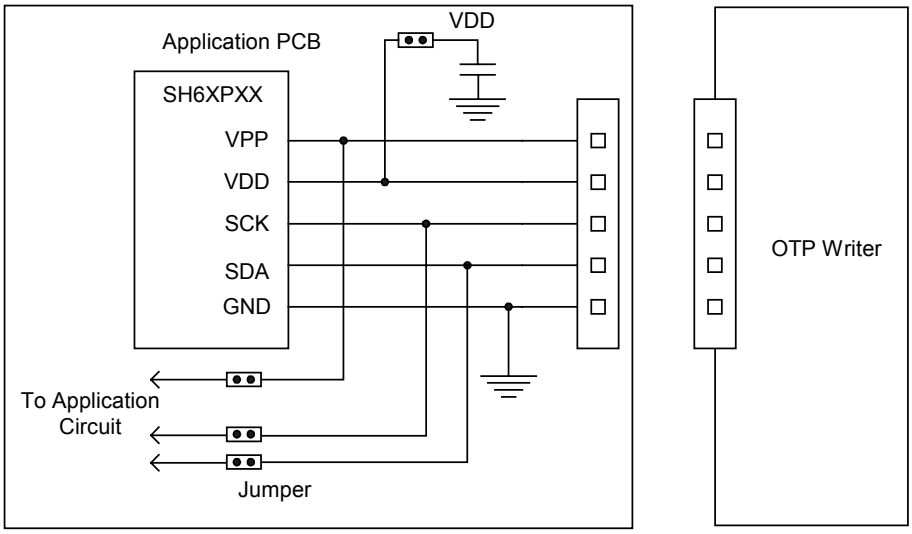
WDT function can be disabled by OTP option.

15. OTP option

(a). Internal pull-up resistor in $\overline{\text{RESET}}$ pad
0 = enable (default)
1 = disable
(b). Watch Dog Timer
0 = enable (default)
1 = disable
(c). OSC type select
0 = 32.768kHz crystal
1 = 131kHz RC

16. In System Programming Notice for OTP

For COB (chip on Board) assembling mode, the In System Programming technology is valid for OTP chip of SinoWealth Co.. The Programming Interface of OTP chip must be left on user's application PCB, and users can assemble all components including OTP chip in application PCB before programming OTP chip first. Of course it is accessible that bonding OTP chip only first, then programming code, and assembling the others components at last.
Because the programming timing of Programming Interface is very sensitive, so four jumpers are needed (VDD, VPP, SDA, SCK) to separate programming pins from application circuit just as following diagram.



The recommended step is as following for these jumpers:
1) The jumper is Open to separate programming pins from application circuit before programming code.
2) Connect the programming interface with OTP Writer and Begin Programming code.
3) Disconnect OTP writer and short these jumpers when programming is finished.
For more detail information please refer to the OTP writer user manual.

Instruction Set

All instructions are one cycle and one-word instructions. The characteristics are memory-oriented operation.
Arithmetic and Logical Instructions

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (,B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC [3]; AC [0] →CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx I I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

(4) In the assembler ASM66 V1.0, EORIM mnemonic is EORI. However, EORI has the same operation identical with EORIM. The same is true for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC; Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not include p)	
RTNW H; L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ←llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where:

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank = 000
P	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Rating*

DC Supply Voltage . . . . . .-0.3V to +6.0V

Input Voltage . . . . . –0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . –10℃to +70℃

Storage Temperature . . . . . –55℃to +125℃

***Comments**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, F_{OSCX} = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ	Max.	Unit	Condition
Operating Voltage	V_{DD}	1.8	3.0	3.6	V	
Operating Current	I_{OP}		0.3	0.5	mA	All output pins unload, LCD on (Execute NOP instruction)
HALT Current	I_{SB1}		4	6	μA	Fosc=32.768k crystal, OSCX off LCD on, without LCD panel WDT on All output pins unload (HALT mode)
STOP Current	I_{SB2}			1	μA	OSC STOP ALL output pins unload
REM sink current	I_{REM1}	0.3			mA	V_{REM1} = 0.3V
REM driving current	I_{REM2}	-5	-9		mA	V_{REM2} = 1V
Input Low Voltage	V_{IL1}	GND-0.3		V_{DD} X 0.3	V	I/O ports, pins tri-state.
Input Low Voltage	V_{IL2}	GND-0.3		V_{DD} X 0.15	V	$\overline{\text{RESET}}$, TEST, OSCI (Schmitt trigger input)
Input High Voltage	V_{IH1}	V_{DD} X 0.7		V_{DD}+0.3	V	I/O Ports, pins tri-state
Input High Voltage	V_{IH2}	V_{DD} X 0.85		V_{DD}+0.3	V	$\overline{\text{RESET}}$, TEST, OSCI (Schmitt trigger input)
Input Leakage Current	I_{IL}	-1		1	μA	Input Pad, V_{IN} =GND or VDD
Output High Voltage	V_{OH1}	V_{DD} – 0.7			V	PortB-PortE, I_{OH} = -0.5mA
Output High Voltage	V_{OH2}	V_{DD}-0.7			V	PortA , I_{OL} = -5mA
Output Low Voltage	V_{OL1}			GND + 0.6	V	PortB-PortE, I_{OL} = 1mA
Output Low Voltage	V_{OL2}			GND + 0.6	V	PortA, I_{OL} = 10mA
Pull-up Resistor	R_P		150		kΩ	Internal pull-up resistor on I/O and reset
LCD ON driving resistor	R_{ON}	-	5	-	kΩ	SEG1~29, COM1~6

Low Power Detect Circuitry(T_A =25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Low Power Detect voltage	V_{LPD}	2.2	2.3	2.4	V	
Low Voltage Reset voltage	V_{LVR}	1.6	1.7	1.8	V	

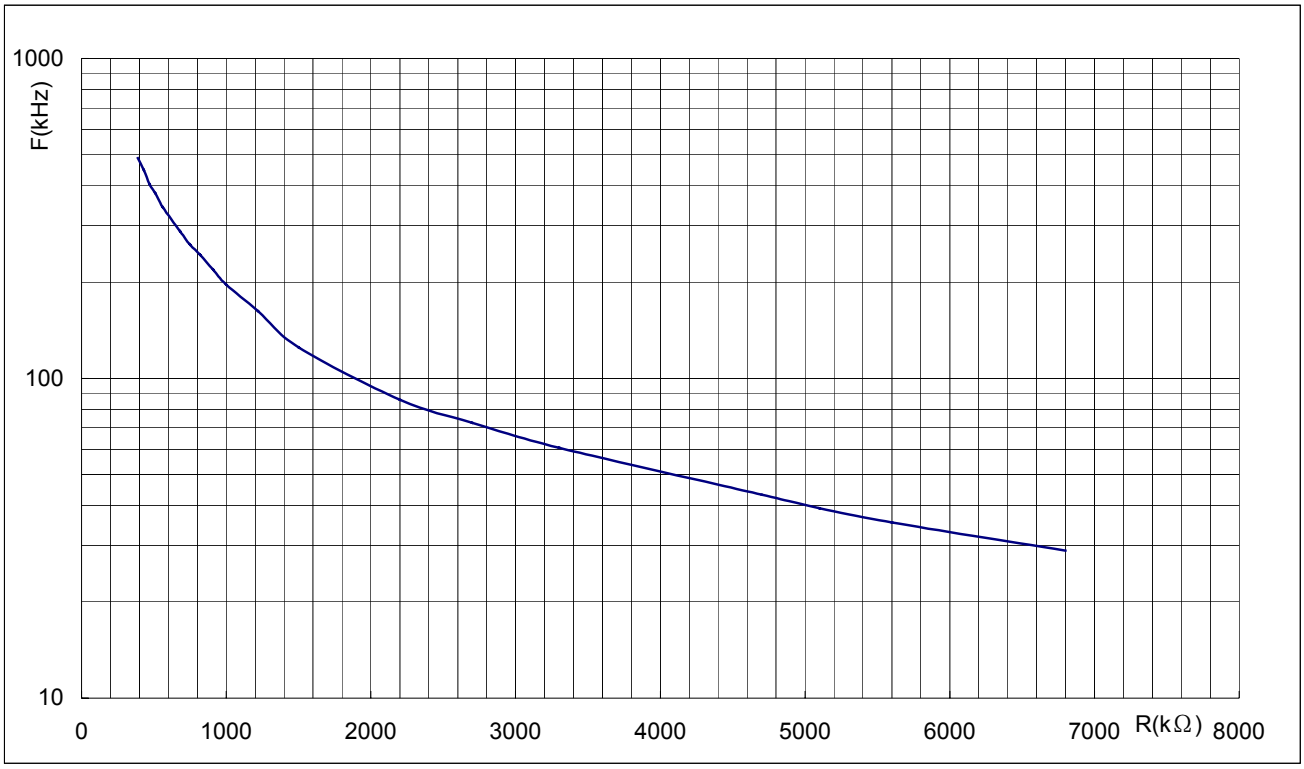
LCD Voltage Regulator Circuitry(V_{DD} = 2.0-3.6V, GND = 0V, T_A =5-45℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Regulator output voltage (VP2 output voltage)	V2	1.8	2.1	2.4	V	Connecting a 200k resistor between VP2 and GND. Without LCD panel load

AC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, internal RC oscillator, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillator Start time	Tosc		1	2	s	Oscillator = 32.768KHz
Internal RC Frequency Variation	Foscx	3.92	4	4.08	MHz	V_{DD} =2.0-3.6V, T_A = +5℃ to +45℃

Low frequency RC oscillator Resistor vs. Frequency: (V_{DD} = 3V, for reference only)

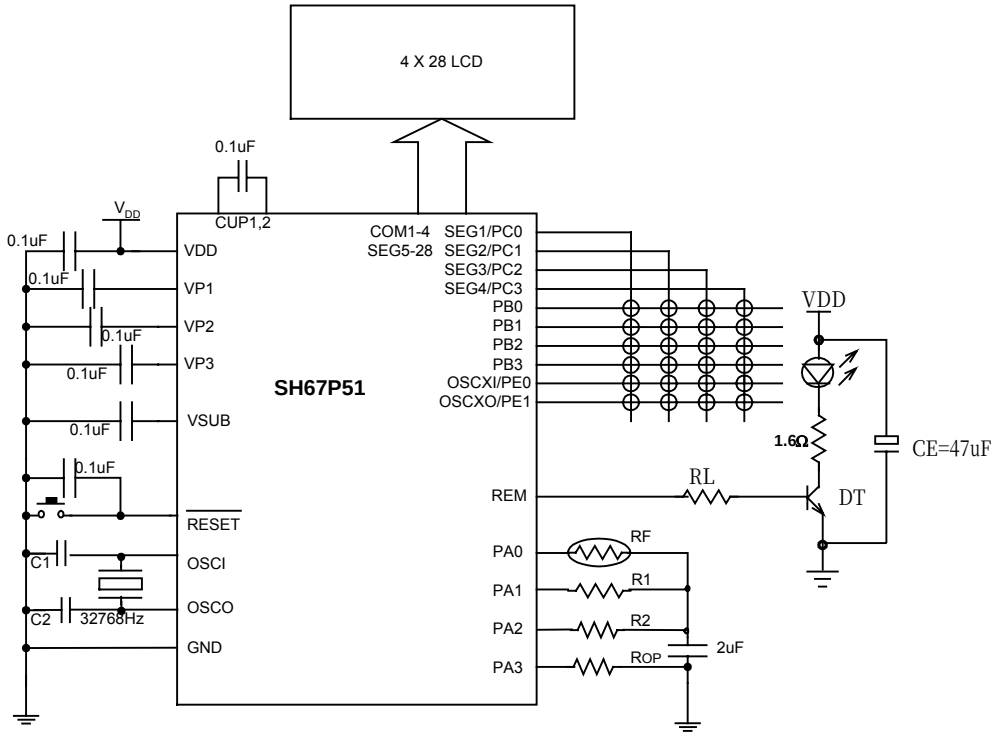


Application Circuit (for reference only)

AP1:

Remote Control (24 Keys)

(5) Oscillator: Internal RC (OSCXI & OSCXO shared to PortE0, 1)
(6) PortA0-2: I/O Buffers
(7) PortB, PortA3 and PortE: Input Buffers
(8) Internal pull high in $\overline{\text{RESET}}$ pin
(9) WDT on
(10) RL = 0 is possible, but the REM specification is revised to reduce power consumption

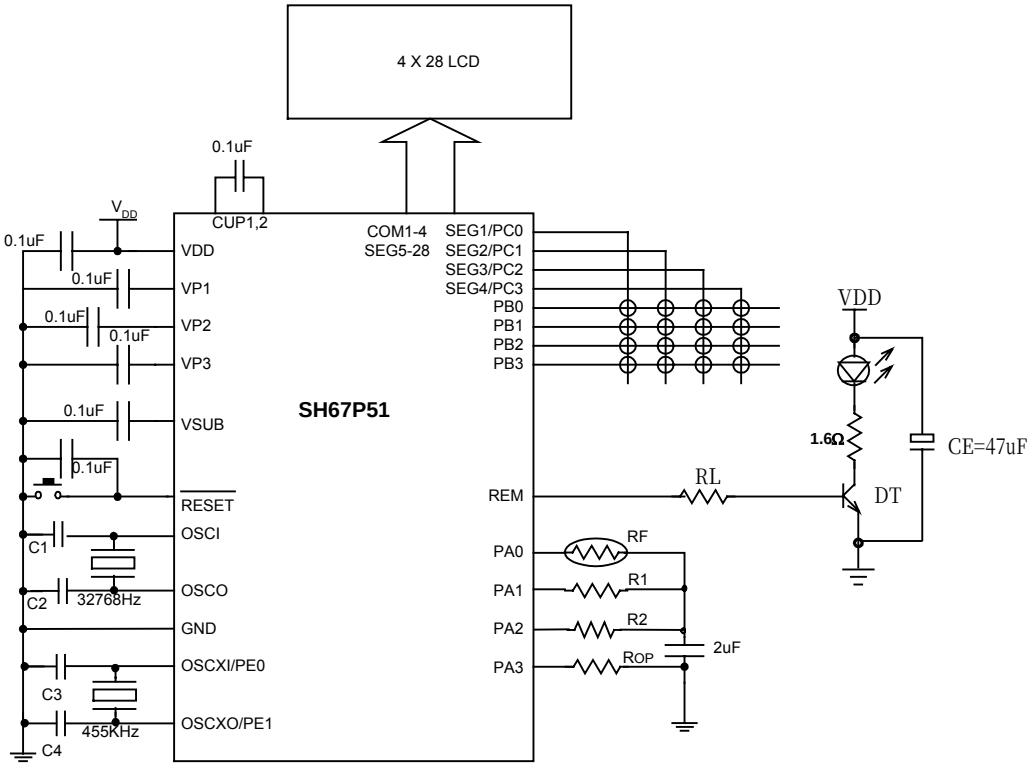


RF: Temperature Sensor
R1,2: Reference Resister
ROP: Option Resister
C1, C2: 12pF for reference. (Please refer to the oscillator spec)

AP2:

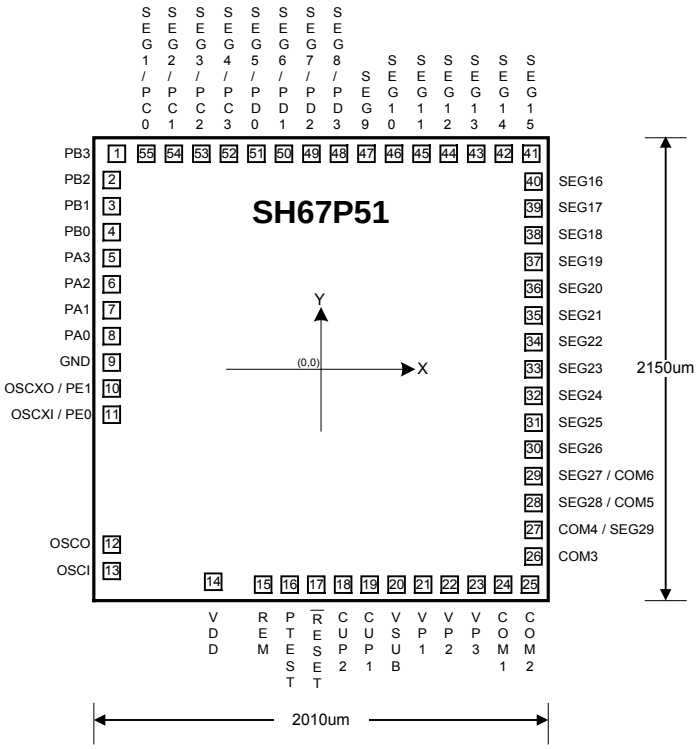
Remote Control (16 Keys)

(11) Oscillator: 455kHz Ceramic oscillator
(12) PortA0-2: I/O Buffers
(13) PortB, PortA3: Input Buffers
(14) Internal pull high in $\overline{\text{RESET}}$ pin
(15) WDT on
(16) RL = 0 is possible, but the REM specification is revised to reduce power consumption



RF: Temperature Sensor
R1,2: Reference Resister
ROP: Option Resister
C1, C2: 12pF for reference. (Please refer to the oscillator spec)
C3, C4: 20~200pF. (Please refer to the oscillator spec)

Bonding Diagram



* Substratum connects to GND.

Pad Location

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PB3	-867.5	947.5	19	CUP1	172.5	-947.4
2	PB2	-878.5	810.05	20	VSUB	287.5	-947.4
3	PB1	-878.5	690.05	21	VP1	402.5	-947.4
4	PB0	-878.5	570.05	22	VP2	517.5	-947.4
5	PA3	-878.5	455.05	23	VP3	632.6	-947.4
6	PA2	-878.5	340.05	24	COM1	747.5	-947.4
7	PA1	-878.5	225.05	25	COM2	867.5	-947.4
8	PA0	-878.5	110.05	26	COM3	878.5	-809.95
9	GND	-878.5	-4.95	27	COM4 / SEG29	878.5	-689.95
10	OSCXO	-878.5	-119.95	28	SEG28 / COM5	878.5	-574.95
11	OSCXI	-878.5	-234.95	29	SEG27 / COM6	878.5	-459.95
12	OSCO	-878.5	-796.3	30	SEG26	878.5	-344.95
13	OSCI	-878.5	-911.3	31	SEG25	878.5	-229.95
14	V_{DD}	-494.8	-933.4	32	SEG24	878.5	-114.95
15	REM	-291.1	-947.4	33	SEG23	878.5	0.05
16	TEST	-174.3	-947.4	34	SEG22	878.5	115.05
17	$\overline{\text{RESET}}$	-57.5	-947.4	35	SEG21	878.5	230.05
18	CUP2	57.5	-947.4	36	SEG20	878.5	345.05

Pad Location (continued)

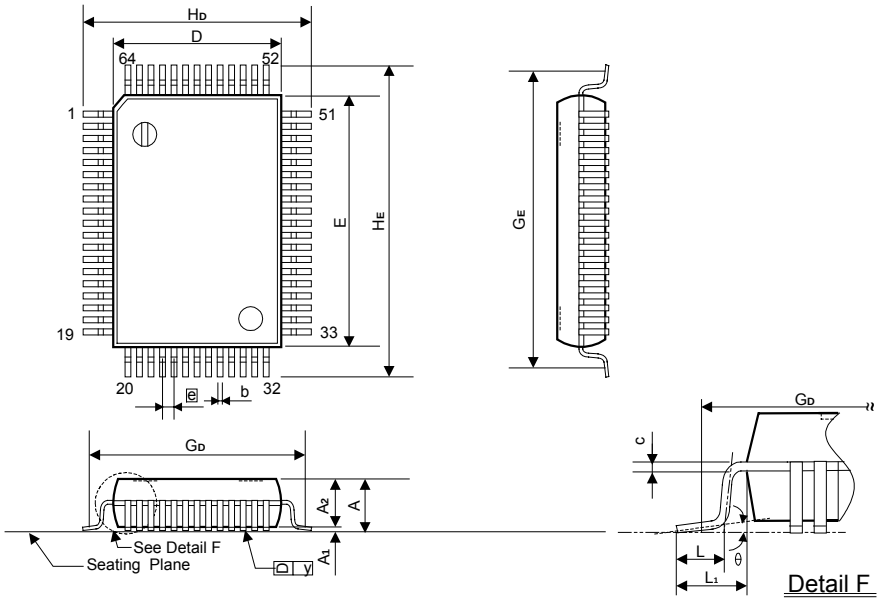
Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
37	SEG19	878.5	460.05	47	SEG9	172.5	947.5
38	SEG18	878.5	575.05	48	SEG8 / PD3	57.5	947.5
39	SEG17	878.5	690.05	49	SEG7 / PD2	-57.5	947.5
40	SEG16	878.5	810.05	50	SEG6 / PD1	-172.5	947.5
41	SEG15	872.5	947.5	51	SEG5 / PD0	-287.5	947.5
42	SEG14	747.5	947.5	52	SEG4 / PC3	-402.5	947.5
43	SEG13	632.5	947.5	53	SEG3 / PC2	-517.5	947.5
44	SEG12	517.5	947.5	54	SEG2 / PC1	-632.5	947.5
45	SEG11	402.5	947.5	55	SEG1 / PC0	-747.5	947.5
46	SEG10	287.5	947.5				

Ordering Information

Part No.	Package
SH67P51H	Chip form
SH67P51F	QFP 64L

QFP 64L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.130 Max.	3.30 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.112 ± 0.005	2.85 ± 0.13
b	0.016 +0.004 -0.002	0.40 +0.10 -0.05
c	0.006 +0.004 -0.002	0.15 +0.10 -0.05
D	0.551 ± 0.005	14.00 ± 0.13
E	0.787 ± 0.005	20.00 ± 0.13
e	0.039 ± 0.006	1.00 ± 0.15
G_D	0.693 NOM.	17.60 NOM.
G_E	0.929 NOM.	23.60 NOM.
H_D	0.740 ± 0.012	18.80 ± 0.31
H_E	0.976 ± 0.012	24.79 ± 0.31
L	0.047 ± 0.008	1.19 ± 0.20
L_1	0.095 ± 0.008	2.41 ± 0.20
y	0.006 Max.	0.15 Max.
θ	0° ~ 12°	0° ~ 12°

Notes:

1. Dimensions D & E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

Specification Revision History

Version	Content	Date
V0.4	Add information about QFP 64L package and pin description. Add bonding diagram. Add low frequency RC Frequency-Resistance diagram. Add information about OTP programming. Change warm up counter.	2003/12/10
V0.3	Add a Pad “VSUB” and change the application current, Change the reset value of the $15	2003/08/06
V0.2	Change address of system register and RAM, change WDT reset value of $1E. Change the definition of voltage regulator and LPD.	2003/07/14
V0.1	Original	2003/06/09