SH67P33

OTP 4-bit Microcontroller

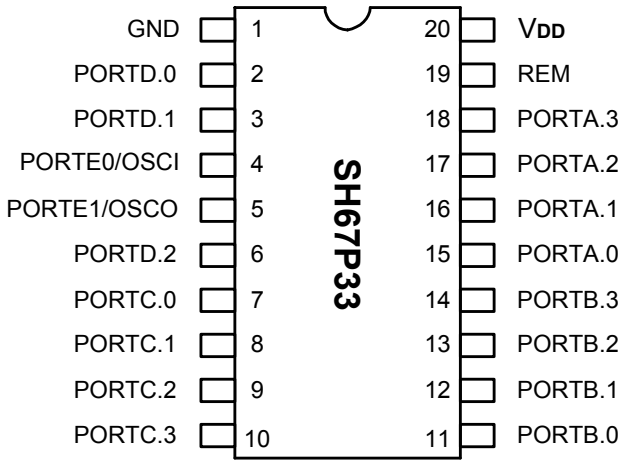
Features

- SH6610C-based single-chip 4-bit micro-controller
- ROM: 1024 X 16 bits OTP ROM
- RAM: 48 X 4 bits RAM (Data Memory)
- Operation voltage: 1.8V – 3.6V (Typically 3.0V)
- 17 CMOS bi-directional I/O pins
- 4-level subroutine nesting (including interrupts)
- One 8-bit auto re-loadable timer/counter
- Warm-up timer for power-on reset
- Powerful interrupt sources:
  - Internal interrupt (Timer0).
  - External interrupts: PortB & PortC (rising edge).
- Built-in remote control programmable carrier synthesizer
- Oscillator
  Ceramic resonator: 400K - 4MHz.
  Build-in RC oscillator: 4MHz ± 2%
- Instruction cycle time:
  - 4/455KHz (≈ 8.79μs) for 455KHz OSC clock
  - 4/4MHz (= 1μs) for 4MHz OSC clock
- Two low power operation modes: HALT and STOP
- Built-in watchdog timer
- Oscillator select (code option)
- Port interrupt source select (code option)

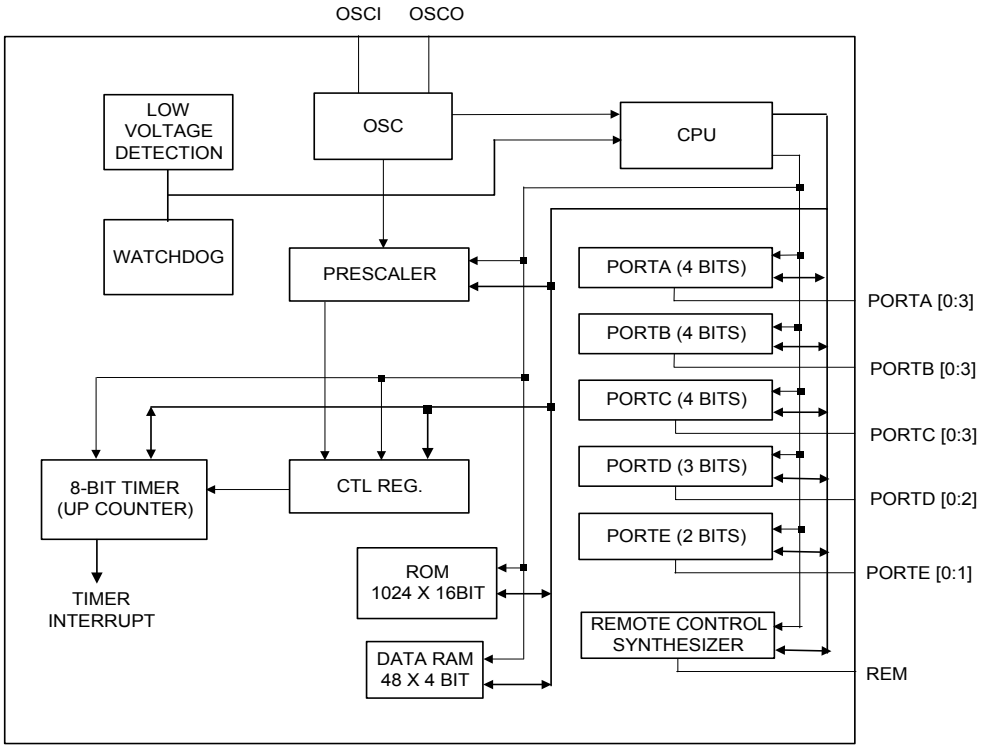
General Description

SH67P33 is dedicated to infrared remote control transmitter applications. This chip integrates the SH6610C 4-bit CPU core with SRAM, program ROM, one 8-bit timer, and programmable input/output driving buffers and carrier synthesizer. The standby function, which can be used to stop/start the ceramic resonator or internal RC oscillation, facilitating the low power dissipation of the system.

Pin Configuration



Block Diagram



Pin Descriptions

Pin No.	Designation	I/O	Descriptions
7~10	PC0 ~ PC3	I/O	Bit programmable I/O pins, Vector Interrupt (Active rising edge).
2	PD0	I	Input pin.
3, 6	PD1 ~ PD2	I/O	Bit programmable I/O pins.
19	REM	O	Carrier synthesizer for infrared or RF output pin.
20	V_{DD}	P	Power supply.
4	PE0/OSCI	I/O	Bit programmable I/O pin, shared with oscillator input pin connected to ceramic oscillator
5	PE1/OSCO	I/O	Bit programmable I/O pin, shared with oscillator output pin connected to ceramic oscillator.
1	GND	P	Ground pin.
15~18	PA0 ~ PA3	I/O	Bit programmable I/O pins.
11~14	PB0 ~ PB3	I/O	Bit programmable I/O pins, Vector Interrupt (Active rising edge).

Functional Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 1K program ROM. It consists of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1 and PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BC);
(2) When executing a subroutine call instruction (CALL);
(3) When an interrupt occurs;
(4) When the chip is at the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

1.2. ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)

Decision (BA0, BA1, BA2, BA3, BAZ, BC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow, which the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and restored back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Stack

A group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. It is organized 13 bits × 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of stack will be shifted out.

2. ROM

The SH67P33 can address 1024 X 16 bit of program area from $000 to $3FF.

Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000H	JMP	Jump to RESET
$001H	NOP	Reserved
$002H	JMP	Jump to TIMER0
$003H	NOP	Reserved
$004H	JMP	Jump to PBC

3. RAM

Built-in RAM consists of general purpose data memory and system registers.
Data memory and the system register can be accessed by direct addressing in one instruction.
The following is the memory allocation map:
$000 - $01F: System register and I/O; $020 - $04F: Data memory (48 × 4 bits).
Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Description
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)
$03	-	-	-	-	-	Reserved
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit
$06	-	-	-	-	-	Reserved
$07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	-	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	PE.1	PE.0	R/W	PORTE
$0D	-	-	-	REMO REM	W R	Bit0: REMO output data. Bit0: REM pin output status.
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	PPULL	CPS2	CPS1	CPS0	R/W	Bit2-0: Carrier OSC pre-divider Bit3: Port Pull-low MOS Control
$14	$\overline{\text{WDT}}$	-	-	-	R/W	Bit3: Watchdog timer reset/flag (write 1 to reset WDT)
$15	LPD3	LPD2	LPD1	LPD0	R/W	LPD Enable Control (LPD3 ~ 0): 1010: LPD Disable Else: LPD Enable (Power-on initial 0000)
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	Set PORTA to be output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	Set PORTB to be output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	Set PORTC to be output port
$19	-	PD2OUT	PD1OUT	0	R/W	Set PORTD to be output port
$1A	-	-	PE1OUT	PE0OUT	R/W	Set PORTE to be output port
$1B	CFL3	CFL2	CFL1	CFL0	R/W	Carrier low level timer load data register
$1C	CFL7	CFL6	CFL5	CFL4	R/W	Carrier low level timer load data register
$1D	CFH3	CFH2	CFH1	CFH0	R/W	Carrier high level timer load data register
$1E	CFH7	CFH6	CFH5	CFH4	R/W	Carrier high level timer load data register
$1F	-	-	-	-	-	Reserved

4. Timer0

4.1. Configuration and Operation

Timer-0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The counter and load register both have low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

Load register programming: Write the low-order digit first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since register H controls the physical READ/WRITE operations, follow the following rules:

Write Operation:

Low nibble first;
High nibble to update the counter

Read Operation:

High nibble first;
Followed by Low nibble.

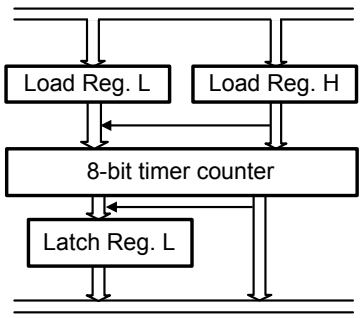


Figure. 1 Timer Load register Configure

4.2. Timer0 Interrupt

The timer overflow will generate an internal interrupt request when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will start. This can also be used to wake CPU from HALT mode.

4.3. Timer0 Mode Register

The timer can be programmed in several different pre-scaler ratios by setting Timer Mode Register (TM0).
The 8-bit counter counts pre-scaler overflow output pulses. The TIMER mode registers (TM0) are 3-bit registers used for timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Register

TM0.2	TM0.1	TM0.0	Pre-scaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^{9}$	512
0	1	0	$/2^{7}$	128
0	1	1	$/2^{5}$	32
1	0	0	$/2^{3}$	8
1	0	1	$/2^{2}$	4
1	1	0	$/2^{1}$	2
1	1	1	$/2^{0}$	1

5. I/O PORT

The SH67P33 provides 17 I/O pins. Each I/O pin contains pull-low MOS controllable by the program. When every I/O is used as an input port, the port control register (PCR) controls ON/OFF of the output buffer. Sections below show the circuit configuration of I/O ports.

PORTA, PORTB, PORTC, PORTD and PORTE
Each of these ports contains 4 bit I/O pins (PortD contains 2 bit I/O pins and 1 input pin, PortE contains 2 bit I/O pins). ON/OFF of the output buffer for port can be controlled by the port control register (PCRA, PCRB, PCRC, PCRD and PCRE) . Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	-	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	PE.1	PE.0	R/W	PORTE

- The following is the circuit configuration diagram:

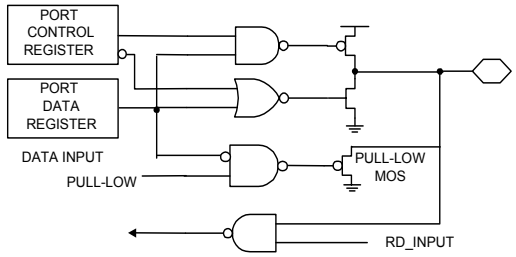


Figure. 2 Port Configuration Function Block Diagram

Port I/O Control Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	Set PORTA as output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	Set PORTB as output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	Set PORTC as output port
$19	-	PD2OUT	PD1OUT	0	R/W	Set PORTD as output port
$1A	-	-	PE1OUT	PE0OUT	R/W	Set PORTE as output port

I/O control register: PAXOUT, PBXOUT, PCXOUT, (X = 0, 1, 2, 3) PD2OUT, PD1OUT, PE1OUT, PE0OUT
1: Set I/O as an output buffer.
0: Set I/O as an input buffer (power-on initial).

Controlling the pull-low MOS

These ports contain pull-low MOS controlled by the program. PPULL register controls On/Off of all pull-low MOS simultaneously. Pull-low MOS is controlled by the port data registers (PA, PB, PC, PD and PE) of each port also. Thus, the pull-low MOS can be turned on and off individually.

Port Function Control (PMOD) is below:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PPULL	CPS2	CPS1	CPS0	R/W	Bit3: Port Pull-low MOS Control

PPULL Port Pull-low MOS enables control
0 = Disable PORT pull-low MOS (power-on initialization)
1 = Enable PORT pull-low MOS

Port Interrupt

The PORTB, PORTC and PORTD are used as port interrupt sources. Since PORT I/O is a bit programmable I/O, therefore only the input port can generate an external interrupt. Any transitions from PORTB and PORTC input pins from GND to **VDD** will generate an interrupt request (Default). when opt_pint is HIGH, PORTB、PORTC and PORTD as the port interrupt source. Thus, further rising edge transitions can not be able to make interrupt request until all of the pins return to GND. The following is the port interrupt function block-diagram.

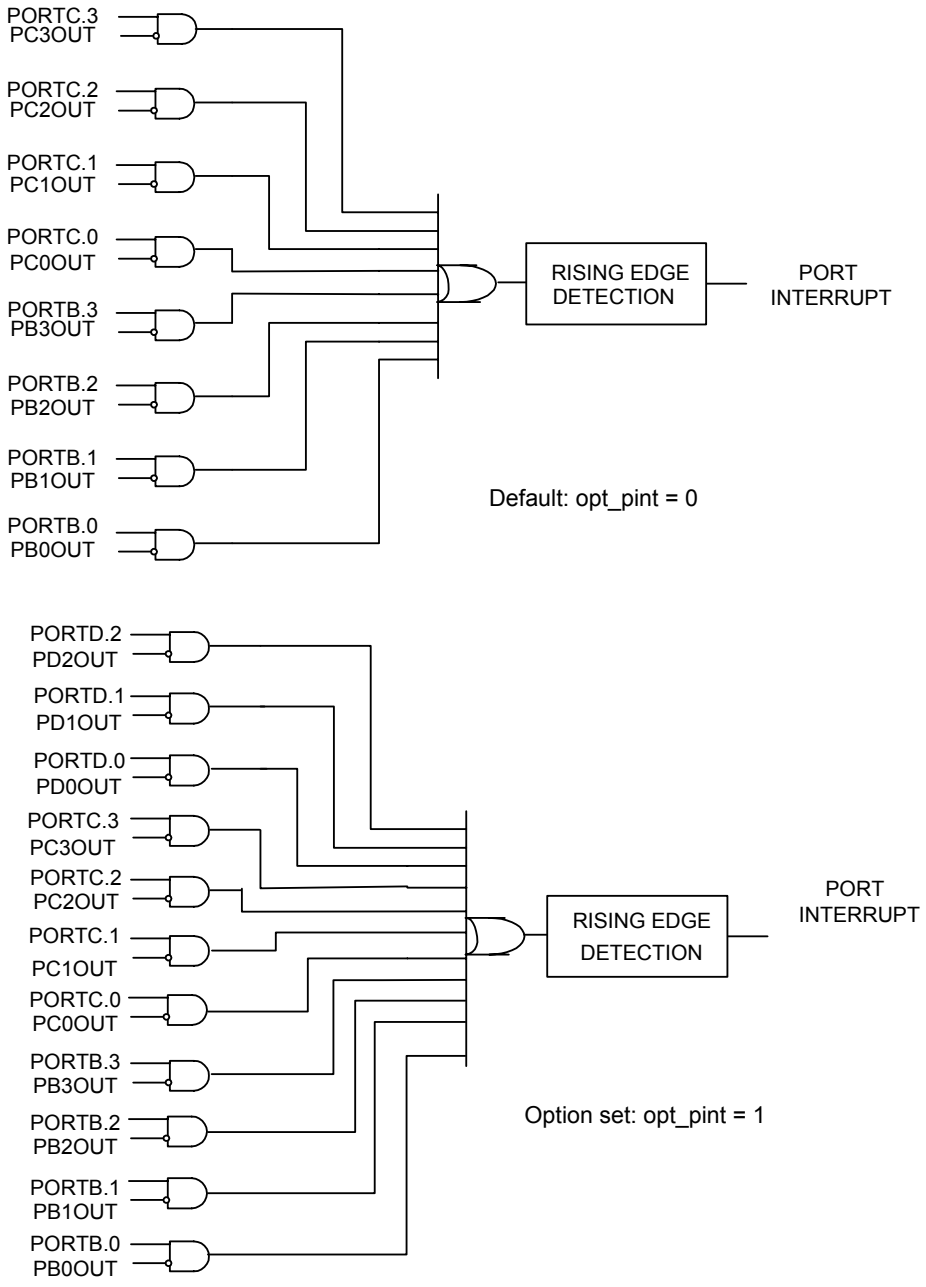


Figure. 3 PORT Interrupt Block Diagram

6. Remote Control Synthesizer

SH67P33 builds-in a carrier synthesizer for infrared or RF remote control circuits.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$0D	-	-	-	REMO REM	W R	Bit0: REMO output data. Bit0: REM pin output status.
$13	PPULL	CPS2	CPS1	CPS0	R/W	Bit2-0: Carrier count source pre-divider Bit3: Port Pull-low MOS Control

REMO: Remote output data control. The REM pin output status can be ready by instruction.
CPS2~0: Carrier counter source pre-divider control Register
The carrier synthesizer can be programmed in several different pre-scaler ratios by setting CPS2~0.

Carrier count source pre-divider control Register

CPS2	CPS1	CPS0	Pre-scaler Divide Ratio	Ratio N
0	0	0	System clock/2^{11}	2048 (initial)
0	0	1	System clock /2^{9}	512
0	1	0	System clock /2^{7}	128
0	1	1	System clock /2^{5}	32
1	0	0	System clock /2^{3}	8
1	0	1	System clock /2^{2}	4
1	1	0	System clock /2^{1}	2
1	1	1	System clock /2^{0}	1

The carrier-generating counter is an 8bit count-up counter and it has two reload data register. The counter and load registers both have low order digits and high order digits. Writing data into the timer load registers ($1B,$1C,$1D,$1E) can initialize the counter.

After system reset, the counter is automatically loaded with the contents of high level timer load data register ($1E,$1D)and output high level at the same time. Following when counter counts overflow from $FF to $00,the counter is automatically loaded with the contents of low level timer load data register ($1C,$1B) and output low level at the same time. When counter counts overflow again from $FF to $00 again, the counter will be loaded with the contents of high level timer load data register again. The above sequences make up a complete loop. So the carrier synthesizer can output continuous carrier wave of certain duties and certain period.

If bit0 of $0D(REMO) is set to 1from 0,the carrier counter will be initialized to load high level timer load data register and output high level whatever states the counter is.

Load register programming: User can modify low level timer load data register ($1B,$1C) to change the width of the low level. User can also modify high level timer load data register($1D,$1E)to change the width of high level. In the way the carrier synthesizer can output carrier wave of different duties and different period.

Carrier load data register

$1B	CFL3	CFL2	CFL1	CFL0	R/W	Carrier low level timer load data register
$1C	CFL7	CFL6	CFL5	CFL4	R/W	Carrier low level timer load data register
$1D	CFH3	CFH2	CFH1	CFH0	R/W	Carrier high level timer load data register
$1E	CFH7	CFH6	CFH5	CFH4	R/W	Carrier high level timer load data register

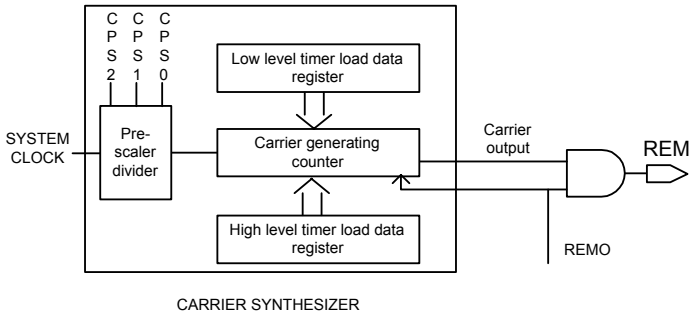


Figure. 4 Remote Control Functional Block Diagram

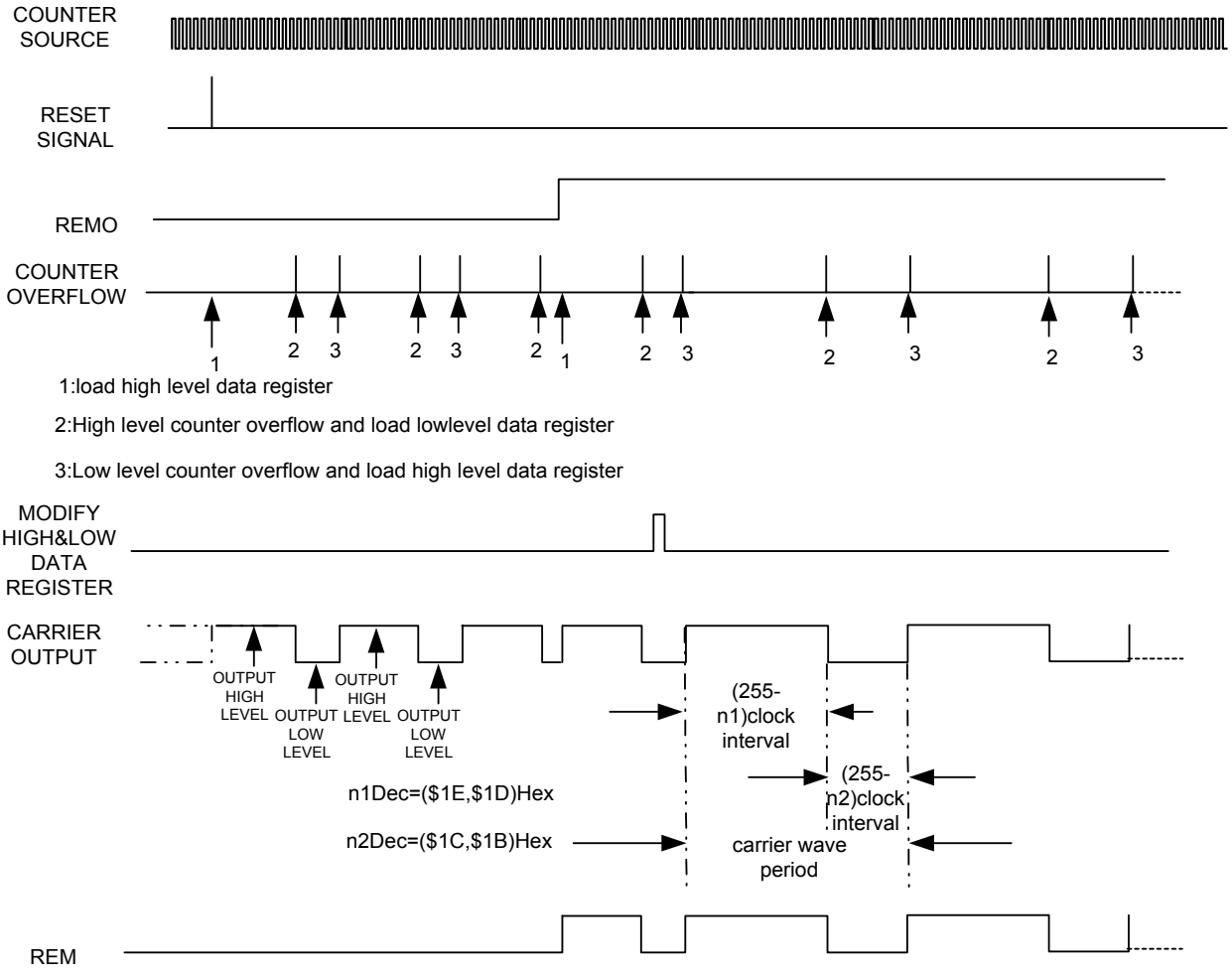


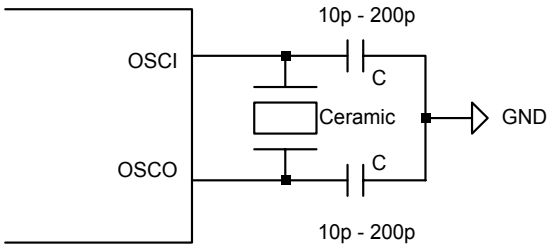
FIGURE.5 CARRIER SYNTHESIZE WAVE

7. System Clock and Oscillator

The System clock generator produces the basic clock pulses that provide the system clock with CPU and peripherals Instruction cycle time:
(1) 4/455KHz (≈ 8.79μs) for 455KHz system clock.
(2) 4/4MHz (= 1μs) for 4MHz system clock.

Oscillator

(1) Ceramic resonator: 400KHz - 4MHz.



(2) Internal oscillator: 4MHz.

8. Interrupt

Two interrupt sources are available on SH67P33:
-Timer0 overflow interrupt
-Port's rising edge detection interrupt (PBC)

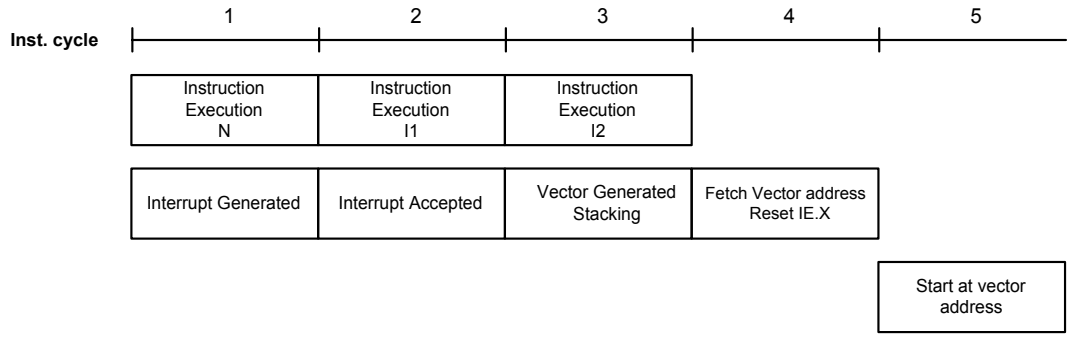
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 through $01 of the system register. They can be accessed or tested by the program. These flags are cleared to 0 at initialization by chip reset.

Address	Bit3	Bit2	Bit1	Bit0	Remarks
$00	-	IET0	-	IEP	interrupt enable flags
$01	-	IRQT0	-	IRQP	interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1) , the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, thus, when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

9. HALT and STOP mode

After the execution of HALT instruction, SH67P33 will enter HALT mode. In HALT mode, the CPU will stop operating; however, the peripheral circuit (timer) will keep operating.
After the execution of STOP instruction, SH67P33 will enter STOP mode.
In STOP mode, the entire chip (including oscillator) will stop operating.
In HALT mode, SH67P33 can be woken up if an interrupt occurs.
In STOP mode, SH67P33 can be woken up if a port interrupt occurs.

10. Warm-up Timer

The SH67P33 has a built in oscillator warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:
(1) Power-on reset
(2) Wake-up from STOP mode

The warm-up time interval (F**osc**/8192 cycles of oscillator) is a follows:
(1) Power-on reset interval is as long as the initial oscillator's frequency mode warm-up timer interval.
When SH67P33 operates in 455K Hz frequency, the warm-up time interval is 18 ms.
(2) 4MHz crystal oscillator wake-up:
When SH67P33 operates in 4 MHz frequency, the warm-up time interval is 2 ms.

11. Low Power Detection (LPD)

The LPD function monitors the supply voltage and applies an internal reset in the micro-controller at battery replacement. If the applied circuit satisfies the following conditions, the LPD can be incorporated by the software control.

Functions of LPD Circuit:

The LPD circuit has the following functions:

Generates an internal reset signal when $V_{DD} \leq V_{LPD}$ ($\approx$ 1.6V).

Stops the oscillator operation and force the CPU to enter STOP mode when $V_{DD} \leq V_{LPD}$. As $V_{DD} \leqq V_{LPD}$, the LPD reset will delay about 1ms before being triggered. If V_{DD} goes back to $V_{DD} > V_{LPD}$, the system will cancel the LPD reset.

LPD Control Register

The LPD circuit is controlled by the software enable flag.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 ~ 0): 1010: LPD Disable Else: LPD Enable (Power-on initial 0000)

12. Watch Dog Timer

Watch dog timer is a 16-bit down-count counter, and its clock source is internal RC oscillator. The watchdog timer automatically generates a device reset when it overflows. To prevent it timing out and generating a device RESET condition, users should write bit3 of system register $14 as “1” before timing-out. The WDT has a time-out period of approx. 16ms. WDT bit3 is watchdog timer overflow flag.

System Register $1F (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power ON
$14	$\overline{\text{WDT}}$				R/W	Bit3: Watchdog timer reset/flag (write 1 to reset WDT)	1000

The $\overline{\text{WDT}}$ bit is cleared only if the Watchdog Timer time-out occurred both in normal operation mode and in the HALT mode. The Watchdog Timer is cleared when the device wakes up from the STOP mode, regardless of the source of wake-up.

Initial State

There are 3 types of system resets:

1. Power-on reset
2. Low Power Detection reset
3. Watchdog reset

Hardware	After power-on reset	After LPD reset	After WDT reset
Program counter	$000	$000	$000
CY	Undefined	Unchanged	Unchanged
Data memory	Undefined	Unchanged	Unchanged
System register	Undefined	Unchanged	Unchanged
AC	Undefined	Unchanged	Unchanged
Timer counter	0	Unchanged	Unchanged
Timer load register	0	Unchanged	Unchanged
LPD	0000	0000	Unchanged
I/O ports	Input	Input	Input
PPULL	0	Unchanged	Unchanged
CPS2~0	Undefined	Unchanged	Unchanged
Carrier low level timer load data register	Undefined	Unchanged	Unchanged
$\overline{WDT}$	1	1	0
REMO	0	0	0

OTP Option list

(a) Oscillator select
0 = 4MHz Build in RC oscillator (default)
1 = 455KHz Ceramic oscillator

(b) Port interrupt source select
0 = Port B,Port C interrupt (default)
1 = Port B,Port C,Port D interrupt

Instruction Set

All instructions are one cycle and one-word instructions. The characteristics are memory-oriented operation.
Arithmetic and Logical Instructions

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (,B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC [3]; AC [0] →CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx I I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM mnemonic is EORI. However, EORI has the same operation identical with EORIM. The same is true for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not include p)	
RTNW H; L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ←llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where:

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank = 000
P	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Rating*

DC Supply Voltage . . . . . .-0.3V to +6.0V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . -10℃to +70℃

Storage Temperature . . . . . -55℃to +125℃

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = -10 to 70℃, F_{OSC} = 4MHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	1.8	3.0	3.6	V	
I_{OP}	Operating Current		0.3	1	mA	All output pins unload (Execute NOP instruction)
I_{SB1}	HALT Current		200		μA	CPU in HALT mode; ALL output pins unload, LPD off
I_{SB2}	STOP Current			1	μA	OSC STOP ALL output pins unload, LPD off
I_{REML}	REM sink current	0.3			mA	V_{REM} = 0.3V
I_{REMH}	REM driving current	-5	-9		mA	V_{REM} = 1V
V_{IL}	Input Low Voltage	GND		V_{DD} X 0.3	V	I/O ports, pins tri-state.
V_{IH}	Input High Voltage	V_{DD} X 0.7		V_{DD}	V	I/O Ports, pins tri-state
I_{IH}	High-level Input Current			0.2	μA	I/O ports; $V_{I/O}$ = 3.0V
I_{IL1}	Low-level Input Current	-30		-10	μA	I/O ports with pull-low; $V_{I/O}$ = V_{DD}
I_{IL2}	Low-level Input Current			-0.2	μA	I/O ports without pull-low; $V_{I/O}$ = V_{DD}
V_{OH}	Output High Voltage	V_{DD} - 0.7			V	I/O ports, I_{OH} = -5.0mA
V_{OL}	Output Low Voltage			GND + 0.6	V	I/O ports, I_{OL} = 1mA

LPD Circuitry (T_A = –10℃ to +70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{LPD}	LPD-detected Voltage	1.2	1.5	1.8	V	
I_{LPD}	LPD circuit current		2.0	3.5	μA	

AC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, internal RC oscillator, unless otherwise specified)

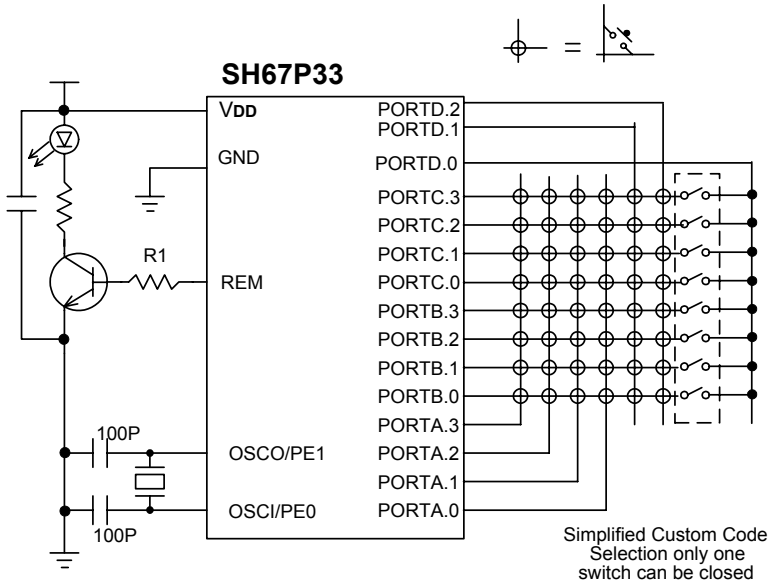
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Tosc	Oscillator Start time			20	ms	Ceramic Oscillator = 455KHz
|ΔF|/F	Frequency Stability	-	-	1	%	| F(V_{DD}) - F(3.0)| / F(3.0); V_{DD}=2.0~3.6V
Fosc	Frequency Variation	3.92	4	4.08	MHz	V_{DD}=2.0 to 3.6V, T_A = +5℃ to +45℃

Application Circuit (for reference only)

AP1:

Remote Control (48 Keys)

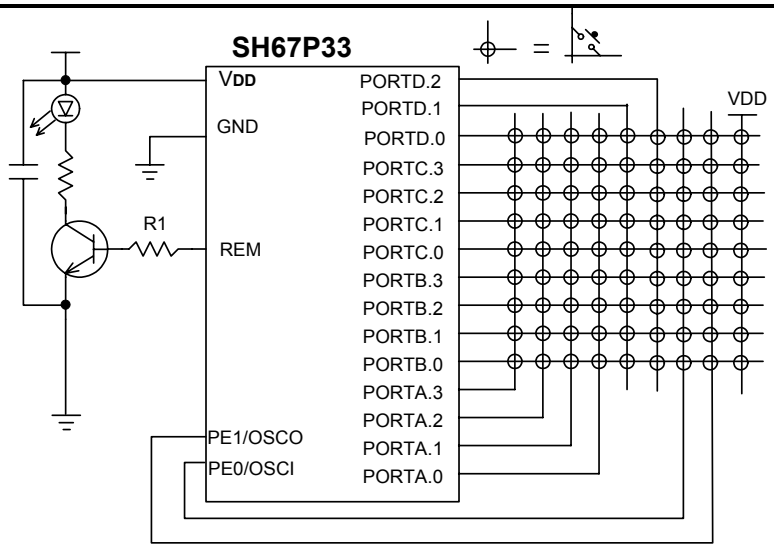
(1) Oscillator: Ceramic 455KHz(PORTE0,1 SHARED TO OSCI&OSCO)
(2) Port A, Port D1,PortD2:I/O Buffers
(3) Port B, C and PortD0: Input Buffers
(4) R1 = 0 is possible, but the REM specification is revised to reduce power consumption
(5) Since PORTD.0 is input only,PORTB or PORTC can be scanned out to detect PORTD.0 option.



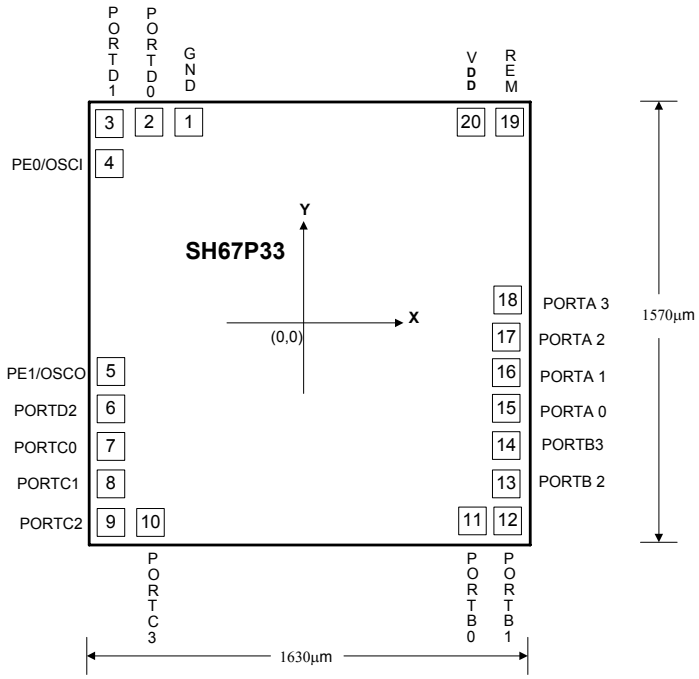
AP2:

Remote Control (81 Keys)

(1) Oscillator: BUILD-IN RC
(2) Port A, Port D1,PortD2,Port E: I/O Buffers
(3) Port B, C and PortD0: Input Buffers


SH67P33
VDD
GND
R1
REM
PE1/OSCO
PE0/OSCI
PORTD.2
PORTD.1
PORTD.0
PORTC.3
PORTC.2
PORTC.1
PORTC.0
PORTB.3
PORTB.2
PORTB.1
PORTB.0
PORTA.3
PORTA.2
PORTA.1
PORTA.0
=
VDD

Bonding Diagram



Substrate connects to GND.

SH67P33 unit: μm

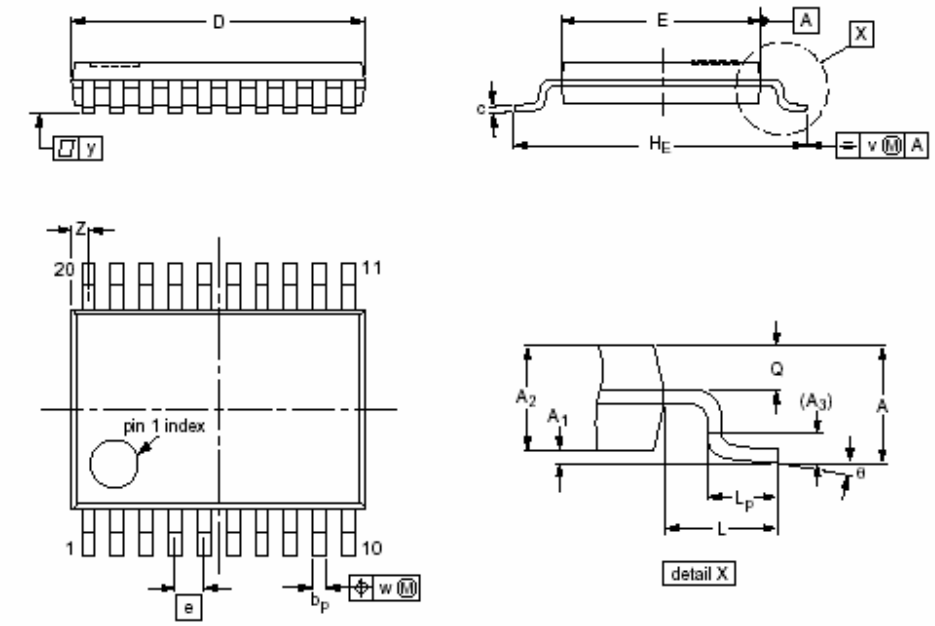
Pad No	Designation	X	Y
1	GND	-484.00	712.50
2	PORTD[0]	-602.00	712.50
3	PORTD[1]	-722.00	712.50
4	PORTE[0]	-733.00	562.05
5	PORTE[1]	-728.00	-180.65
6	PORTD[2]	-745.00	-322.50
7	PORTC[0]	-745.00	-437.50
8	PORTC[1]	-745.00	-552.50
9	PORTC[2]	-734.00	-707.50
10	PORTC[3]	-614.00	-707.50
11	PORTB[0]	614.00	-707.50
12	PORTB[1]	734.00	-707.50
13	PORTB[2]	745.00	-552.50
14	PORTB[3]	745.00	-432.50
15	PORTA[0]	745.00	-312.50
16	PORTA[1]	745.00	-192.50
17	PORTA[2]	745.00	-72.50
18	PORTA[3]	745.00	67.50
19	REM	733.00	700.50
20	VDD	618.00	700.50

Ordering Information

Part No.	Package
SH67P33H	CHIP FORM
SH67P33X	20L TSSOP
SH67P33	20L DIP
SH67P33M	20L SOP

Package Informations

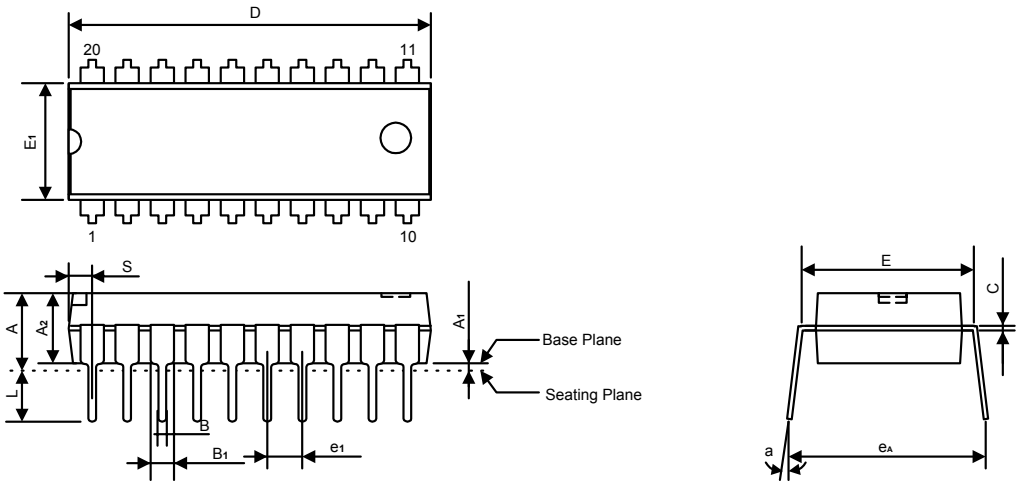
TSSOP 20L Outline Dimensions unit: inches/mm



Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.1	---	---	0.044
A1	0.05	---	0.15	0.002	---	0.006
A2	0.80	---	0.95	0.032	---	0.038
A3	---	0.25	---	---	0.01	---
bp	0.19	---	0.30	0.008	---	0.012
c	0.1	---	0.2	0.004	---	0.008
D(1)	6.4	---	6.6	0.256	---	0.264
E(2)	4.3	---	4.5	0.172	---	0.18
e	---	0.65	---	---	0.026	---
HE	6.2	---	6.6	0.248	---	0.264
L	---	1	---	---	0.04	---
Lp	0.5	---	0.75	0.02	---	0.03
Q	0.3	---	0.4	0.012	---	0.016
v	---	0.2	---	---	0.008	---
w	---	0.13	---	---	0.005	---
y	---	0.1	---	---	0.004	---
Z(1)	0.2	---	0.5	0.008	---	0.02
θ	0°	---	8°	0°	---	8°

Notes:
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

DIP 20L Outline Dimensions unit: inches/mm

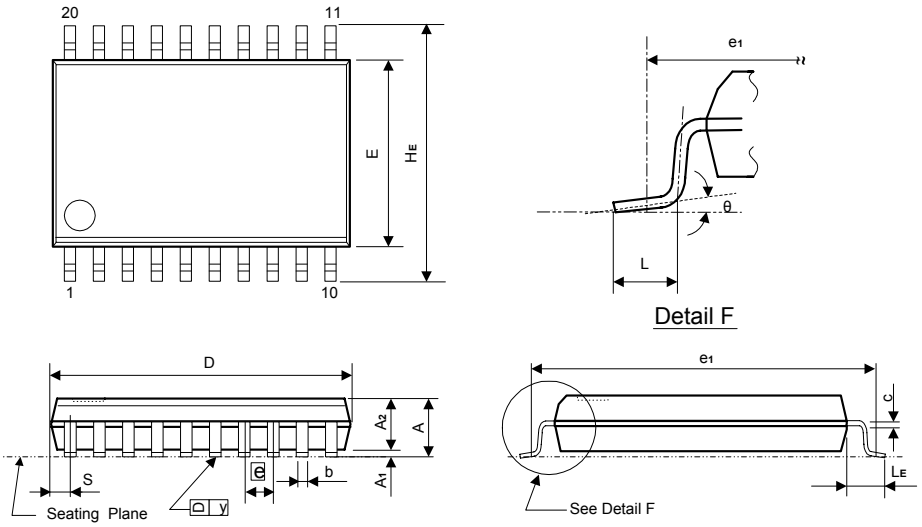


Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.010	3.30 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.026 Typ. (1.046 Max.)	26.06 Typ. (26.57 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.078 Max.	1.98 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash

SOP 20L (W.B.) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.106 Max.	2.69 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.500 ± 0.02	12.80 ± 0.51
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.50 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.032 ± 0.008	0.81 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.042 Max.	1.07 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch. Designer reference only.
4. Dimension S includes end flash.

Specification Revision History

Version	Content	Date
0.2	1. Add bonding diagram 2. Add pad location 3. Add application circuit 4. Add package informations	May.2003
0.1	Original	Jan. 2003