SH93P423

Caller ID Controller with CAS Detector and One-Time PROM(OTP)

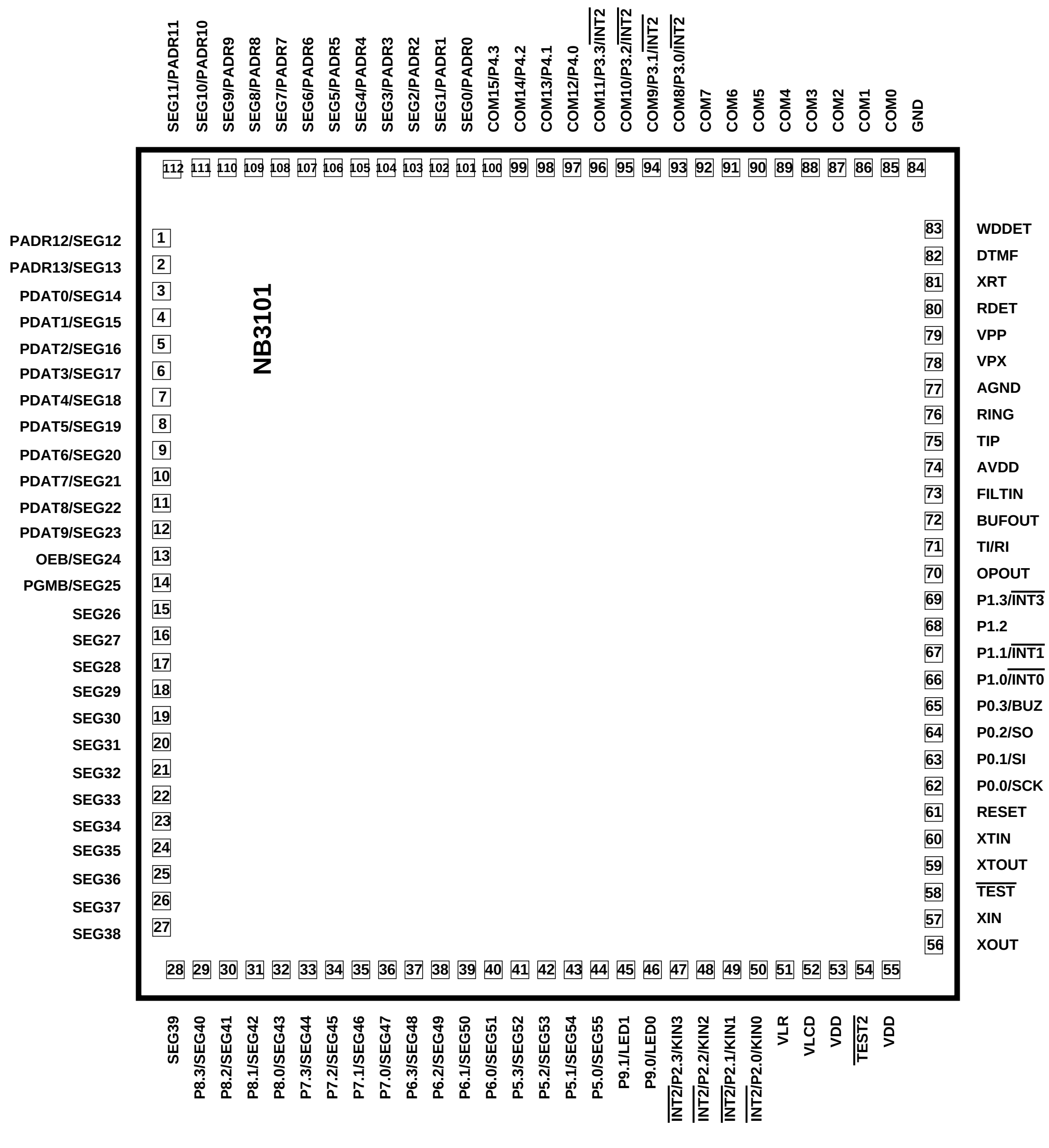
Features

- Memory
  - One-time PROM: 16K x 10 bits
    Includes:
      Program code
      Character/Graphic pattern
  - RAM: 6K x 4 bits
    Includes:
      RAM mapped control registers
      Memory registers
      Stack
      LCD memory
      Data memory
- CPE Alerting Signal (CAS) Detector
  - Compatible with the Bellcore SR-TSV-002476 TYPE II specification
- Subroutine nesting
  - 16-level subroutine nesting
- LCD Controller/Driver
  - 16 commons x 56 segments
  - Duty option: 1/8, 1/16
  - Bias option: 1/4, 1/5
  - 16-level contrast control
  - External contrast control
- Ring detector
  - Built-in ring detector
- FSK demodulator
  - Compatible with Bell 202 and ITU-T V.23
- Keyboard
  - 32 x 4 keys maximum
- Battery-low detection
  - 4-level detection for battery-low
- I/O Pins with per pin definition
  - 2 LED driver pins
  - 12 general I/O pins
  - 8 I/O pins shared with LCD common pins
  - 16 I/O pins shared with LCD segment pins
- DTMF Generator
  - Built-in low distortion DTMF generator
- Interrupts
  - 12 interrupts are available
- Beeper
  - 4 options of frequency for each CPU speed
- Timers/Counters
  - One Watch dog Timer
  - One 8-bit Watch Timer/Counter (driven by a standard 32.768KHz crystal oscillator)
  - One 8-bit programmable Timer/Counter with external clock option
  - One 8-bit programmable Timer
  - One 12-bit programmable Timer
- Communication port
  - 1 high speed serial I/O port
- Power-down modes
  - Stop mode (CPU stop with main oscillator off)
  - Halt mode (CPU stop with main oscillator on)
- Dual Oscillators System
  - Main oscillator frequency (Fmain): 3.579545MHz crystal/ceramic oscillator
  - Watch oscillator frequency (Fwatch): 32.768KHz crystal oscillator
- Instruction Execution Time
  - 1.1μs, 2.2μs or 4.4μs (Fmain = 3.58MHz)
- Power System
  - Operating voltage range:
    For CPU: 2.8V to 5.5V
    For FSK demodulator: 3.5V to 5.5V
    For CAS detector: 3.5 V to 5.5 V
  - CPU Standby current: 3μA typical for 3V

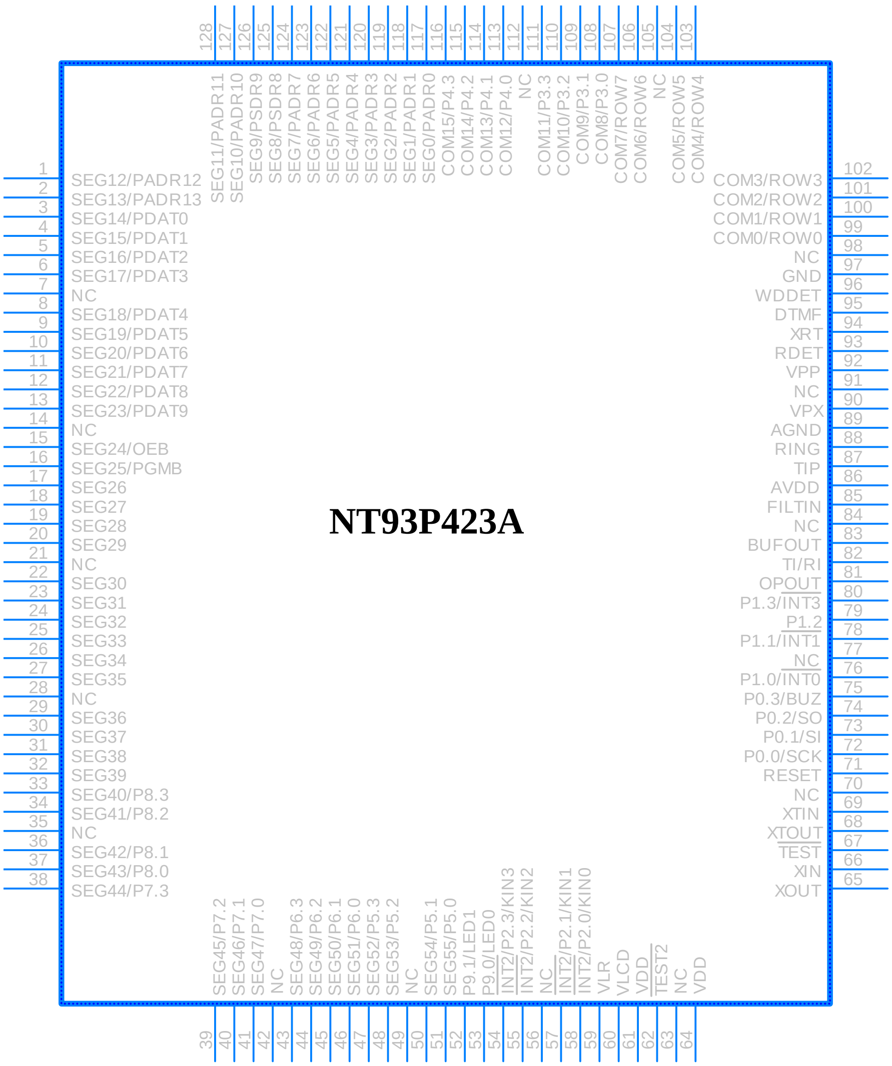
General Description

This chip is a single-chip OTP type CMOS 4-bit micro-controller that dedicates to serve the telephone calling identification. To achieve the best performance, it is integrated with one real time clock, two 8-bit timers, one 12-bit Timer, one watch dog timer, one serial I/O, CAS detector, FSK demodulator, Ring detector, DTMF generator and 16 x 56 LCD driver. Up to 36 pins of this chip can be specified as a general I/O. The built-in DTMF generator can provide the call back service. Twelve interrupt vectors provide rapid response to internal and external events. Ring detected circuit can work even in STOP mode. Furthermore, it also offers two power consumption modes (STOP and HALT) for energy saving in idle condition.

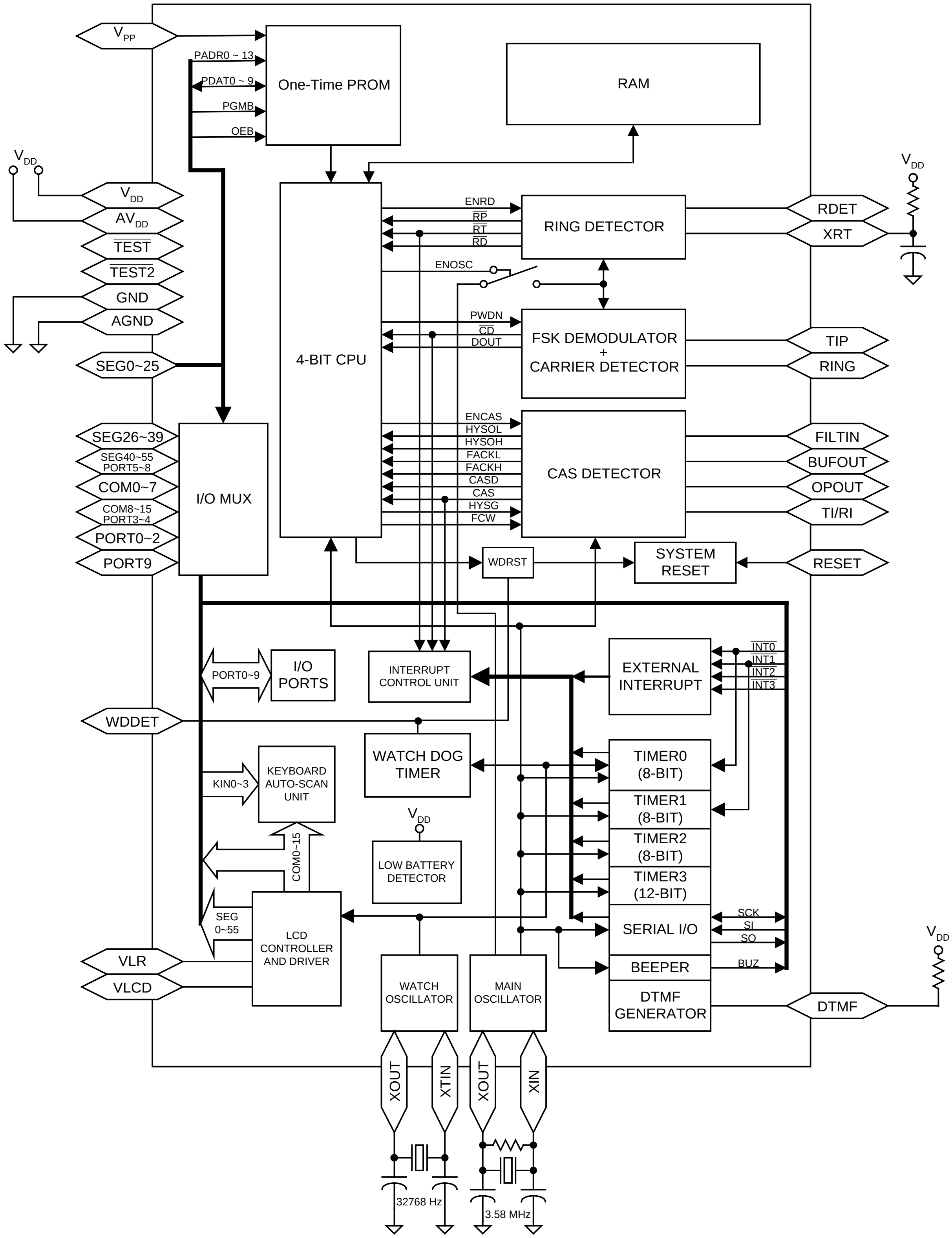
Pad Configuration



Pin Configuration



Block Diagram



Pad Description

Pad No.	Designation	I/O	Description
1 ~ 2	SEG12~13 / PADR12~13	O I	LCD segment signal outputs / Address bus for OTP ROM
3 ~ 12	SEG14~23 / PDAT0~9	O I/O	LCD segment signal outputs / Data bus for OTP ROM
13	SEG24 / OEB	O I	LCD segment signal output / OTP data output enable for verify
14	SEG25 / PGMB	O I	LCD segment signal output / OTP programming enable
15 ~ 28	SEG26~SEG39	O	LCD segment signal outputs
29 ~ 32	SEG40~43 / P8.3~0	O I/O	LCD segment signal outputs / Port8
33 ~ 36	SEG44~47 / P7.3~0	O I/O	LCD segment signal outputs / Port7
37 ~ 40	SEG48~51 / P6.3~0	O I/O	LCD segment signal outputs / Port6
41 ~ 44	SEG52~55 / P5.3~0	O I/O	LCD segment signal outputs / Port5
45 ~ 46	LED1, LED0 / P9.1, P9.0	O	LED driving pins / Port9, These pins are N-channel open drain output.
47 ~ 50	KIN3~0 ($\overline{\text{INT2}}$)/ P2.3~0	I I/O	Keyboard interrupt inputs ($\overline{\text{INT2}}$) / Port2
51	VLR	O	Output pin for LCD reference voltage
52	VLCD	I	Input pin for LCD reference voltage
53	VDD	P	Power supply input. Should be decoupled to GND by a capacitor mounted close to the device pin
54	$\overline{\text{TEST2}}$	I	Enable TEST MODE 2 when low (For factory used only)
55	VDD	P	This pad should be connected to VDD.
56	XOUT	O	Main oscillator output
57	XIN	I	Main oscillator input
58	$\overline{\text{TEST}}$	I	Enable TEST MODE 1 when low (For factory used only)
59	XTOUT	O	Watch crystal oscillator output
60	XTIN	I	Watch crystal oscillator input
61	RESET	I	System reset input (High active)
62	SCK / P0.0	I/O I/O	Serial clock I/O / Port0.0
63	SI / P0.1	I I/O	Serial data input / Port0.1

Pad Configuration (Continued)

Pad No.	Designation	I/O	Description
64	SO / P0.2	O I/O	Serial data output / Port0.2
65	BUZ / P0.3	O I/O	Buzzer output (Normal low) / Port0.3
66	$\overline{\text{INT0}}$ / P1.0	I I/O	External interrupt inputs ($\overline{\text{INT0}}$) / Port1.0
67	$\overline{\text{INT1}}$ / P1.1	I I/O	External interrupt inputs ($\overline{\text{INT1}}$) / Port1.1
68	P1.2	I/O	Port1.2
69	$\overline{\text{INT3}}$ / P1.3	I I/O	External interrupt input ($\overline{\text{INT3}}$) / Port1.3
70	OPOUT	O	Output of TI/RI input OP Amp
71	TI/RI	I	Tip in or Ring in should be connected with twisted pair
72	BUFOUT	O	Internal buffer output
73	FILTIN	I	Band pass filter input
74	AVDD	P	Analog power supply input. Should be decoupled to AGND by a capacitor mounted close to the device pin
75	TIP	I	TIP line input pin
76	RING	I	RING line input pin
77	AGND	P	Analog ground
78	VPX	P	OTP programming power
79	VPP	P	OTP programming power
80	RDET	I	Ring detected input pin
81	XRT	O	Ring detected output pin (open drain, low active)
82	DTMF	O	DTMF signal output pin
83	WDDET	I/O	Output: watch dog status detecting pin Input: disable watch dog timer while low
84	GND	P	Ground
85 ~ 92	COM0-7	O	LCD common signal outputs (Keyboard scanning outputs)
93 ~ 96	COM8~11 / P3.0~3 / $\overline{\text{INT2}}$	O I/O I	LCD common signal outputs / Port3 / Keyboard interrupt inputs ($\overline{\text{INT2}}$)
97 ~ 100	COM12~15 / P4.0~3	O I/O	LCD common signal outputs / Port4
101 ~ 112	SEG0~11 PADR0~11	O I	LCD segment signal outputs / Address bus for OTP ROM

Note: All external interrupt inputs would be triggered by any negative-edge signal

Absolute Maximum Ratings

Power Supply Voltage . . . . -0.5V to 6.0V
Input Voltage . . . . -0.5V to VDD+0.5V
Output Voltage . . . . -0.5V to VDD+0.5V
Power Dissipation 0.05W
Operating Temperature . . . . 0°C to 70°C
Storage Temperature . . . . -55°C to 135°C

Comments

Stresses above those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these of any other conditions above specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Temperature = 0°C to 70°C, VDD = 5.0V±10%, GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Supply voltage	V_{CPU}	2.8		5.5	V	For all mode with FSK & CAS off	
	V_{FSK}	3.5		5.5	V	For all mode with FSK on, CAS off	
	V_{CAS}	3.5		5.5	V	For all mode with FSK off, CAS on	
Operating current	I_{DD1}		1.5	2.5	mA	V_{DD} = 5V	Normal mode FSK off, DTMF off CAS off
	I_{DD2}		0.7	1.5	mA	V_{DD} = 3V	
	I_{DD3}		I_{DD1} + 1.6	I_{DD1} + 2.5	mA	V_{DD} = 5V	Normal mode FSK on, DTMF off CAS off
	I_{DD4}		I_{DD1} + 0.45	I_{DD1} + 1.0	mA	V_{DD} = 5V	Normal mode FSK off, DTMF on CAS off
	I_{DD5}		I_{DD1} + 1.6	I_{DD1} + 2.5	mA	V_{DD} = 5V	Normal mode FSK off, DTMF off CAS on
Standby current	I_{SB1}		600	900	μA	V_{DD} = 5V	Halt mode FSK off, DTMF off LCD off, CAS off
	I_{SB2}		12	30	μA	V_{DD} = 5V	Stop mode FSK off, DTMF off LCD off, CAS off
	I_{SB3}		3	20	μA	V_{DD} = 3V	
Input high voltage	V_{IH1}	0.9 V_{DD}		V_{DD} +0.3	V	RESET	
	V_{IH2}	V_{DD} –0.3		V_{DD} +0.3	V	XIN, XTIN	
	V_{IH3}	0.8 V_{DD}		V_{DD} +0.3	V	All pins except RESET, XIN & XTIN	
Input low voltage	V_{IL1}	–0.3		0.1 V_{DD}	V	RESET	
	V_{IL2}	–0.3		0.3	V	XIN, XTIN	
	V_{IL3}	–0.3		0.2 V_{DD}	V	All pins except RESET, XIN & XTIN	
Output high voltage	V_{OH}	V_{DD} –1.0			V	Output pin without loading	
Output low voltage	V_{OL}			0.6	V	Output pin without loading	
Drive/Sink current of general output pins	I_{OH1}	1.5	2.0		mA	V_{OH} = 4.0V, V_{OL} = 0.6V Port0, Port1 and Port2	
	I_{OL1}	–1.5	–2.0		mA		
Drive/Sink current of general output pins	I_{OH2}	1.0	2.0		mA	V_{OH} = 4.0V, V_{OL} = 0.6V Port3 and Port4	
	I_{OL2}	–1.5	–2.0		mA		

DC Electrical Characteristics (Temperature = 0°C to 70°C, VDD = 5.0V±10%, GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drive/Sink current of shared output pins	I_{OH3}	1.0	1.5		mA	V_{OH} = 4.0V, V_{OL} = 0.6V Port5, Port6, Port7 and Port8
	I_{OL3}	–1.0	–1.5		mA	
Sink current of Port 9	I_{OL3}		–5		mA	V_{OL} = 0.6V
Pull-up resistance 1	R_{UP1}		180		KΩ	Port0, Port1, Port3 & Port4
Pull-up resistance 2	R_{UP2}		50		KΩ	Port2
Pull-up resistance 3	R_{UP3}		100		KΩ	Port5, Port6, Port7 & Port8

OTP DC Electrical Characteristics (Temperature = 0°C to 70°C, VPP = 10.5V±10%, VDD = 5.0V±10%,GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
OTP programming voltage	V_{PP}		10.5		V	
Programming current	I_{PP}			30	mA	
Input high voltage	V_{IPH}	0.8 V_{DD}		V_{DD} +0.3	V	PADR0 ~ 13, PDAT 0 ~9, PGMB, OEB
Input low voltage	V_{IPL}	–0.3		0.2 V_{DD}	V	PADR0 ~ 13, PDAT 0 ~9, PGMB, OEB
Output high voltage	V_{OPH}	V_{DD} –1.0			V	PDAT 0 ~9, without loading
Output low voltage	V_{OPL}			0.6	V	PDAT 0 ~9, without loading

Analog Electrical Characteristics (Temperature = 0°C to 70°C, V_{DD} = 5.0V±10%, GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Single Row Tone Output Amplitude	V_{OR}	500	580	650	mVp-p	With 100KΩ pull-up resister
Single Column Tone Output Amplitude	V_{OC}	685	760	835	mVp-p	With 100KΩ pull-up resister
DTMF output distortion	DIS%		2	5	%	With 100KΩ pull-up resister
DTMF pre-emphasis	Twist	1	2	3	dB	With 100KΩ pull-up resister
Tip/Ring input impedance	R_{IN}	400	500	600	KΩ	Input frequency = 0
Input sensitivity of Tip and Ring	P_{SIG}	-45	–42		dBm	SNR = 15dB
Hysteresis of Carrier detected	H_{CD}		3		dB	SNR = 15dB
Frequency response of the Band Pass Filter of FSK demodulator			–54 0 +1 –19 –35		dB	≤ 60Hz 1200Hz 2200Hz 5000Hz ≥ 10000Hz
Battery detected level	V_{BAT}	V_{DET} –0.3		V_{DET}+0.3	V	V_{DET} = 2.8V or 3.6V or 4.4V

Analog Electrical Characteristics (Temperature = 0°C to 70°C, V_{DD} = 5.0V±10%, GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input sensitivity		-36	-32		dBm	
Frequency response of the Band Pass Filter of CAS detector (frequency 2130 Hz @ 0 dBm)			–30 –1 –1 –30		dB	1930Hz 2115Hz 2160Hz ≥ 2440Hz
Frequency response of the Band Pass Filter of CAS detector (frequency 2750 Hz @ 0 dBm)			–30 –1 –1 –30		dB	2450Hz 2725Hz 2780Hz ≥ 3000Hz

AC Electrical Characteristics (Temperature = 0°C to 70°C, V_{DD} = 5.0V±10%, GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Execution cycle time	T_{CYC}	1.1		4.4	μs	Fmain = 3.58MHz
Hardware Reset duration	T_{RES}	2			T_{CYC}	Fmain = 3.58MHz
CPU start up time from Reset or STOP	T_{CPU}		2.5	10	ms	Fmain = 3.58MHz By crystal oscillator
FSK power up time before data in	T_{PUD}		8	20	ms	P_{SIG} = -40dBm, SNR = 30dB
$\overline{CD}$ delay time	T_{CDD}		7	20	ms	P_{SIG} = -40dBm, SNR = 30dB
$\overline{CD}$ hold time	T_{CDH}		9	20	ms	P_{SIG} = -40dBm, SNR = 30dB
Main oscillator frequency	Fmain		3.579545		MHz	Crystal or Ceramic oscillator
Watch oscillator frequency	Fwatch		32.768		KHz	Crystal oscillator
Watch oscillator start up time	T_{WS}			1	sec	
Serial clock cycle time	T_{SP}	250			ns	
Serial output data delay time	T_{SD}			120	ns	
Serial input data set up time	T_{SS}	35			ns	
Serial input data hold time	T_{SH}	75			ns	
Filter output valid signal delay	Tfd1		6	10	ms	
Filter output invalid signal delay	Tfd2		6	10	ms	
Frequency counter of 2130 Hz valid delay time	Tdl1	1.9		15	ms	
Frequency counter of 2130 Hz invalid delay time	Tdl2	0		1.4	ms	
Frequency counter of 2750 Hz valid delay time	Tdh1	1.5		12	ms	
Frequency counter of 2750 Hz invalid delay time	Tdh2	0		1.1	ms	
Debonucing time of valid signal	Tdb1		16		ms	
Debouncing time of invalid signal	Tdb2		8		ms	

OTP AC Electrical Characteristics (Temperature = 0°C to 70°C, V_{DD} = 5.0V±10%, GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{DD} setup time	T_{VDS}	2			μs	
Address setup time	T_{AS}	2			μs	
Data setup time	T_{DS}	2			μs	
Data hold time	T_{DH}	2			μs	
Programming time	T_{PG}	100	120		μs	
OEB setup time	T_{OES}	3			μs	
Data output enable delay time	T_{OED}	1			μs	
Data output disable delay time	T_{ODD}			200	ns	
Verify time	T_{VF}	2			μs	
Address hold time	T_{AHD}	1			μs	

Functional Description

Program memory

This 4-bit CPU can directly access up to 16K words of one-time programmable (OTP) memory. Most instruction (except RET & RETI) would complete its operation in one or two execution cycle(s). For instruction RET or RETI, it takes 3 execution cycles to complete the operation of returning from a subroutine.

Vector address area ($0000 to $001F)

This chip provides a vector address area for program initialization and interrupt services. They are:

$00~01	Jump to RESET (initialization) routine
$02~03	Jump to $\overline{\text{INT0}}$ service routine
$04~05	Jump to $\overline{\text{INT1}}$ service routine
$06~07	Jump to $\overline{\text{INT2}}$ service routine
$08~09	Jump to $\overline{\text{INT3}}$ service routine
$0A~0B	Jump to $\overline{\text{TIMER0}}$ service routine
$0C~0D	Jump to $\overline{\text{TIMER1}}$ service routine
$0E~0F	Jump to $\overline{\text{TIMER2}}$ service routine
$10~11	Jump to $\overline{\text{TIMER3}}$ service routine
$12~13	Jump to Serial I/O service routine
$14~15	Jump to Ring detected service routine or CAS tone detected service routine
$16~17	Jump to Carrier detected service routine
$18~1F	Reserved

Random Access Data Memory

Resident data memory is organized as 6K x 4 bits (6144 nibbles). RAM is used for data storage, register storage, stack, and storage of segment data for LCD display RAM. All the interrupt control registers and other special function registers are implemented by means of memory mapping to the internal RAM space.

RAM Addressing

Like most CPU structure, data may be accessed either by direct or indirect addressing. Direct addressing is defined by operand itself while indirect addressing is defined by the four registers, BANK, V, X and Y. Indirect addressing is more general than direct addressing because only the first 1K data can be accessed by means of direct addressing while the others have no limitation for this. There are 16 special RAM spaces (R0 to R15) that can be accessed directly either by special instruction or the general one.

RAM Mapping

This chip employs memory-mapped registers for controlling the system function and on-chip peripherals, such as Interrupts, I/O port, LCD control and Timers. All the control bits and data are defined from address $000 through $03F in data memory.

OTP ROM MAP

Address	Area
$0000 – $001F	Vector Address Area
$0020 – $003F	Zero-page Subroutines
$0040 – $3FFF	System Program

RAM MAP

Address	Area
$000	RAM Mapped Register
$040	Memory Register (R0~15)
$050	Data
$100	LCD Display Area
$200	Stack
$240 – $17FF	Data

RAM Mapped Register

Register		Contents					
Addr	Name	Description	Bit3	Bit2	Bit1	Bit0	Attribute
$000	SENSE0	Sense register 0	IE0 (s/r/t)	IRQ0 (r/t)	RSP (r)	IE (s/r/t)	-
$001	SENSE1	Sense register 1	IE2 (s/r/t)	IRQ2 (r/t)	IE1 (s/r/t)	IRQ1 (r/t)	-
$002	SENSE2	Sense register 2	IET1 (s/r/t)	IRQT1 (r/t)	IET0 (s/r/t)	IRQT0 (r/t)	-
$003	SENSE3	Sense register 3	IET2 (s/r/t)	IRQT2 (r/t)	IESI (s/r/t)	IRQSI (r/t)	-
$004	TMOD0	Timer 0 mode register	TMOD0.3	TMOD0.2	TMOD0.1	TMOD0.0	W
	OVF0	Overflow counter of Timer 0	OVF0.3	OVF0.2	OVF0.1	OVF0.0	R
$005	TMOD1	Timer 1 mode register	TMOD1.3	TMOD1.2	TMOD1.1	TMOD1.0	W
$006	TC00	Timer 0 counter register 0	TC00.3	TC00.2	TC00.1	TC00.0	R
	TL00	Timer 0 load register 0	TL00.3	TL00.2	TL00.1	TL00.0	W
$007	TC01	Timer 0 counter register 1	TC01.3	TC01.2	TC01.1	TC01.0	R
	TL01	Timer 0 load register 1	TL01.3	TL01.2	TL01.1	TL01.0	W
$008	TC10	Timer 1 counter register 0	TC10.3	TC10.2	TC10.1	TC10.0	R
	TL10	Timer 1 load register 0	TL10.3	TL10.2	TL10.1	TL10.0	W
$009	TC11	Timer 1 counter register 1	TC11.3	TC11.2	TC11.1	TC11.0	R
	TL11	Timer 1 load register 1	TL11.3	TL11.2	TL11.1	TL11.0	W
$00A	SIOL	Serial data low register	SIOL.3	SIOL.2	SIOL.1	SIOL.0	R/W/t
$00B	SIOH	Serial data high register	SIOH.3	SIOH.2	SIOH.1	SIOH.0	R/W/t
$00C	SIOM	Serial mode register	SIOM.3	SIOM.2	SIOM.1	SIOM.0	R/W
$00D	CKS	System clock register	WDRST (r)	ENOSC (W) {Must be set to 1}	CKS.1 (W)	CKS.0 (W)	-
$00E	BPM	Beep mode register	BPM.3	BPM.2	BPM.1	BPM.0	W
$00F	TESTM	Test mode register	CONFIDENTIAL				W
$010	PMODA	Port mode register A	PMODA.3	PMODA.2	PMODA.1	PMODA.0	W/s
$011	PMODB	Port mode register B	PMODB.3	PMODB.2	PMODB.1	PMODB.0	W/s
$012	PMODC	Port mode register C	PMODC.3	PMODC.2	PMODC.1	PMODC.0	W/s
$013	TMOD3	Timer 3 mode register	TMOD3.3	TMOD3.2	TMOD3.1	TMOD3.0	W
$014	PMODE	Port mode register E	PMODE.3	PMODE.2	PMODE.1	PMODE.0	W
$015	PMODF	Port mode register F	PMODF.3	PMODF.2	PMODF.1	PMODF.0	W
$016	-	Reserved for EV-chip	-	-	-	-	-
$017	LCON	LCD control register	LCON.3	LCON.2	LCON.1	LCON.0	W/s/r
$018	LMOD0	LCD mode register 0	LMOD0.3	LMOD0.2	LMOD0.1	LMOD0.0	W
$019	LMOD1	LCD mode register 1	LMOD1.3	LMOD1.2	LMOD1.1	LMOD1.0	W
$01A	TGC	Tone control register	Reserved	TGC.2	TGC.1	TGC.0	W
$01B	TGD	Tone Data register	TGD.3	TGD.2	TGD.1	TGD.0	W

RAM Mapped Register (continued)

Register		Contents					
Addr	**Name**	**Description**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Attribute**
$01C	TC30	Timer 3 counter register 0	TC30.3	TC30.2	TC30.1	TC30.0	R
	TL30	Timer 3 load register 0	TL30.3	TL30.2	TL30.1	TL30.0	W
$01D	TC31	Timer 3 counter register 1	TC31.3	TC31.2	TC31.1	TC31.0	R
	TL31	Timer 3 load register 1	TL31.3	TL31.2	TL31.1	TL31.0	W
$01E	TC32	Timer 3 counter register 2	TC32.3	TC32.2	TC32.1	TC32.0	R
	TL32	Timer 3 load register 2	TL32.3	TL32.2	TL32.1	TL32.0	W
$01F	CTL0	Control register 0	KPRS (R/t)	ENBAT (W/t)	KPAD (W/t)	KRVS (W/t)	-
			KB2 (W/s/r)	-	-	-	-
$020	SPA	Stack pointer register A	Reserved	SP.12	SP.11	SP.10	R/W/t
$021	SPB	Stack pointer register B	SP.9	SP.8	SP.7	SP.6	R/W/t
$022	SPC	Stack pointer register C	SP.5	SP.4	SP.3	SP.2	R/t
$023	SENSE4	Sense register 4	IECD (s/r/t)	IRQCD (r/t)	IET3 (s/r/t)	IRQT3 (r/t)	-
$024	SENSE5	Sense register 5	IERT/ IECAS (s/r/t)	IRQRT/ IRQCAS (r/t)	IE3 (s/r/t)	IRQ3 (r/t)	-
$025	TMOD2	Timer 2 mode register	TMOD2.3	TMOD2.2	TMOD2.1	TMOD2.0	W
$026	TC20	Timer 2 counter register 0	TC20.3	TC20.2	TC20.1	TC20.0	R
	TL20	Timer 2 load register 0	TL20.3	TL20.2	TL20.1	TL20.0	W
$027	TC21	Timer 2 counter register 1	TC21.3	TC21.2	TC21.1	TC21.0	R
	TL21	Timer 2 load register 1	TL21.3	TL21.2	TL21.1	TL21.0	W
$028	KREG0	Keypad register 0	KREG0.3	KREG0.2	KREG0.1	KREG0.0	R/W/t
$029	KREG1	Keypad register 1	KREG1.3	KREG1.2	KREG1.1	KREG1.0	R/W/t
$02A	KREG2	Keypad register 2	KREG2.3	KREG2.2	KREG2.1	KREG2.0	R/W/t
$02B	KREG3	Keypad register 3	KREG3.3	KREG3.2	KREG3.1	KREG3.0	R/W/t
$02C	KREG4	Keypad register 4	KREG4.3	KREG4.2	KREG4.1	KREG4.0	R/W/t
$02D	KREG5	Keypad register 5	KREG5.3	KREG5.2	KREG5.1	KREG5.0	R/W/t
$02E	KREG6	Keypad register 6	KREG6.3	KREG6.2	KREG6.1	KREG6.0	R/W/t
$02F	KREG7	Keypad register 7	KREG7.3	KREG7.2	KREG7.1	KREG7.0	R/W/t
$030	P0	Port 0	P0.3	P0.2	P0.1	P0.0	R/W/s/r/t
$031	P1	Port 1	P1.3	P1.2	P1.1	P1.0	R/W/s/r/t
$032	P2	Port 2	P2.3	P2.2	P2.1	P2.0	R/W/s/r/t
$033	P3	Port 3	P3.3	P3.2	P3.1	P3.0	R/W/s/r/t
$034	P4	Port 4	P4.3	P4.2	P4.1	P4.0	R/W/s/r/t

RAM Mapped Register (continued)

Register		Contents					
Addr	**Name**	**Description**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Attribute**
$035	P5	Port 5	P5.3	P5.2	P5.1	P5.0	R/W/s/r/t
$036	P6	Port 6	P6.3	P6.2	P6.1	P6.0	R/W/s/r/t
$037	P7	Port 7	P7.3	P7.2	P7.1	P7.0	R/W/s/r/t
$038	P8	Port 8	P8.3	P8.2	P8.1	P8.0	R/W/s/r/t
$039	P9	Port 9	FACKH (t)	FACKL (t)	P9.1 (W/s/r/t)	P9.0 (W/s/r/t)	-
$03A	CTL1	Control register 1	-	BANK (s/r/t)	HYSG (s)	FCW (s)	-
$03B	-	Reserved for EV-chip	-	-	-	-	-
$03C	CTL2	Control register 2	$\overline{\text{RT}}$	$\overline{\text{RD}}$	$\overline{\text{CD}}$	DOUT	R/t
$03D	CTL3	Control register 3	RP	BAT.2	BAT.1	BAT.0	R/t
			ENCAS	PWDN	ENRD	BEEP	W
$03E	CASR	CAS register	HYSOH	HYSOL	CAS	CASD	R/t
	CVAR	Contrast control register	CVAR.3	CVAR.2	CVAR.1	CVAR.0	W
$03F	DBUF	Data buffer	DBUF.3	DBUF.2	DBUF.1	DBUF.0	R/W

Notes

- R/W/s/r/t:
  - R: Available for all nibble-read instructions, for example, MTA
  - W: Available for all nibble-write instructions, for example, ITMD
  - s: Available for instructions, SM and SMD
  - r: Available for instructions, RM and RMD
  - t: Available for instructions, TM and TMD
- IE: Enable all Interrupts of this chip
- IEn: Enable Interrupt n, IRQn: Interrupt request of INTn
- IETn: Enable Interrupt of Timer n, IRQTn: Interrupt request of Timer n
- IESI: Enable Interrupt of Serial interface, IRQSI: Interrupt request of Serial interface
- IECD: Enable Interrupt of Carrier detected, IRQCD: Interrupt request of Carrier detected
- IERT: Enable Interrupt of Ring time detected, IRQRT: Interrupt request of Ring time detected
- IECAS: Enable Interrupt of CAS tone detected, IRQCAS: Interrupt request of CAS tone detected
- SP.y: Bit y of stack pointer, RSP: Reset stack pointer address
- OVF0: Increase 1 while Timer 0 up counter has been overflowed (counter value from $FF to $00). It will be reset by H/W after reading. Default value is 0
- WDRST: Reset watch-dog timer
- ENOSC: Enable the clock for FSK demodulator and frequency counter (within the Ring Detector) when set (It must be set to one during initialization if FSK demodulator has to be used in case!)
- CKS: Clock selection register
  CKS.0 and CKS.1 are used to select the system clock speed,
  e.g. If CKS = xx00, then system clock = Fmain/16
  If CKS = xx01, then system clock = Fmain/8
  If CKS = xx10, then system clock = Fmain/4
- KB2: Enable 2nd page of keypad registers for keyboard scanning COM8 ~ COM15
- KPRS: It would be set when any key is pressed
- ENBAT: Enable low-battery detection when high
- KPAD: Enable Key pressed detection
- KRVS: Reverse Keyboard scanning signal
- FACKH: 2750 Hz acknowledge output
- FACKL: 2130 Hz acknowledge output
- P9.0, P9.1: Output pins only

- $\overline{\text{RT}}$: Bit for indicates Ring time pulse status
- $\overline{\text{RD}}$: Bit for indicates Ring detected status
- CD: Bit for indicates Carrier detected status
- DOUT: FSK demodulator output data bit
- BANK: Select the 1st bank of RAM: $000h~ $FFFh while reset BANK, or
  Select the 2nd bank of RAM: $1000h ~ $17FFh while set BANK.
- RP: Bit for indicates Ring pulse signal
- BAT.m: Battery power level data (Please refer to the Battery-low table)
- ENCAS: Enable CAS tone detection when set
- PWDN: Turn off the FSK demodulator when set
- ENRD: Enable Internal Ring detector
- BEEP: Enable Beeper
- HYSOH: Hysteresis comparator output of 2750 Hz
- HYSOL: Hysteresis comparator output of 2130 Hz
- CASD: CAS tone detected output after de-bouncing time
- CAS: CAS tone detected output before de-bouncing time
- CVAR: Contrast control register (Write-only)
- DBUF.n: Data buffer for Port I/O modes setting except Port1 and Port4; Also see the following description of FCW and HYSG for the usage of DBUF

  For example:
  ```
  ITMD   :0100,PMODA     ;set PORT0 & PORT3 as I/P; PORT2 as O/P
  ```
  If users want to set only one port I/O mode, the following example is available
  ```
  ITMD   :0101,DBUF      ;0 as I/P; 1 as O/P
  SMD    0,PMODA         ;set PORT0.0 & 0.2 as O/P; PORT0.1 & 0.3 as I/P
  ```
- FCW: Control register for 2130/2750 Hz frequency counter length and detection window width control register

Frequency Counter Control Register

Bit3	Bit2	Bit1	Bit0	Counter Length	Fmax (Hz)	Fmin (Hz)	dFmax/Fo	dFmin/Fo
0	0	0	0	32	2151.49	2107.77	1.01%	-1.04%
0	1	0	0	32	2140.55	2119.01	0.50%	-0.51%
1	0	0	0	32	2135.76	2124.67	0.27%	-0.25%
1	1	0	0	32	2133.21	2127.51	0.15%	-0.12%
0	0	0	1	16	2173.04	2085.66	2.02%	-2.07%
0	1	0	1	16	2150.84	2107.77	0.98%	-1.04%
1	0	0	1	16	2141.19	2119.01	0.53%	-0.51%
1	1	0	1	16	2136.08	2124.67	0.29%	-0.25%
0	0	1	0	8	2217.47	2042.81	4.11%	-4.07%
0	1	1	0	8	2171.72	2085.66	1.96%	-2.07%
1	0	1	0	8	2152.13	2107.77	1.04%	-1.04%
1	1	1	0	8	2141.83	2119.01	0.56%	-0.51%
0	0	1	1	4	2312.02	1962.17	8.55%	-7.84%
0	1	1	1	4	2214.73	2042.81	3.98%	-4.07%
1	0	1	1	4	2174.36	2085.66	2.08%	-2.07%
1	1	1	1	4	2153.43	2107.77	1.10%	-1.04%

- Fo = 2130 Hz

Frequency Counter Control Register

Bit3	Bit2	Bit1	Bit0	Counter Length	Fmax (Hz)	Fmin (Hz)	dFmax/Fo	dFmin/Fo
0	0	0	0	32	2778.73	2721.67	1.04%	-1.02%
0	1	0	0	32	2764.24	2736.24	0.52%	-0.50%
1	0	0	0	32	2760.51	2744.63	0.38%	-0.19%
1	1	0	0	32	2756.79	2748.85	0.25%	-0.04%
0	0	0	1	16	2804.86	2690.98	1.99%	-2.14%
0	1	0	1	16	2775.49	2719.6	0.93%	-1.10%
1	0	0	1	16	2767.98	2736.24	0.65%	-0.50%
1	1	0	1	16	2760.51	2744.63	0.38%	-0.19%
0	0	1	0	8	2858.63	2631.62	3.95%	-4.28%
0	1	1	0	8	2798.28	2686.94	1.76%	-2.28%
1	0	1	0	8	2783.05	2719.6	1.20%	-1.10%
1	1	1	0	8	2767.98	2736.24	0.65%	-0.50%
0	0	1	1	4	2972.59	2520.42	8.09%	-8.31%
0	1	1	1	4	2844.99	2623.9	3.45%	-4.56%
1	0	1	1	4	2813.68	2686.94	2.32%	-2.28%
1	1	1	1	4	2783.05	2719.6	1.20%	-1.10%

☞ Fo = 2750 Hz

DBUF: Data buffer for frequency counter length and detection window width
For example: ITMD :xxxx,DBUF
SMD 0,FCW

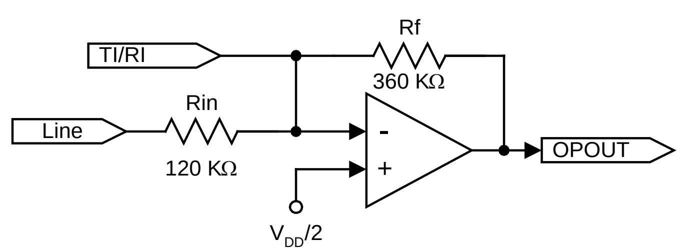
☞ HYSG: Minimum gain control register for the input signal of 2130/2750 Hz hysteresis comparator

Gain Control Register

Bit3	Bit2	Bit1	Bit0	Function
		0	0	Minimum Gain = -36 dBm of 2130 Hz/2750 Hz
		0	1	Minimum Gain = -32 dBm of 2130 Hz/2750 Hz
		1	0	Minimum Gain = -14 dBm of 2130 Hz/2750 Hz
		1	1	Minimum Gain = -10 dBm of 2130 Hz/2750 Hz

DBUF: Data buffer for gain value
For example: ITMD :xxxx,DBUF
SMD 1,HYSG

☸ Note: CAS Line Gain (Rf/Rin) = 3



☞ (m = 0, 1, 2; n = 0, 1, 2, 3; x = 0,1; y = 2, ... , 12)

Registers and Flags

This chip provides nine registers and two flags for CPU operation. They are described below:

Accumulator A (4 bits) and Register B (4 bits)

Accumulator A and Register B are 4-bit registers that hold the result of the arithmetic logic units (ALU). They are the very basic registers for a CPU to execute all the arithmetic calculation, logic operation and data transfer among memories, I/Os and registers.

Register V (4 bits)

Register V is a 4-bit register that holds the page address (256 addresses per page) of RAM.

Register X (4 bits), Register Y (4 bits)

Register X and Y register are used for indirect RAM addressing such that the RAM address is defined as the following format:

Bit location	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM address	BANK	V3	V2	V1	V0	X3	X2	X1	X0	Y3	Y2	Y1	Y0

Note: Select the 1st bank of RAM: $000h~ $FFFh while reset BANK, or
Select the 2nd bank of RAM: $1000h ~ $17FFh while set BANK.

Register EX (4 bits), Register EY (4 bits)

Register EX and EY are 4-bit registers available to assist register X and Y, respectively.

Carry Flag, CY (1 bit)

The carry flag holds the ALU overflow bit generated by arithmetic operation. It can be set or reset by instruction directly, and is affected by the rotation instruction.

Status Flag, SF (1 bit)

The flag holds ALU compare, arithmetic instruction and the status of accumulator. This flag would be tested by those instructions of conditional jump and conditional call. After the execution of BR, LBR, CAL, or CALL instruction, the status bit would be set. Furthermore, SF will be pushed onto the stack during serving interrupt. Note that SF will not be restored by instruction RET, but instruction RETI.

Program Counter, PC (14 bits)

The program counter is used for addressing ROM data. It is reserved in the RAM space from $200 to $23F, so that 16 program addresses can be restored for subroutine call function or interrupt service.

Stack Pointer, SP (13 bits)

The stack pointer is implemented by a typical RAM mapped structure so as to make the system become more flexible. SP is an 13-bit register that holds the start address of the recent level of Stack. Stack is combined of sixteen 4-nibble registers, which hold the return address with its status flag and carry flag. Therefore, 16-level stack operation is possible. And yet it can be initialized to the starting address ($23F) of the stack by either system reset or software method.
The following table shows how the stack register configured:

Reset Stack Pointer Flag, RSP (1bit)

RSP is used for resetting the stack pointer to $23F and it will be cleared while system RESET. In general, it would not be used unless software reset of stack pointer is necessary for extraordinary condition. The stack pointer can be reset to $23F by reset RSP through instruction RM/RMD.

Stack Register Bits Configuration: (For level 1)

Address	Bit 3		Bit 2		Bit 1		Bit 0	
$23F	S3	-PC3	S2	-PC2	S1	-PC1	S0	-PC0
$23E	S7	CY	S6	-PC6	S5	-PC5	S4	-PC4
$23D	S11	-PC10	S10	-PC9	S9	-PC8	S8	-PC7
$23C	S15	SF	S14	-PC13	S13	-PC12	S12	-PC11

Note: PC stored in the stack is a negative value.

Memory Allocation of Stack Level

Level	Address	Level	Address	Level	Address	Level	Address
16	$203 ~ $200	12	$213 ~ $210	8	$223 ~ $220	4	$233 ~ $230
15	$207 ~ $204	11	$217 ~ $214	7	$227 ~ $224	3	$237 ~ $234
14	$20B ~ $208	10	$21B ~ $218	6	$22B ~ $228	2	$23B ~ $238
13	$20F ~ $20C	9	$21F ~ $21C	5	$22F ~ $22C	1	$23F ~ $23C

Interrupts

There are twelve interrupts with one system initialization:

1. System initialization:
   - RESET (Reset pin)
2. General interrupts:
   - $\overline{INT0}$ (Interrupt from pin P1.0)
   - $\overline{INT1}$ (Interrupt from pin P1.1)
   - $\overline{INT2}$ (Interrupt from pin Port2 / Port3)
   - $\overline{INT3}$ (Interrupt from pin P1.3)
3. Timer interrupts:
   - $\overline{TIMER0}$ (Interrupt from pin Timer 0)
   - $\overline{TIMER1}$ (Interrupt from pin Timer 1)
   - $\overline{TIMER2}$ (Interrupt from pin Timer 2)
   - $\overline{TIMER3}$ (Interrupt from pin Timer 3)
4. Serial communication port interrupt:
   - SERIAL (interrupt from Serial COM port)
5. Ring detected interrupt:
   - $\overline{RT}$ (interrupt from Ring detector)
6. Carrier detected interrupt:
   - $\overline{CD}$ (interrupt from FSK demodulator)
7. CAS tone detected interrupt:
   - CAS (interrupt from CAS tone detector)

Interrupt Control bits and Request flags

The RAM mapped register from $00 through $03, $23 and $24 can only be accessed by bit operation instructions. Any interrupt (such as $\overline{INTn}$) may be accepted while IE and its own enable flag (such as IEn) were set. The interrupt request flag (such as IRQn) will only be set by its interrupt signal (a negative-edge signal). Yet this request flag can be cleared by system RESET or software.

Interrupt Enabled (IE)

The interrupt-enable bit, IE, enables all interrupt requests when it is set. Also, it can be enabled by instruction RETI and will be reset during entering the interrupt service routine automatically. Once the program enters the interrupt service routine, IE will be reset by CPU itself so that other interrupt (if any) would be pending with its execution priority. That is the reason why only one level of interrupt service can be performed in general. However, multi-level interrupt service can be achieved by setting IE within the interrupt service routine. For multi-level interrupt programming, please refer to the Timing diagram of interrupt events.

Actually, it is the gate for all interrupt requests. No interrupt service would be done until IE is set.

Any two different interrupts occurred in the same instruction cycle would be treated as collision of interrupt when IE=1. The interrupt service with higher priority will come first while the other is pending.

Any two different interrupts occurred whatever in the same or different instruction cycle would also be treated as collision of interrupt when IE=0. Both interrupts would be pending until IE is set. Once IE is set, the interrupt service with higher priority will come first while the other is pending.

Individual Interrupt Enabled (IEn, IETn, IESI, IECD)

The interrupt-enable bit (such as IEn) enables a specific interrupt request (such as IRQn) when it is set. In other words, it is the gate for its own interrupt request only.

General Interrupts

$\overline{INT0}$, $\overline{INT1}$:

Interrupt request flag, IRQ0/IRQ1, will be set while interrupt input, $\overline{INT0}$ / $\overline{INT1}$, has received any negative edge signal. The program will enter the service routine of $\overline{INT0}$ / $\overline{INT1}$ provided that both IE and IE0/IE1 were set. Also, $\overline{INT0}$ or $\overline{INT1}$ (P1.0 or P1.1) can be programmed as an external clock input of Timer0 or Timer1 by the register, TMOD0 or TMOD1, respectively.

$\overline{INT2}$:

Interrupt request flag, IRQ2, will be set while any one of the interrupt inputs, $\overline{INT2}$ (Port2.0-3/Port3.0-3), has received a negative edge signal. Generally, it is used as a keyboard interrupt. Port3 can not be used as interrupt when 1/16 duty of LCD has been selected.

$\overline{INT3}$:

Interrupt request flag, IRQ3, will be set while interrupt input $\overline{INT3}$ has received any negative edge signal.

Timer Interrupts

Interrupt request flag, IRQTn, will be set by the output signal of Timer n (n = 0, 1, 2, 3). Details should be referred to the section of Timer.

Serial communication port interrupt

Interrupt request flag, IRQSI, will be set by the internal serial interface signal. Details should be referred to the section of Serial Communication port.

Ring detected interrupt

Interrupt request flag, IRQRT, will be set by the internal signal from Ring detector provided that Ring detector has been enabled (ENRD = 1). Details should be referred to the section of Ring detector.

Carrier detected interrupt

Interrupt request flag, IRQCD, will be set in NORMAL mode by the internal signal from Carrier detector provided that FSK demodulator has been turned on (PWDN = 0 & ENOSC = 1). Note that it does not work in STOP mode.

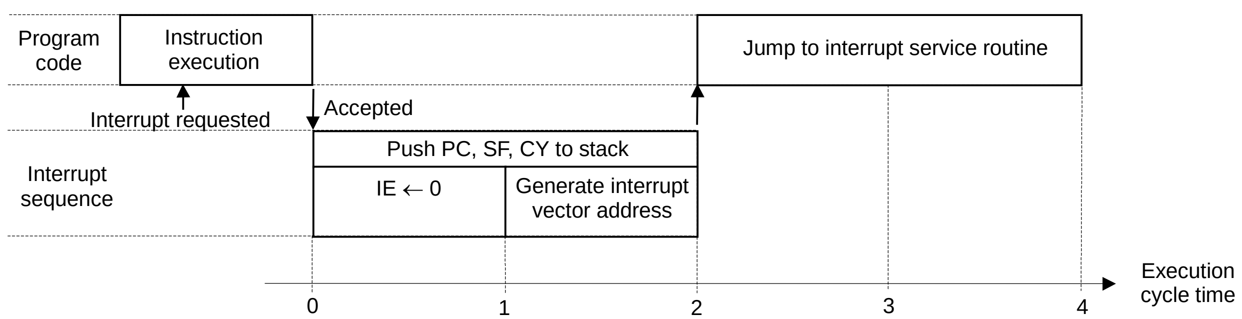
CAS tone detected interrupt

Interrupt request flag, IRQCAS, will be set by the internal signal from CAS detector provided that CAS detector has been enabled (ENCAS = 1). Details should be referred to the section of Built-in CAS detector.

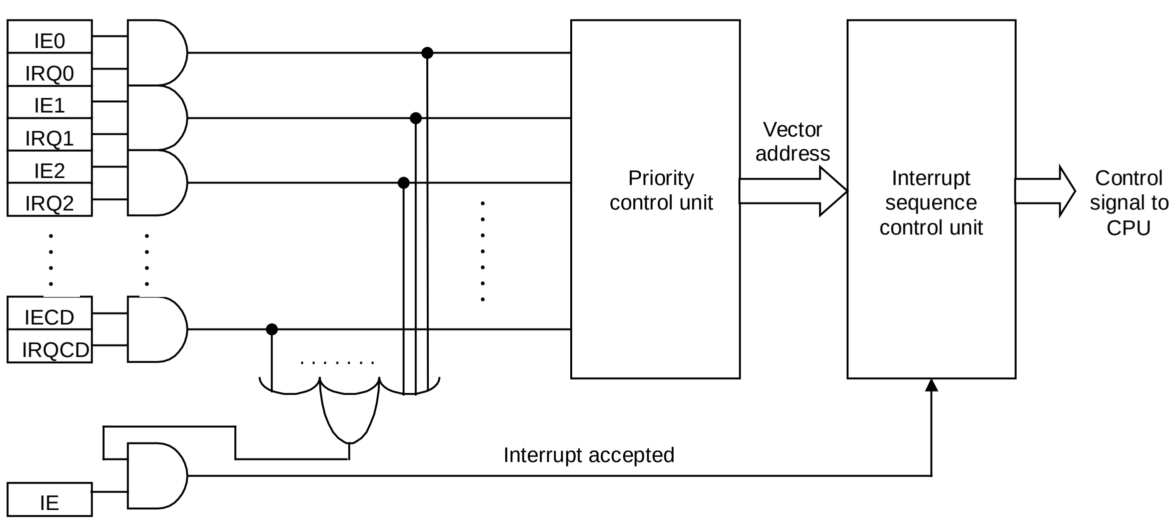
Interrupt Vector Address and execution priority

Interrupt	Signal	Priority	Issued by	Condition	Vector
RESET	External	1st	Reset pin	RESET PIN = 1 for at least 2 instruction cycles	$00
$\overline{INT0}$	External	2nd	IRQ0	IE = IE0 = IRQ0 = 1	$02
$\overline{INT1}$	External	3rd	IRQ1	IE = IE1 = IRQ1 = 1	$04
$\overline{INT2}$	External	4th	IRQ2	IE = IE2 = IRQ2 = 1	$06
$\overline{INT3}$	External	5th	IRQ3	IE = IE3 = IRQ3 = 1	$08
$\overline{TIMER0}$	Internal	6th	IRQT0	IE = IET0 = IRQT0 = 1	$0A
$\overline{TIMER1}$	Internal	7th	IRQT1	IE = IET1 = IRQT1 = 1	$0C
$\overline{TIMER2}$	Internal	8th	IRQT2	IE = IET2 = IRQT2 = 1	$0E
$\overline{TIMER3}$	Internal	9th	IRQT3	IE = IET3 = IRQT3 = 1	$10
SERIAL	Internal	10th	IRQSI	IE = IESI = IRQSI = 1	$12
$\overline{RT}$/CAS	Internal	11th	IRQRT/IRQCAS	IE = IERT = IECAS = ENRD = ENCAS = 1	$14
CD	Internal	12th	IRQCD	IE = IECD = ENOSC = 1 & PWDN = 0	$16

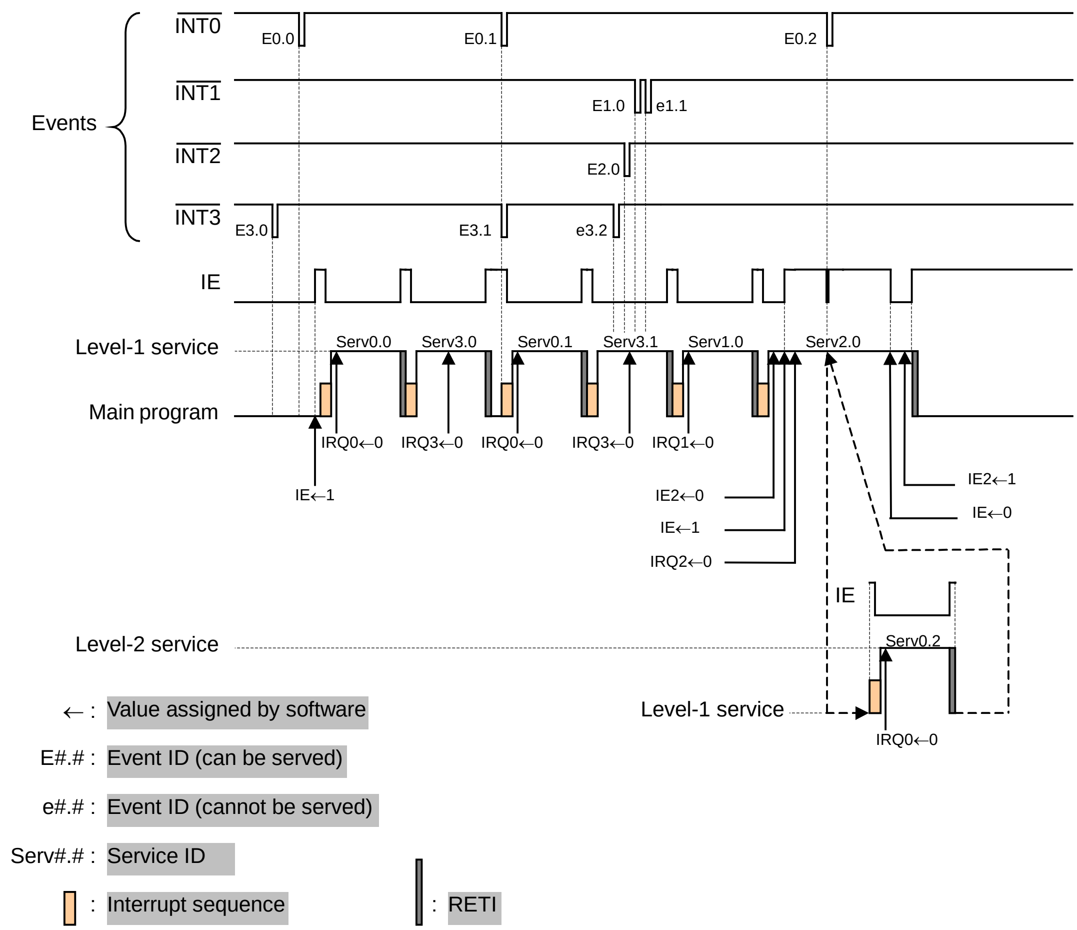
Timing of interrupt sequence



Hardware structure of interrupt control unit



Example of Timing of interrupt events



Input/Output Port

There are 36 I/O pins, which are divided into 9 groups. Each I/O pin contains a pull-up resistor that can be controlled by software. The pull-up resistor will be enabled if it is configured as an input pin with a data '1'. For example, the pull-up resistor of P0.3 would be enabled by the following procedure:

```
ITMD  :1110, PMODA          ;set P0 as I/P port
ITMD  :1000, P0        ;enable pull-up resistor of P0.3
```

Do not let any unconnected pin floating because it may cause the large current problem to the chip.
All the I/O pins would be reset to the default status (input with pull-up resistor enabled) after system reset.
In case there is an internal pull-up resistor of input pin have been disabled, an external pull-up/pull-down resistor (100 KΩ typically) must be connected.

Port Mode Register	Bit 3	Bit 2	Bit 1	Bit 0	Mode	
PMODA ($010)	PORT3	PORT2	Reserved	PORT0	0: Input	1: Output
PMODB ($011)	PORT7	PORT6	PORT5	Reserved	0: Input	1: Output
PMODC ($012)	Reserved	Reserved	Reserved	PORT8	0: Input	1: Output
PMODE ($014)	PORT1.3	PORT1.2	PORT1.1	PORT1.0	0: Input	1: Output
PMODF ($015)	PORT4.3	PORT4.2	PORT4.1	PORT4.0	0: Input	1: Output

Serial Interface

The serial interface is basically an 8-bit Half-duplex Serial Transmitter/Receiver, which consists of two data registers (SIOL, SIOH), one serial mode register (SIOM) and an internal octal counter. During execution of STS instruction, the octal counter would be reset first and then it will increment by one at the rising edge of the transfer clock (SCK). However, the octal counter would be reset and the serial interrupt flag will also be set after the eighth transfer clocks (SCK) has been sent or the octal counter has been reset during transferring data.
Note that Port0 must be set up as an input port before the serial interface function is enabled.

Serial Data Register (SIOL($00A), SIOH($00B))

This 8-bit read/write serial data register consists of a lower nibble (SIOL) and an upper nibble (SIOH). The data stored in serial data register can be shifted out through the SO pin. Similarly, the external data stream can be shifted in and stored in SIOL & SIOH via SI pin. The output bit stream is synchronized by the falling edge of the transfer clock (SCK) while the input bit stream will be extracted by the rising edge of SCK. Read/write operation of the serial data register must be performed after completion of data transfer. Otherwise, the data cannot be guaranteed.

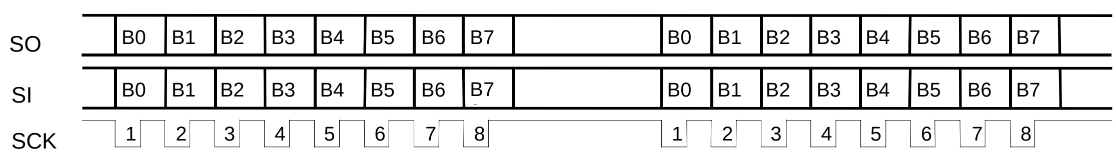
Serial Mode Register (SIOM ($00C))

It is a 4-bit write-only register, which determines what the speed or the source of transferring clock (SCK) is. It may be reset by RESET instruction. Be ware that writing data to SIOM will initialize the data transfer operation whatever it is being data transfer or not. It means that the transfer clock will stop, octal counter will be reset to zero. During data transferring, serial interrupt request (IRQSI) will also be set after writing SIOM. Furthermore, data transferring will not be start up until the STS instruction has been executed. Note that PMODA.0 must be reset, and do not let any input pin (SI, SCK-input or P0.3) floating (Internal or external pull-up resistor can be utilized).

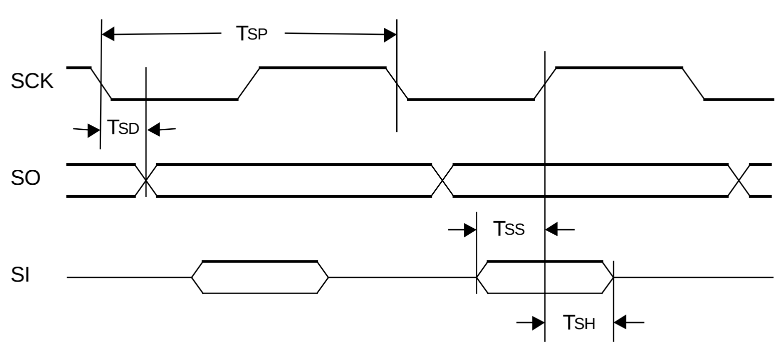
Serial Mode Register (SIOM, $00C) (PMODA.0 = 0) (FCYC = 1/TCYC = Fmain/4 or Fmain/8 or Fmain/16)

SIOM.3	SIOM.2	SIOM.1	SIOM.0	SCK	Clock Source	Serial I/O	P0.0~2
0	X	X	X	-	-	Disabled	Enabled
1	0	0	0	Input	External Clock	Enabled	Disabled
1	0	0	1	Output	FCYC	Enabled	Disabled
1	0	1	0	Output	FCYC / 4	Enabled	Disabled
1	0	1	1	Output	FCYC / 16	Enabled	Disabled
1	1	0	0	Output	FCYC / 64	Enabled	Disabled
1	1	0	1	Output	FCYC / 256	Enabled	Disabled
1	1	1	0	Output	FCYC / 1024	Enabled	Disabled
1	1	1	1	Output	FCYC / 4096	Enabled	Disabled

Serial Data Format



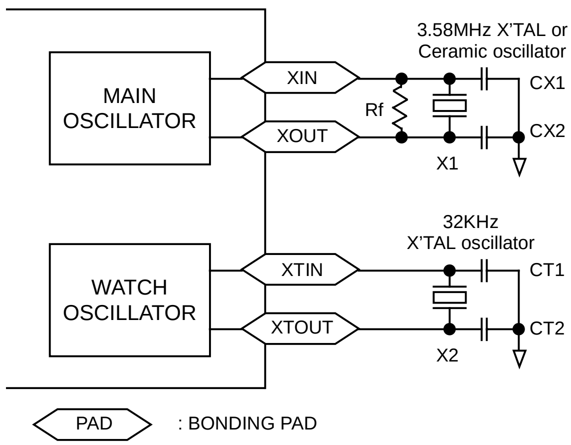
Timing of Serial Data Transfer



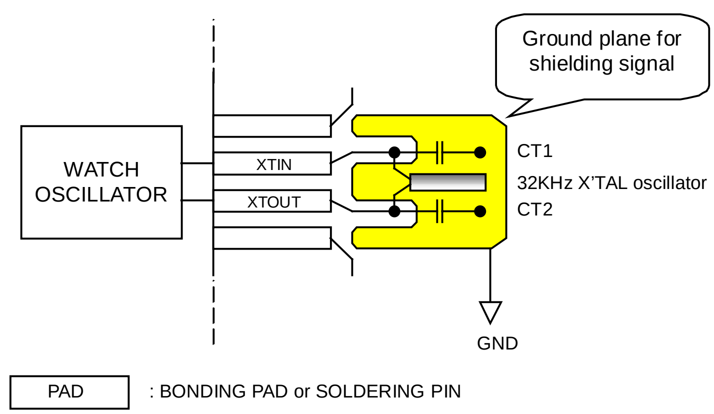
Oscillators

This is a typical dual oscillator system such that low power idle state with real time clock can be guaranteed even if the CPU has been stopped. Also, a simple RC delay circuit that co-operates with an I/O pin, the Timer0 and suitable software routine can give out a practical Watch-dog Timer.
As shown in the following figure, the main oscillation circuit should be connected to an external crystal or ceramic oscillator. To ensure that these two oscillators can work well, a feedback resistor and 4 auxiliary capacitors should be employed. The recommendation for the value of these components is:

Component	RANGE	RECOMMENDED
Rf	1MΩ~5MΩ	1MΩ
CX1	22pF~30pF	22pF
CX2	22pF~30pF	22pF
CT1	22pF~30pF	22pF
CT2	22pF~30pF	22pF



To ensure the oscillation quality of the real time clock, there is a recommendation for the PC board layout that can be help for improving the noise immunity. In addition, any micro-strip that cross over the oscillation signal would cause unexpected high-frequency noise to the watch oscillator. As shown in the following figure, the oscillation signal is easily be shielded by such simple ground plane for one-layer or two-layer design. Similarly, this method can be applied for the main oscillator in some noisy environment.



Timers

There are 4 Timers (Timer 0~3), in which prescaler and clock selection circuits have been built. By programming timer mode registers TMOD0~TMOD3, different clock source and speed can be selected. Yet Timer 0 can be set up as a real time clock for the watch oscillator would never stop after power up.

1) Operation of Timer 0: *8-bit Watch Timer*

Timer 0 is an 8-bit timer, which consists of two 4-bit write-only timer load registers (TL00, TL01) and two 4-bit read-only counter registers (TC00, TC01). Besides the internal clock source, Fmain, an external clock source, $\overline{INT0}$, is also provided.

To write this load register, the lower nibble, TL00, must be written first, then the upper nibble, TL01.

To read the data of this counter register, the upper nibble, TC01, must be read out first, then the lower nibble, TC00.

The order of data reading and writing must be followed otherwise unexpected counting may be occurred.

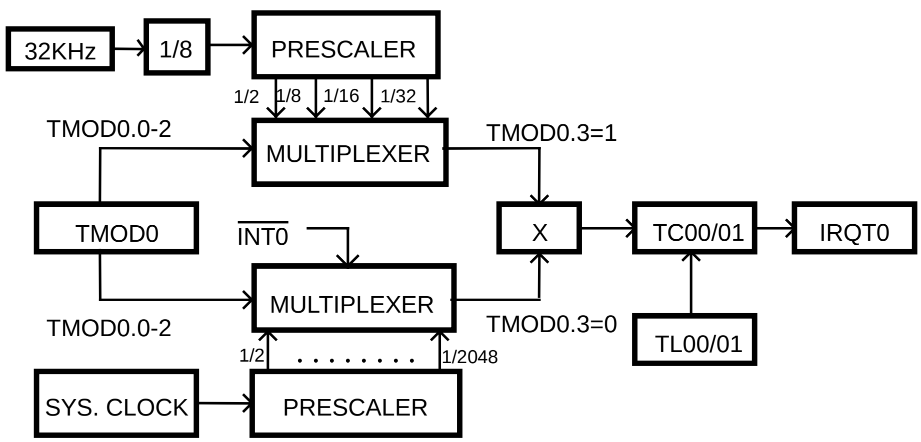
There are three kinds of clock source can be selected by controlling the timer mode register 0 (TMOD0, $004):

- The first one is the system clock, which can be programmed to Fmain/4, Fmain/8 or Fmain/16 by writing 00, 01 or 10 to CKS.1-0 respectively.
- The second one is the standard watch oscillator, 32768Hz.
- The Last one is the external source, $\overline{INT0}$.

Interrupt request flag (IRQT0) will be set when its 8-bit up counter has been overflowed (IRQT0 will be set during the transition from $FF, the counter value, to $00).

For the clock speed value, please refer the following table.

Timer 0 Block Diagram



Timer Mode 0 Register (TMOD0, $004) (FCYC = 1/TCYC = Fmain/4 or Fmain/8 or Fmain/16)

TMOD0.3	TMOD0.2	TMOD0.1	TMOD0.0	Clock speed	Clock Source
0	0	0	0	FCYC / 2048	Main oscillator
0	0	0	1	FCYC / 512	Main oscillator
0	0	1	0	FCYC / 128	Main oscillator
0	0	1	1	FCYC / 32	Main oscillator
0	1	0	0	FCYC / 8	Main oscillator
0	1	0	1	FCYC / 4	Main oscillator
0	1	1	0	FCYC / 2	Main oscillator
0	1	1	1	-	External source, $\overline{INT0}$
1	0	0	0	32768Hz / 256	Watch oscillator
1	0	0	1	32768Hz / 128	Watch oscillator
1	0	1	0	32768Hz / 64	Watch oscillator
1	0	1	1	32768Hz / 16	Watch oscillator
1	1	X	X	-	Reserved

2) Operation of Timer 1: *8-bit Timer*

Auto-reload function has been implemented in Timer 1. User can select different clock speed with or without auto-reload by putting the appropriate value into the timer mode register 1, TMOD1. Besides the internal clock source, Fmain, an external clock source, $\overline{\text{INT1}}$, is also provided.

To write this load register, the lower nibble, TL10, must be written first, then the upper nibble, TL11.

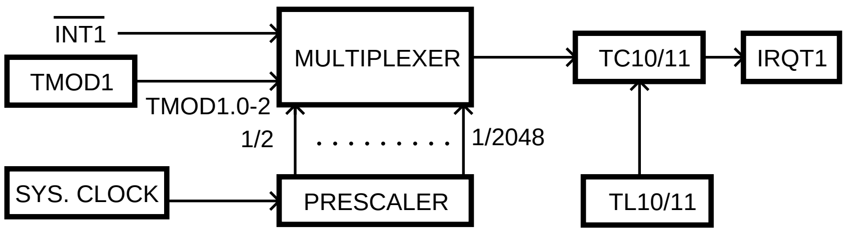
To read the data of this counter register, the upper nibble, TC11, must be read out first, then the lower nibble, TC10.

The order of data reading and writing must be followed otherwise unexpected counting may be occurred.

Interrupt request flag (IRQT1) will be set when its 8-bit up counter has been overflowed (IRQT1 will be set during the transition from $FF, the counter value, to $00).

For the clock speed value, please refer the following table.

Timer 1 Block Diagram



Timer Mode Register 1: (TMOD1 $005) (FCYC = 1/TCYC = Fmain/4 or Fmain/8 or Fmain/16)

TMOD1.3	TMOD1.2	TMOD1.1	TMOD1.0	Clock speed	Clock Source	Auto-Reload
0	0	0	0	FCYC / 2048	Main oscillator	No
0	0	0	1	FCYC / 1024	Main oscillator	No
0	0	1	0	FCYC / 512	Main oscillator	No
0	0	1	1	FCYC / 32	Main oscillator	No
0	1	0	0	FCYC / 16	Main oscillator	No
0	1	0	1	FCYC / 8	Main oscillator	No
0	1	1	0	FCYC / 2	Main oscillator	No
0	1	1	1	-	External, $\overline{\text{INT1}}$	No
1	0	0	0	FCYC / 2048	Main oscillator	Yes
1	0	0	1	FCYC / 1024	Main oscillator	Yes
1	0	1	0	FCYC / 512	Main oscillator	Yes
1	0	1	1	FCYC / 32	Main oscillator	Yes
1	1	0	0	FCYC / 16	Main oscillator	Yes
1	1	0	1	FCYC / 8	Main oscillator	Yes
1	1	1	0	FCYC / 2	Main oscillator	Yes
1	1	1	1	-	External, $\overline{\text{INT1}}$	Yes

3) Operation of Timer 2: *8-bit Timer*

Auto-reload function has been implemented in Timer 2. User can select different clock speed with or without auto-reload by putting the appropriate value into the timer mode register 2, TMOD2.

Only the internal clock source, Fmain, is provided for Timer 2.

To write this load register, the lower nibble, TL20, must be written first, then the upper nibble, TL21.

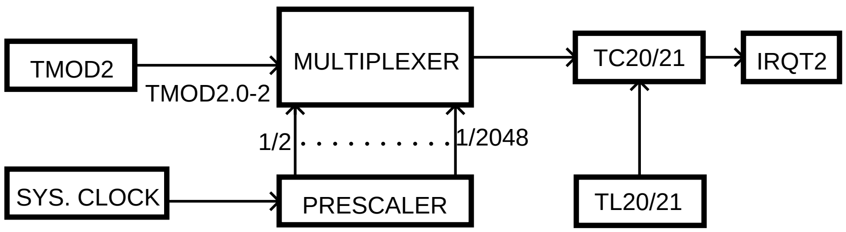
To read the data of this counter register, the upper nibble, TC21, must be read out first, then the lower nibble, TC20.

The order of data reading and writing must be followed otherwise unexpected counting may be occurred.

Interrupt request flag (IRQT2) will be set when its 8-bit up counter has been overflowed (IRQT2 will be set during the transition from $FF, the counter value, to $00).

For the clock speed value, please refer the following table.

Timer 2 Block Diagram



Timer Mode Register 2: (TMOD2 $0025) (FCYC = 1/TCYC = Fmain/4 or Fmain/8 or Fmain/16)

TMOD2.3	TMOD2.2	TMOD2.1	TMOD2.0	Clock speed	Clock Source	Auto-Reload
0	0	0	0	FCYC / 2048	Main oscillator	No
0	0	0	1	FCYC / 1024	Main oscillator	No
0	0	1	0	FCYC / 512	Main oscillator	No
0	0	1	1	FCYC / 128	Main oscillator	No
0	1	0	0	FCYC / 32	Main oscillator	No
0	1	0	1	FCYC / 16	Main oscillator	No
0	1	1	0	FCYC / 8	Main oscillator	No
0	1	1	1	FCYC / 2	Main oscillator	No
1	0	0	0	FCYC / 2048	Main oscillator	Yes
1	0	0	1	FCYC / 1024	Main oscillator	Yes
1	0	1	0	FCYC / 512	Main oscillator	Yes
1	0	1	1	FCYC / 128	Main oscillator	Yes
1	1	0	0	FCYC / 32	Main oscillator	Yes
1	1	0	1	FCYC / 16	Main oscillator	Yes
1	1	1	0	FCYC / 8	Main oscillator	Yes
1	1	1	1	FCYC / 2	Main oscillator	Yes

4) Operation of Timer 3: *12-bit Timer*

Auto-reload function has also been implemented in Timer 3. User can select different clock speed with or without auto-reload by putting the appropriate value into the timer mode register 3, TMOD3.

Only the internal clock source, Fmain, is provided for Timer 3.

To write this load register, the lower nibble, TL30, must be written first, then the middle nibble, TL31, and finally the upper nibble, TL32.

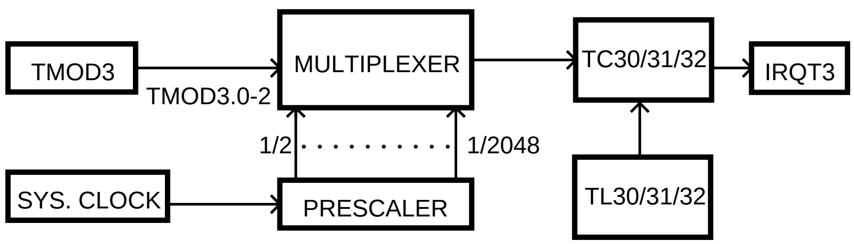
To read the data of this counter register, the upper nibble, TC32, must be read out first, then the TC31, and finally the TC30.

The order of data reading and writing must be followed otherwise unexpected counting may be occurred.

Interrupt request flag (IRQT3) will be set when its 12-bit up counter has been overflowed (IRQT3 will be set during the transition from $FFF, the counter value, to $000).

For the clock speed value, please refer the following table.

Timer 3 Block Diagram



Timer Mode Register 3: (TMOD3, $013) (FCYC = 1/TCYC = Fmain/4 or Fmain/8 or Fmain/16)

TMOD3.3	TMOD3.2	TMOD3.1	TMOD3.0	Clock speed	Clock Source	Auto-Reload
0	0	0	0	FCYC / 2048	Main oscillator	No
0	0	0	1	FCYC / 1024	Main oscillator	No
0	0	1	0	FCYC / 512	Main oscillator	No
0	0	1	1	FCYC / 128	Main oscillator	No
0	1	0	0	FCYC / 32	Main oscillator	No
0	1	0	1	FCYC / 16	Main oscillator	No
0	1	1	0	FCYC / 8	Main oscillator	No
0	1	1	1	FCYC / 2	Main oscillator	No
1	0	0	0	FCYC / 2048	Main oscillator	Yes
1	0	0	1	FCYC / 1024	Main oscillator	Yes
1	0	1	0	FCYC / 512	Main oscillator	Yes
1	0	1	1	FCYC / 128	Main oscillator	Yes
1	1	0	0	FCYC / 32	Main oscillator	Yes
1	1	0	1	FCYC / 16	Main oscillator	Yes
1	1	1	0	FCYC / 8	Main oscillator	Yes
1	1	1	1	FCYC / 2	Main oscillator	Yes

Liquid Crystal Display (LCD)

This chip can directly drive a LCD panel of up to 896 dots (16 commons x 56 segments). LCD driver contains:

- LCD controller/driver
- Display RAM for storing display data ($100~$1FF) (some of them are empty space (no memory cell))
- 16 common output pins (COM0~COM15)
- 56 segment output pins (SEG0~SEG55)
- 16-level contrast control with external adjustment

LCD control register, LCON, is used to turn the LCD display on and off so as to save energy in some cases. Also, it can control the LCD bias voltage to accommodate different type of LCD.

LCD mode register 0, LMOD0, is in charge of controlling the frame frequency of LCD and the display modes.

Users can select 1/8 or 1/16 duty for LCD by setting or resetting the bit, LMOD1.0. When it is reset to zero, for example, 1/8 duty will be performed and COM8~COM15 will also be recovered to be the normal I/O ports, Port3, Port4. In addition, LMOD1.1~LMOD1.3 offers 5 choices of I/O combination.

When LCON.0 is set, the LCD would always be enabled even in STOP or HALT mode.

LCD Control Register: LCON ($017)

LCON.3	LCON.2	LCON.1	LCON.0	Function
0	0		0	Disable LCD (Power off)
0	0		1	Enable LCD (Power on)
0	0	0		1/5 bias
0	0	1		1/4 bias

LCD Mode Register 0: LMOD0 ($018)

LMOD0.3	LMOD0.2	LMOD0.1	LMOD0.0	Function
		0	0	All LCD dots off (Blank)
		0	1	All LCD dots on
		1	0	Normal display
		1	1	Normal display
0	0			Frame Frequency = 32Hz
0	1			Frame Frequency = 64Hz
1	0			Frame Frequency = 128Hz
1	1			Frame Frequency = 256Hz

LCD Mode Register 1: LMOD1 ($019)

LMOD1.3	LMOD1.2	LMOD1.1	LMOD1.0	Pin30~33	Pin34~37	Pin38~41	Pin42~45	Pin82~85	Pin86~89	Duty
0	0	0		SEG40~43	SEG44~47	SEG48~51	SEG52~55			
0	0	1		SEG40~43	SEG44~47	SEG48~51	Port5.3~0			
0	1	0		SEG40~43	SEG44~47	Port6.3~0	Port5.3~0			
0	1	1		SEG40~43	Port7.3~0	Port6.3~0	Port5.3~0			
1	X	X		Port8.3~0	Port7.3~0	Port6.3~0	Port5.3~0			
			0					Port3.0~3	Port4.0~3	1/8
			1					COM8~11	COM12~15	1/16

LCD RAM Mapped Address

LCD data RAM ($100-$1FF) is a dual port RAM that data can be transferred without any software restriction. Each bit represents a segment value, SEGn, corresponding to a COMn and can be set (LCD dot on) or reset (LCD dot off) by bit or nibble operation instructions. The following diagram shows the configuration of the RAM Mapped of LCD.

LCD RAM Area Configuration

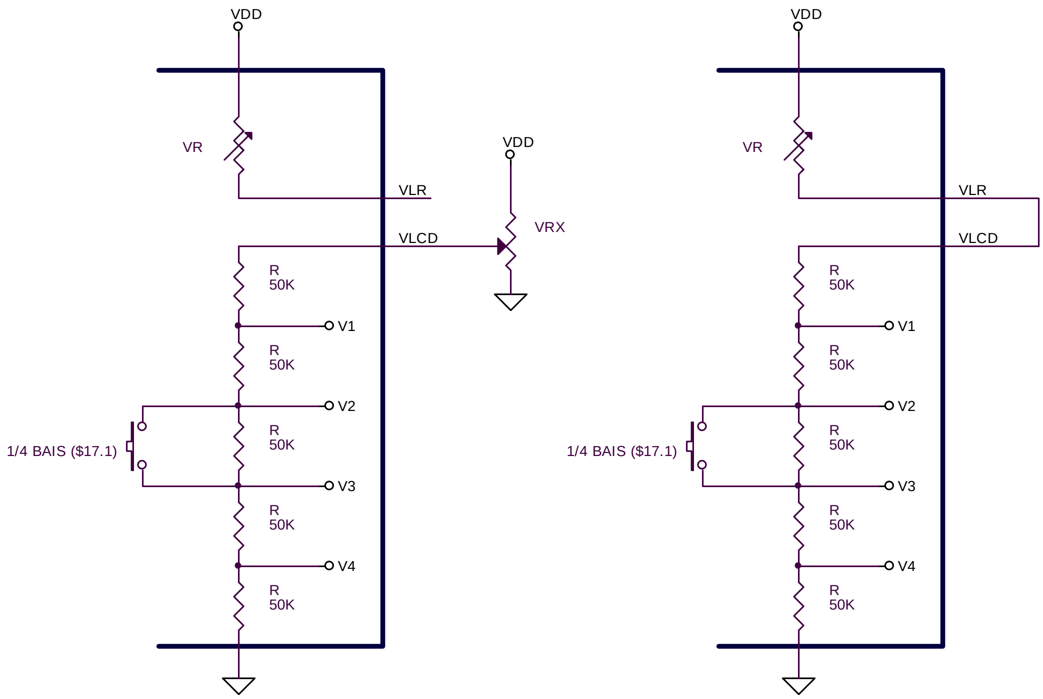
COM0					COM1					. . . .	COM15				
Addr	**B3**	**B2**	**B1**	**B0**	**Addr**	**B3**	**B2**	**B1**	**B0**	. . . .	**Addr**	**B3**	**B2**	**B1**	**B0**
$100	SEG3	SEG2	SEG1	SEG0	$110	SEG3	SEG2	SEG1	SEG0	. . . .	$1F0	SEG3	SEG2	SEG1	SEG0
$101	SEG7	SEG6	SEG5	SEG4	$111	SEG7	SEG6	SEG5	SEG4	. . . .	$1F1	SEG7	SEG6	SEG5	SEG4
$102	SEG11	SEG10	SEG9	SEG8	$112	SEG11	SEG10	SEG9	SEG8	. . . .	$1F2	SEG11	SEG10	SEG9	SEG8
$103	SEG15	SEG14	SEG13	SEG12	$113	SEG15	SEG14	SEG13	SEG12	. . . .	$1F3	SEG15	SEG14	SEG13	SEG12
$104	SEG19	SEG18	SEG17	SEG16	$114	SEG19	SEG18	SEG17	SEG16	. . . .	$1F4	SEG19	SEG18	SEG17	SEG16
$105	SEG23	SEG22	SEG21	SEG20	$115	SEG23	SEG22	SEG21	SEG20	. . . .	$1F5	SEG23	SEG22	SEG21	SEG20
$106	SEG27	SEG26	SEG25	SEG24	$116	SEG27	SEG26	SEG25	SEG24	. . . .	$1F6	SEG27	SEG26	SEG25	SEG24
$107	SEG31	SEG30	SEG29	SEG28	$117	SEG31	SEG30	SEG29	SEG28	. . . .	$1F7	SEG31	SEG30	SEG29	SEG28
$108	SEG35	SEG34	SEG33	SEG32	$118	SEG35	SEG34	SEG33	SEG32	. . . .	$1F8	SEG35	SEG34	SEG33	SEG32
$109	SEG39	SEG38	SEG37	SEG36	$119	SEG39	SEG38	SEG37	SEG36	. . . .	$1F9	SEG39	SEG38	SEG37	SEG36
$10A	SEG43	SEG42	SEG41	SEG40	$11A	SEG43	SEG42	SEG41	SEG40	. . . .	$1FA	SEG43	SEG42	SEG41	SEG40
$10B	SEG47	SEG46	SEG45	SEG44	$11B	SEG47	SEG46	SEG45	SEG44	. . . .	$1FB	SEG47	SEG46	SEG45	SEG44
$10C	SEG51	SEG50	SEG49	SEG48	$11C	SEG51	SEG50	SEG49	SEG48	. . . .	$1FC	SEG51	SEG50	SEG49	SEG48
$10D	SEG55	SEG54	SEG53	SEG52	$11D	SEG55	SEG54	SEG53	SEG52	. . . .	$1FD	SEG55	SEG54	SEG53	SEG52
$10E	-	-	-	-	$11E	-	-	-	-		$1FE	-	-	-	-
$10F	-	-	-	-	$11F	-	-	-	-		$1FF	-	-	-	-

Note: ☞ The RAM spaces without name that listed above is empty space (no memory cell existed).

LCD Contrast Control

LCD contrast can easily be adjusted by software or by an external component (resistor or potentiometer). The simplified LCD power supply circuit below illustrates the idea of how the LCD contrast ratio can be adjusted by software programming. Because the VR is connected between V_{DD} and VLCD, the required contrast ratio can be set by the value of register CVAR ($03E). On the table below, it listed all the VR values according to different programming value of register, CVAR. Note that the default value of CVAR is zero. In addition, this LCD contrast can easily be modified by an external potentiometer. The following figures show how they are configured.

CVAR.3	CVAR.2	CVAR.1	CVAR.0	VR
0	0	0	0	35KΩ
0	0	0	1	30KΩ
0	0	1	0	25KΩ
0	0	1	1	20KΩ
0	1	0	0	15KΩ
0	1	0	1	10KΩ
0	1	1	0	5KΩ
0	1	1	1	0KΩ
1	0	0	0	40KΩ
1	0	0	1	45KΩ
1	0	1	0	50KΩ
1	0	1	1	55KΩ
1	1	0	0	60KΩ
1	1	0	1	65KΩ
1	1	1	0	70KΩ
1	1	1	1	75KΩ



Low Power Consumption Modes

To save power, user can issue one of the Low Power consumption modes by instructions, STOP or HALT. Both of these modes can make the CPU going sleep. It means that CPU does nothing anyway until an external interrupt or a reset signal comes up. STOP mode will save more power than that of the others (HALT or NORMAL), however, it takes a little bit longer to wake up the CPU due to the settling time for main oscillator.

Operation mode	Issued by instruction	Main oscillator	Watch oscillator	RAM Data	Registers & Flags	I/O Pins	Released by
Stop Mode	STOP	Stop	Alive	Hold	Hold	Hold	Reset, IRQ0~3, IRQT0 or IRQRT/IRQCAS
Halt Mode	HALT	Alive	Alive	Hold	Hold	Hold	Reset or any available interrupt

Battery-low Detection

To monitor power consumption, the function of battery-low detection is enabled by setting ENBAT ($01F.2) to one. The Battery-low detection table shows what the 3 bits, BAT.2-0 ($03D.2-0), would respond while the battery power drops to a certain rank of voltage level. ENBAT should be reset to zero while it is not in use.

Battery-low detection table

Power Supply Level	BAT.2	BAT.1	BAT.0
4.4V < VDD	0	0	0
3.6V < VDD ≤ 4.4V	1	0	0
2.8V < VDD ≤ 3.6V	1	1	0
VDD ≤ 2.8V	1	1	1

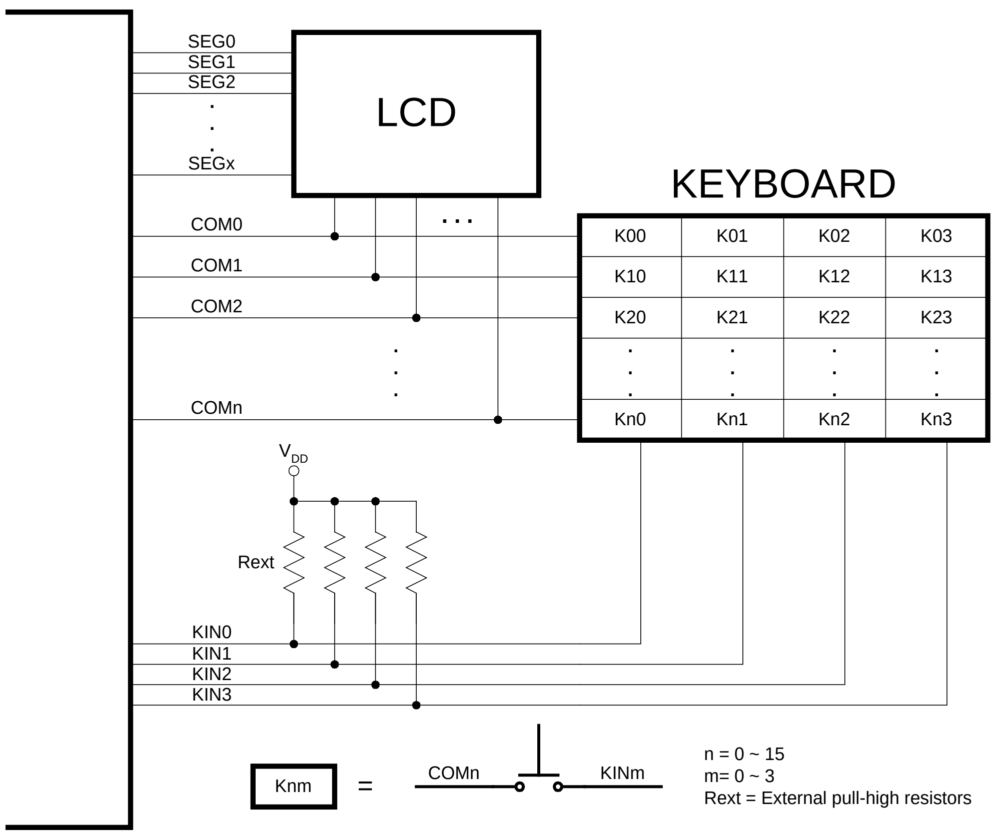
n x m Optional Keyboard (n = 16, m = 4)

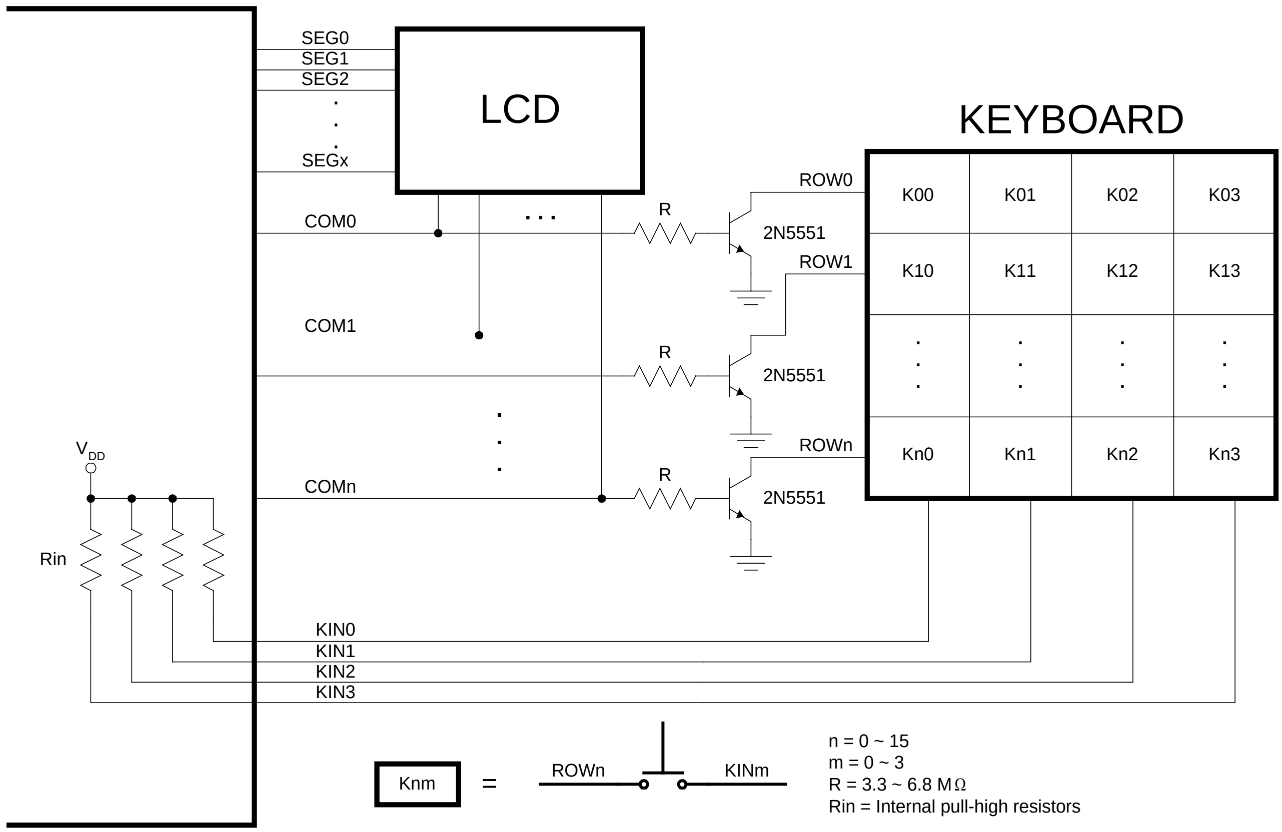
To expand the number of keypads, sharing the keyboard scan-line with LCD drivers (COM0-n) may be the best way to do so. It means the LCD drivers (COM0-n) serve not only the LCD, but keyboard scanning. Furthermore, Port2 ($\overline{\text{INT2}}$) is chosen for detecting the key pressed signal. Port2 behaves like a normal I/O port with interrupt function while KPAD = 0. After setting bit KPAD to 1, the built-in keyboard circuit will automatically scan and sample the keyboard all the time. The sampling data would then be reflected to Keyboard registers ($028 to $02F). If there is any one of the 32 bits going low (normal high), the KPRS bit will go high right away. Otherwise, KPRS will go low. However, keyboard de-bounce function is not offered for this version.

Due to only 8 nibbles keyboard registers ($028 to $02F), the 16 common signals (COM0 ~ COM15) are divided two parts for the keyboard scanning. If KB2 ($1F.3) is zero, the scanning signals are from COM0 ~ 7. If KB2 ($1F.3) is one, the scanning signals are from COM8 ~ 15.

To prevent affecting the display quality from pressing key(s), there are two recommended methods:

1. Disable Port2 internal pull-high resistors. Using external pull-high resistors (~330KΩ) for Port2, and LCD must be enabled while using this keyboard scanning function.
2. An inverting buffer may be added to isolate LCD driver signal. In this case, the sampling timing must be shifted to the reversed frame by setting bit KRVS to 1. In addition, Port2 must be set to input mode with data $F so as to activate the pull-high resistors, and LCD must be enabled while using this keyboard scanning function.





Beeper Output Circuit

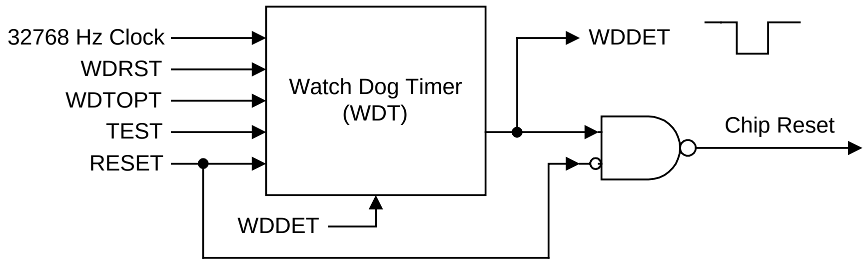
The beep output circuit can be selected by setting the RAM-mapped register bit, BEEP ($03D.0) to one. The beep mode register (BPM) is the register used to specify operation mode of the beep output circuit. This circuit can also be implement as a key-tone generator by software programming so that different key-tone may indicate different key operation message, such as, acceptance or error message.

Beep Mode Register, BPM

BEEP ($03D.0)	BPM ($00E)				P0.3	BUZ		
	BPM.3	BPM.2	BPM.1	BPM.0		CKS = xx10 (TCYC = 1.1µs)	CKS = xx01 (TCYC = 2.2µs)	CKS = xx00 (TCYC = 4.4µs)
0	X	X	X	X	Enable	Disable	Disable	Disable
1	0	X	X	X	Disable	Low	Low	Low
1	1	X	0	0	Disable	7KHz	3.5KHz	1.7KHz
1	1	X	0	1	Disable	3.5KHz	1.7KHz	874Hz
1	1	X	1	0	Disable	1.7KHz	874Hz	437Hz
1	1	X	1	1	Disable	874Hz	437Hz	219Hz

Watch-Dog Timer

This Timer is designed to prevent the system from going into the deadlock or any unexpected shutdown condition. It shares the clock source of the watch oscillator, so that it can work properly even in the stop mode. This WDT can be disabled by means of wiring WDDET pin to ground. The WDT must be cleared by reset the bit WDRST ($0D.3) before time-out (2 or 4 seconds selected by mask option; default is 4 seconds). Otherwise the WDT will send out a pulse signal, WDDET (pulse width is about 1/64 msec), to reset the whole system.



DTMF Generation Circuit

This chip provides a dual tone multi-frequency (DTMF) generation circuit. The DTMF signal consists of two sine waves with which to access the switching system. The following figure shows the relationship between the key pressed and its dual tone frequencies.
The DTMF generator employs 2 dedicate D/A converters, which can generate two separate single-tone signals, low-frequency group for Row and high-frequency group for Column. These two signals would finally mix together producing a Dual Tone Frequency Signal. Each single-tone signal consists of 32-level waveform that guarantees low distortion signal quality.
This DTMF is basically controlled by a 4-bit write-only Tone Generator Control register, TGC, and the signal data would be prepared by programming another 4-bit write-only register called Tone Generator Data register, TGD.
These two registers, TGC & TGD, would be cleared to zero while system is reset.
Single Tone signal can also be generated for quality checking by means of programming TGC.1 or TGC.2.

COL / ROW	1209Hz	1336Hz	1477Hz	1633Hz
697Hz	1	2	3	A
770Hz	4	5	6	B
852Hz	7	8	9	C
941Hz	#	0	*	D

Tone Generator Control Register: TGC ($01A)

Bit 3	Bit 2	Bit 1	Bit 0	Function		
				Column signal	Row signal	DTMF power
	X	X	0	Disable	Disable	OFF
	0	0	1	Disable	Disable	ON
	0	1	1	Disable	Enable	ON
	1	0	1	Enable	Disable	ON
	1	1	1	Enable	Enable	ON

Tone Generator Data Register: TGD ($01B)

Bit 3	Bit 2	Bit 1	Bit 0	Output Frequency	Digit
0	1	1	1	941 + 1336Hz	″0 ″
0	0	0	0	697 + 1209Hz	″1 ″
0	1	0	0	697 + 1336Hz	″2 ″
1	0	0	0	697 + 1477Hz	″3 ″
0	0	0	1	770 + 1209Hz	″4 ″
0	1	0	1	770 + 1336Hz	″5 ″
1	0	0	1	770 + 1477Hz	″6 ″
0	0	1	0	852 + 1209Hz	″7 ″
0	1	1	0	852 + 1336Hz	″8 ″
1	0	1	0	852 + 1477Hz	″9 ″
0	0	1	1	941 + 1209Hz	″* ″
1	0	1	1	941 + 1477Hz	″# ″
1	1	0	0	697 + 1633Hz	″A ″
1	1	0	1	770 + 1633Hz	″B ″
1	1	1	0	852 + 1633Hz	″C ″
1	1	1	1	941 + 1633Hz	″D ″

Clock Selection Register: CKS ($00D)

CKS.0~1 is in charge of controlling the speed of CPU. After the value of CKS.0~1 has been changed, the speed of CPU will be changed on the next instruction without any additional delay. ENOSC (CKS.2) is such a bit for controlling the clock source for FSK demodulator and Frequency counter for Ring detection. For Caller-ID application, it is recommended that ENOSC should be set to one during initialization.

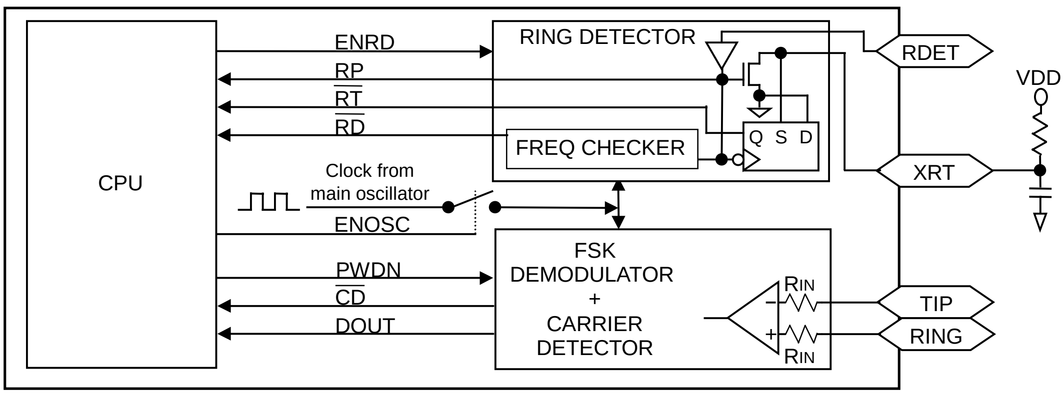
Bit3	Bit2	Bit1	Bit0	Description
		0	0	System Clock = Fmain / 16
		0	1	System Clock = Fmain / 8
		1	0	System Clock = Fmain / 4
		1	1	Inhibited
	0			Disable the clock for FSK demodulator
	1			Enable the clock for FSK demodulator (Must be set to one during initialization)

Built-in FSK Demodulator, Carrier Detector and Ring Detector

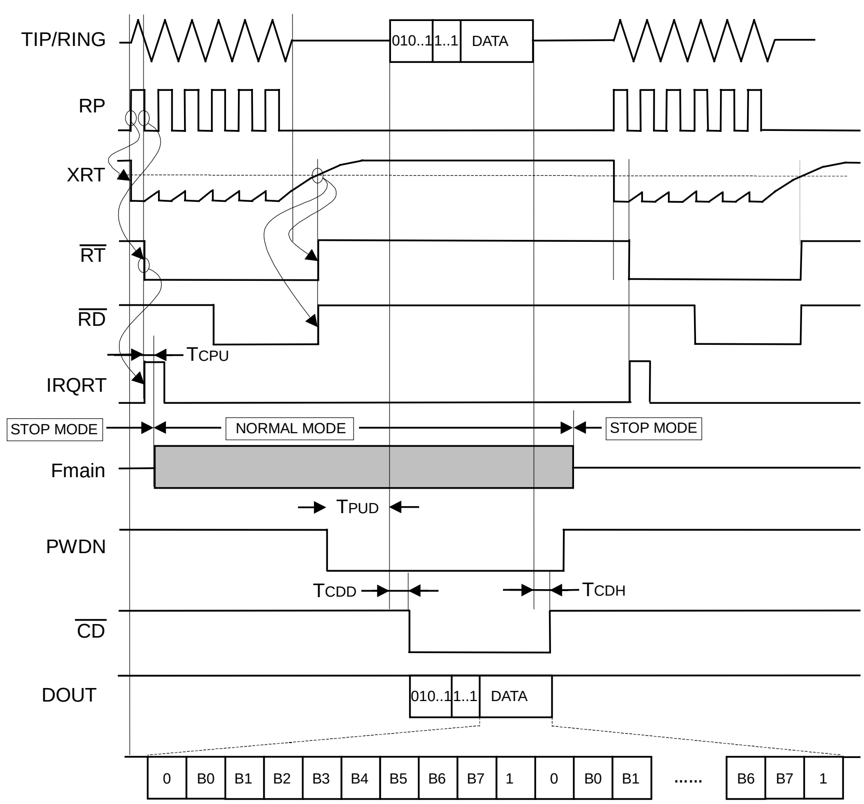
A FSK demodulator, Carrier detector and Ring detector are employed to serve the Calling Identification. These circuits are merged to a 4-bit CPU by several interface signals, which are described below:

Fmain: System clock from main oscillator
ENRD: Enable the internal Ring Detector
PWDN: Switch off/on the FSK demodulator only
$\overline{\text{RP}}$: Ring pulse signal
$\overline{\text{RT}}$: Ring time signal
$\overline{\text{XRT}}$: Ring detected output signal
$\overline{\text{RD}}$: Ring detected signal (signal confirmed)
$\overline{\text{CD}}$: Carrier detected signal
DOUT: Data output stream

If there is any part of the Ring Detector has to be utilized, bit ENRD must be set to 1 first. CD or $\overline{\text{RD}}$ will be available only if ENOSC = 1. It is recommended that bit ENOSC should be set to one during initialization. Details should be referred to the section of Timing Description.



Timing Diagram (ENRD = ENOSC = 1)



Timing description

A. Hardware detection with internal Ring Detector (ENRD=1)

Step 1: After power up initialization, CPU should enters into stop mode, and also FSK demodulator should enters into power down mode for saving power.

Step 2: During ringing, the internal Ring Detector will sense the ring-in signal and will send out an interrupt request, IRQRT, to CPU. After receiving such request, CPU will then activate the main oscillator, so as to enter into normal operation mode.

Step 3: Afterwards, CPU should keep on watching the bit RD ($3C.2) until time out. If RD goes low (signal has been has been confirmed by internal ring detector), CPU should check the bit RT until it goes high. At this moment, CPU should reset bit PWDN ($3D.2) in order to turn on the FSK demodulator for detecting carrier. Otherwise, CPU should return to STOP mode until next.

Step 4: Once the FSK demodulator senses the FSK signal, the bit CD ($3C.1) would go low and an interrupt request, IRQCD, would be issued. This interrupt request starts up the service routine for sampling out the data stream from the bit DOUT.

Step 5: CD and DOUT will go back to high after FSK signal disappeared. Also CPU should then return to STOP mode and prepares for another Ringing.

B. Software detection with internal Ring Detector (ENRD=1)

Step 1: After power up initialization, CPU should enters into stop mode, and also FSK demodulator should enters into power down mode for saving power.

Step 2: During ringing, the internal Ring Detector will sense the ring-in signal and will send out an interrupt request, IRQRT, to CPU. After receiving such request, CPU will then activate the main oscillator, so as to enter into normal operation mode.

Step 3: Afterwards, CPU should check the bit RP ($3D.3) bit if it is ring-in signal until time out. (Notes that checking the ringing frequency by software needs a relative complicate programming sequence!) If this RP signal has been confirmed by software, CPU should check the bit RT until it goes high. At this moment, CPU should reset bit PWDN ($3D.2) in order to turn on the FSK demodulator for detecting carrier. Otherwise, CPU should return to STOP mode until next.

Step 4: Once the FSK demodulator senses the FSK signal, the bit CD ($3C.1) would go low and an interrupt request, IRQCD, would be issued. This interrupt request starts up the service routine for sampling out the data stream from the bit DOUT.

Step 5: CD and DOUT will go back to high after FSK signal disappeared. Also CPU should then return to STOP mode and prepares for another Ringing.

C. Software detection with external Ring Detector (ENRD=0, and IRQn is employed)

Step 1: After power up initialization, CPU should enters into stop mode, and also FSK demodulator should enters into power down mode for saving power.

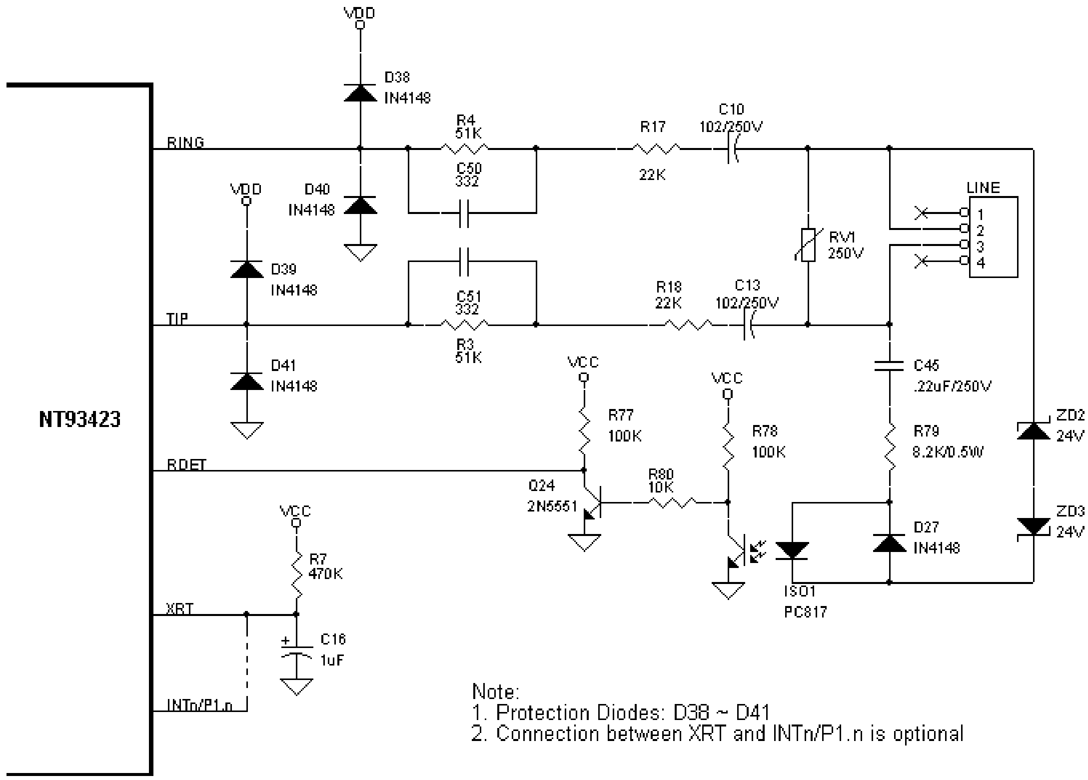
Step 2: During ringing, the external Ring Detector will sense the ring-in signal and should send out a negative-edge signal to pin INTn/P1.n, so as to trigger IRQn. After receiving such request, CPU will then activate the main oscillator, so as to enter into normal operation mode.

Step 3: Afterwards, CPU should keep on watching the pin P1.n until it goes high. At this moment, CPU should reset bit PWDN ($3D.2) in order to turn on the FSK demodulator for detecting carrier. Otherwise, CPU should return to STOP mode until next.

Step 4: Once the FSK demodulator senses the FSK signal, the bit CD ($3C.1) would go low and an interrupt request, IRQCD, would be issued. This interrupt request starts up the service routine for sampling out the data stream from the bit DOUT.

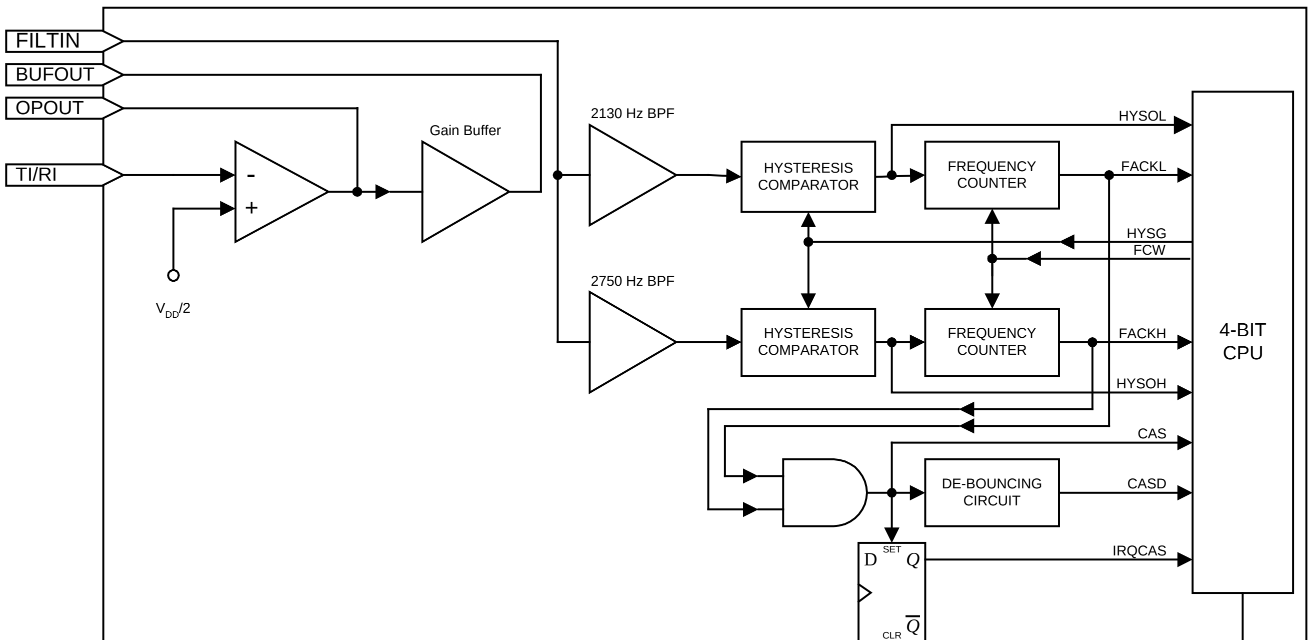
Step 5: CD and DOUT will go back to high after FSK signal disappeared. Also CPU should then return to STOP mode and prepares for another Ringing.

Application Circuits (for reference only)



Built-in CAS Detector

A CAS detector is employed to detect Bellcore's CPE Alerting Signal. This CAS detector is merged to a 4-bit CPU by several interface signals.
CAS detection is enabled when bit ENCAS ($3D.3) is set.
After the CAS tone came in, this multi-tone would be separated into two by the Band-pass filters. These two signals are re-shaped into two different square waves, HYSOL ($3E.2) and HYSOH ($3E.3). The overall delay time for these two signals is T_{fd1}. For further confirmation, these two signals are checked up by two groups of Frequenter Counter. The confirmation signals, FACKH ($39.3) and FACKL ($39.2), would go high after the delay time, $T_{dl}1$ and T_{dh1}, respectively. If both of these two confirmation signals come out, CAS ($3E.1) and IRQCAS ($24.2) will go high at this moment. In order to make a double confirm of the CAS signal, a De-bounce circuit is made to give the final output, CASD ($3E.0). After the CAS tone went out, all the output signals (HYSOL, HYSOH, FACKL, FACKH, CAS, and CASD) will return to zero. However, IRQCAS can only be reset by software. To improve the reliability, the input can be adjusted by programming the Gain Control Register through bit HYSG ($3A.1) and DBUF ($3F). Also, the speed and accuracy can be adjusted by programming the Frequency Control Register through bit FCW ($3A.0) and DBUF ($3F).



Block Diagram of CAS Tone Detector

Timing description

Step 1: Set IERT/IECAS ($24.3) to receive CAS interrupt.

Step 2: If CPU detects off hook state, CPU should enter into operating mode, and set ENCAS ($3D.3) to power up CAS detector. However, FSK demodulator should be still in power down mode.

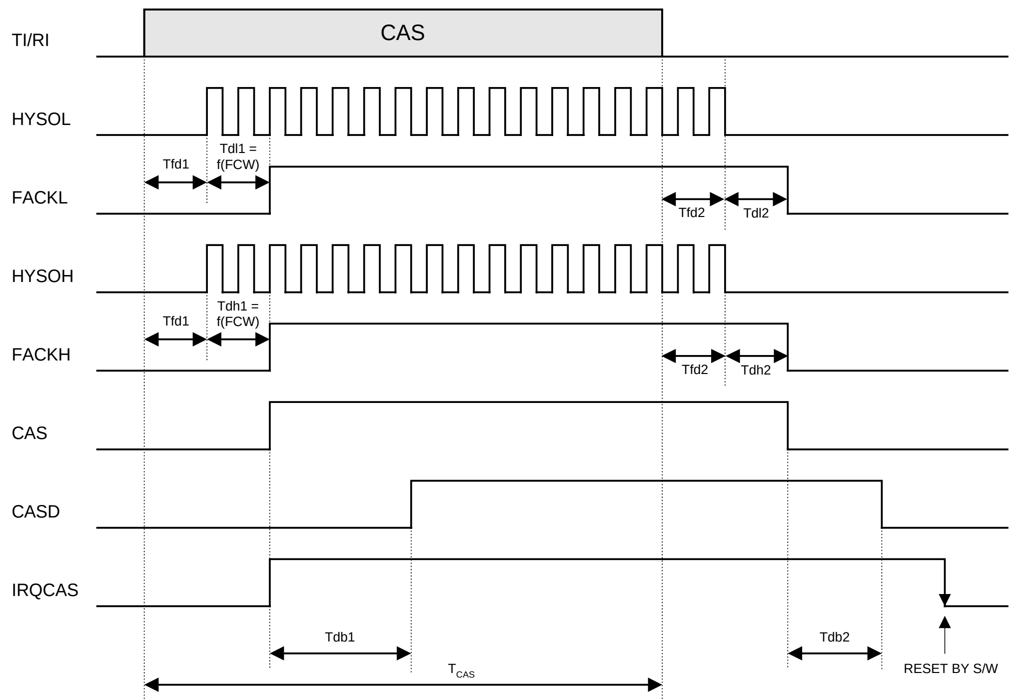
Step 3: If CAS interrupt occurs, CPU should go to the subroutine to process the CAS signal and send out DTMF signal D.

Step 4: After generating DTMF signal D, CPU should reset bit PWDN ($3D.2) in order to turn on the FSK demodulator for detecting carrier.

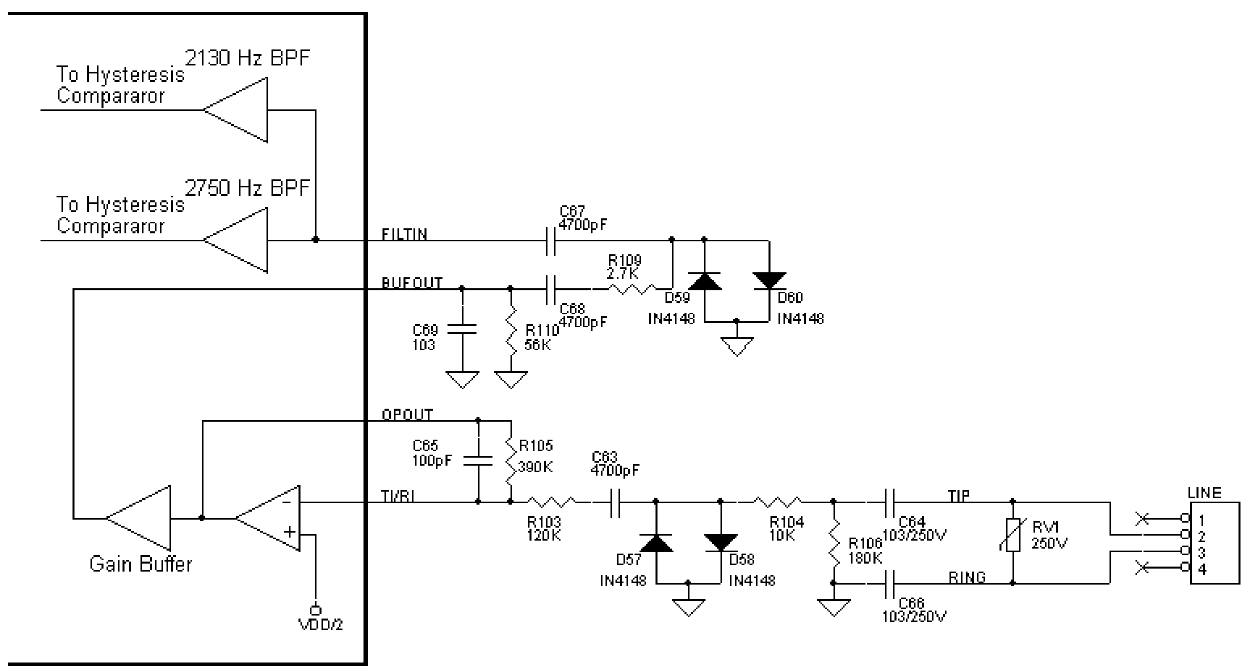
Step 5: Once the FSK demodulator senses the FSK signal, the bit CD ($3C.1) would go low and an interrupt request, IRQCD, would be issued. This interrupt request starts up the service routine for sampling out the data stream from the bit DOUT.

Step 6: CD and DOUT will go back to high after FSK signal disappeared. Also CPU should then power down FSK demodulator to reduce power consumption and prepares for the next CAS signal occurs.

Timing Diagram (ENCAS = 1)



Application circuits (for reference only)

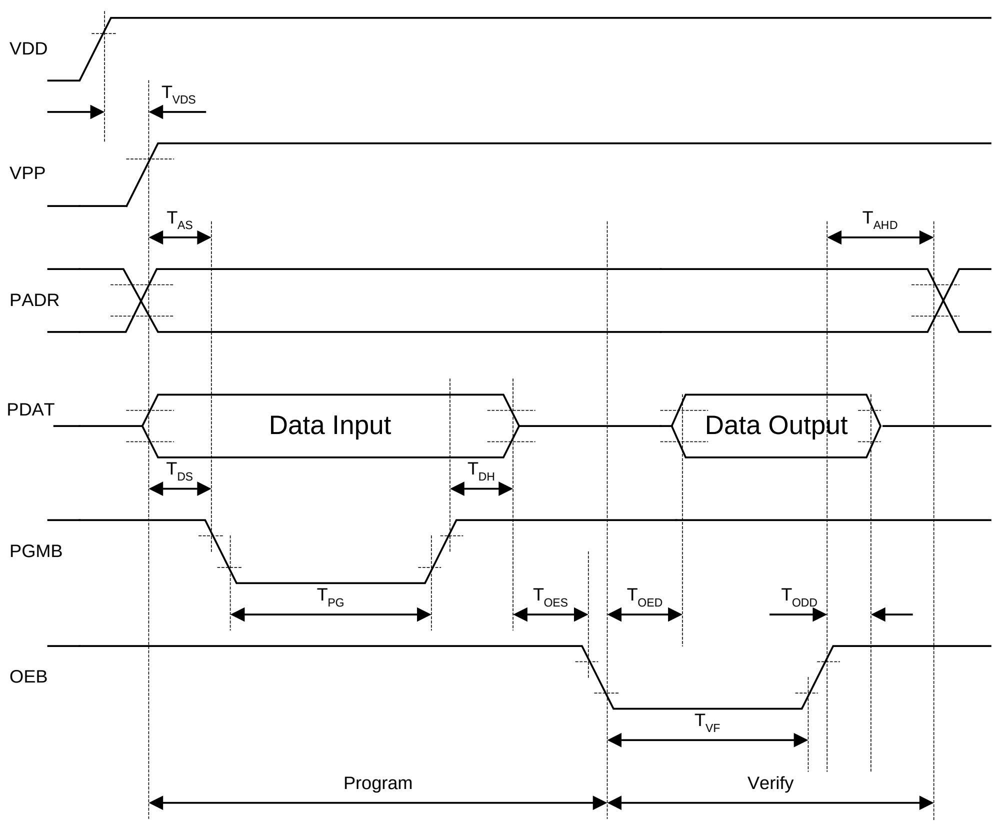


OTP Operation

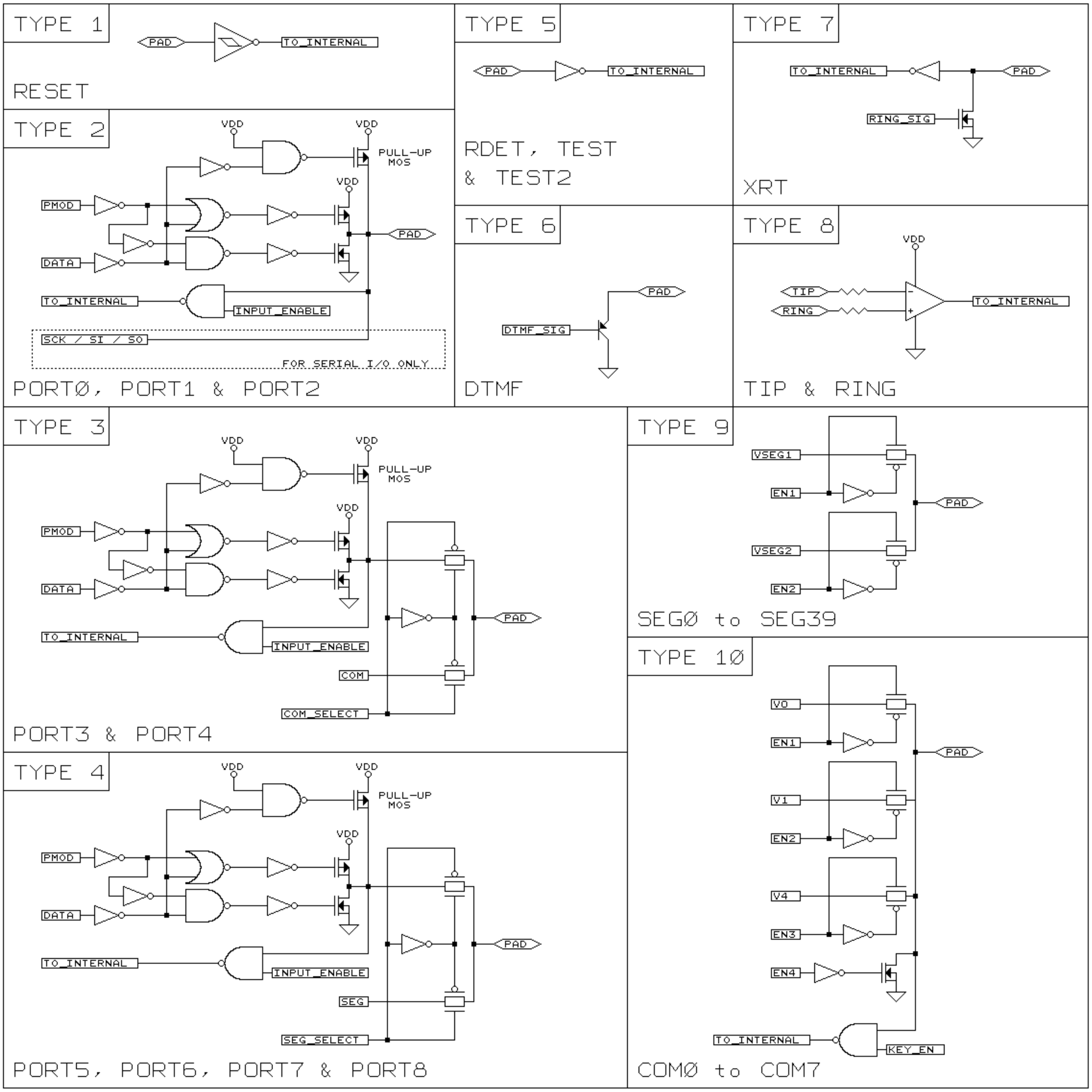
OTP mode selection table:

Mode	PGMB	OEB	PDAT0 ~ 9	V_{PP}	V_{PX}	TEST/TEST2
Programming	Low	High	Data Input	10.5 V	10.5 V	Connected to OTP Writer
Verify	High	Low	Data Output	10.5 V	10.5 V	Connected to OTP Writer
Programming Inhibited	-	-	-	GND	Floating	High

Timing Diagram



Pin definition with its structure



RESET

SH93P423A can be reset by external RESET pin or internal WDT. To reset this chip by external pin, the reset pin should be held high at least two execution cycles. The following table shows the initial conditions for different operation mode after RESET.

RAM Mapped Register Initial Value in Normal mode

<table>
<tr><th>Name</th><th>Address</th><th>Initial</th><th>R/W/s/r/t</th><th colspan="3">Note</th></tr>
<tr><td>Program Counter (PC)</td><td>-</td><td>$0000</td><td>R/W/s/r/t</td><td colspan="3">Refer to section of Stack pointer</td></tr>
<tr><td>Stack Pointer (SP)</td><td>$20~$22</td><td>$023F</td><td>R/t</td><td colspan="3">Refer to section of Stack pointer</td></tr>
<tr><td>Status Flag (SF)</td><td>-</td><td>:1</td><td>By software</td><td colspan="3">Refer to section of Stack pointer</td></tr>
<tr><td>Carry Flag (CY)</td><td>-</td><td>Retained</td><td>By software</td><td colspan="3">Data will be loss (unknown value) when VDD < VT</td></tr>
<tr><td>General register (A, B, V, X, Y, EX, EY)</td><td>-</td><td>Retained</td><td>By software</td><td colspan="3">Data will be loss (unknown value) when VDD < VT</td></tr>
<tr><td>Data RAM</td><td>-</td><td>Retained</td><td>R/W/s/r/t</td><td colspan="3">Data will be loss (unknown value) when VDD < VT</td></tr>
<tr><td>Interrupt
- Interrupt enable (IE)
- All Request enable flags
- All Interrupt request flags</td><td>-</td><td>
:0
:0
:0</td><td>
s/r/t
s/r/t
r/t</td><td colspan="2">
0 = Interrupt disabled
0 = Request disabled
0 = No request</td><td>
1 = Interrupt enabled
1 = Request enabled
1 = With request</td></tr>
<tr><td>I/O Port
- I/O mode of any port
- Data on any I/O pin
- Pull-up resistor</td><td>-</td><td>
:0
:1
Enabled</td><td>
W
R/W/s/r/t</td><td colspan="3">Except Port9.0 & Port9.1
0: Input | 1: Output</td></tr>
<tr><td>Timer
- Mode register (TMODn)
- Counter register (TCnx)
- Load register (TLnx)</td><td>-</td><td>
$00
$00 / $000
$00 / $000</td><td>
W
R
W</td><td colspan="3">Refer to section of RAM mapped</td></tr>
<tr><td>OVF0.0~3</td><td>$04.0-3</td><td>:0000</td><td>R</td><td colspan="3"></td></tr>
<tr><td>Serial Interface
- Mode register (SIOM)
- Internal octal counter
- Serial data register (SIOH,SIOL)</td><td>
$0C
-
$0A,$0B</td><td>
$0
$0
Retained</td><td>
R/W

R/W/t</td><td colspan="3">Refer to section of Serial interface</td></tr>
<tr><td>LCD
- Control register (LCON)
- Mode register (LMOD0-1)</td><td>
$17
$18, $19</td><td>
$0
$0</td><td>
W/s/r
W</td><td colspan="3">Refer to section of LCD</td></tr>
<tr><td>CKS.1.0</td><td>$0D.1.0</td><td>:00</td><td>W</td><td>:00 = Fmain/16</td><td>:01 = Fmain/8</td><td>:10 = Fmain/4</td></tr>
<tr><td>ENOSC (CKS.2)</td><td>$0D.2</td><td>:0</td><td>W</td><td colspan="3">It must be set to one during initialization</td></tr>
<tr><td>WDRST</td><td>$0D.3</td><td>:0</td><td>r</td><td colspan="3"></td></tr>
<tr><td>BPM</td><td>$0E</td><td>:0000</td><td>W</td><td colspan="3">Refer to section of BEEPER</td></tr>
<tr><td>TGC</td><td>$1A</td><td>:0000</td><td>W</td><td colspan="3">Refer to section of DTMF GENERATOR</td></tr>
<tr><td>TGD</td><td>$1B</td><td>:0000</td><td>W</td><td colspan="3">Refer to section of DTMF GENERATOR</td></tr>
<tr><td>KRVS</td><td>$1F.0</td><td>:0</td><td>W/t</td><td colspan="2">0 = Non inverted</td><td>1 = Inverted</td></tr>
<tr><td>KPAD</td><td>$1F.1</td><td>:0</td><td>W/t</td><td colspan="2">0 = Disable</td><td>1 Enable</td></tr>
<tr><td>ENBAT</td><td>$1F.2</td><td>:0</td><td>W</td><td colspan="2">0 = Disable</td><td>1 = Enable</td></tr>
<tr><td>KPRS</td><td>$1F.3</td><td>:0</td><td>R/t</td><td colspan="2">0 = Any key released</td><td>1 = Any key pressed</td></tr>
<tr><td>KB2</td><td>$1F.3</td><td>:0</td><td>W/s/r</td><td colspan="2">0 = Disable 2nd page</td><td>1 = Enable 2nd page</td></tr>
<tr><td>KREG0~7</td><td>$28~$2F</td><td>:1111</td><td>R/W/t</td><td colspan="2">0 = Key pressed</td><td>1 = Key released</td></tr>
<tr><td>Port9.0, 9.1</td><td>$39.0-1</td><td>:11</td><td>W/s/r/t</td><td colspan="3"></td></tr>
<tr><td>FACKL, FACKH</td><td>$39.2-3</td><td>:00</td><td>t</td><td colspan="2">0 = Invalid signal output</td><td>1 = Valid signal output</td></tr>
<tr><td>BANK</td><td>$3A.2</td><td>:0</td><td>s/r/t</td><td colspan="2">0 = RAM $000 ~ $FFF</td><td>1 = RAM $1000 ~</td></tr>
<tr><td>FCW, HYSG</td><td>$3A.0-1</td><td>:00</td><td>s</td><td colspan="3"></td></tr>
<tr><td>DOUT</td><td>$3C.0</td><td>:1</td><td>R/t</td><td colspan="3">Data output stream</td></tr>
<tr><td>$\overline{CD}$</td><td>$3C.1</td><td>:1</td><td>R/t</td><td colspan="2">0 = Carrier detected</td><td>1 = No carrier</td></tr>
<tr><td>$\overline{RD}$</td><td>$3C.2</td><td>:1</td><td>R/t</td><td colspan="2">0 = Ring detected</td><td>1 = No Ring</td></tr>
<tr><td>$\overline{RT}$</td><td>$3C.3</td><td>:1</td><td>R/t</td><td colspan="2">0 = Ring time detected</td><td>1 = No Ring time signal</td></tr>
<tr><td>PWDN</td><td>$3D.2</td><td>:1</td><td>W</td><td colspan="2">0 = FSK power up</td><td>1 = FSK power down</td></tr>
</table>

Name	Address	Initial	R/W/s/r/t	Note	
ENRD	$3D.1	:1	W	0 = Disable ring detector	1 = Enable ring detector
BEEP	$3D.0	:0	W	0 = I/O Enabled	1 = Beeper enabled
BAT.0	$3D.0	:1	R/t	0 = $V_{DD} > 2.8V$	1 = $V_{DD} < 2.8V$
BAT.1	$3D.1	:1	R/t	0 = $V_{DD} > 3.6V$	1 = $V_{DD} < 3.6V$
BAT.2	$3D.2	:1	R/t	0 = $V_{DD} > 4.4V$	1 = $V_{DD} < 4.4V$
RP	$3D.3	:0	R/t	Refer to section of RING DETECTOR	
ENCAS	$3D.3	:0	W	0 =disable CAS detector	1 =Enable CAS detector
CVAR.0-3	$3E.0-3	:0000	W	Refer to section of LCD Contrast Control	
CASD	$3E.0	:0	R/t	0 = Invalid signal output	1 = Valid signal output
CAS	$3E.1	:0	R/t	0 = Invalid signal output	1 = Valid signal output
HYSOL, HYSOH	$3E.2-3	:00	R/t	0 = Invalid signal output	1 = Valid signal output
DBUF.0-3	$3F.0-3	:0000	R/W		

Note: n = 0, 1, 2, 3; x = 0, 1, 2 $data = Hexadecimal data, :data = Binary data, V_T = Retention voltage

Addressing Mode

As shown below, there are 3 kinds of RAM addressing modes and 5 kinds of ROM addressing modes.

RAM Addressing Mode

1. Register indirect addressing:

Bit location	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM address	Bank	V3	V2	V1	V0	X3	X2	X1	X0	Y3	Y2	Y1	Y0

2. Direct addressing:

Bit location	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM address	0	0	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0

3. Memory register addressing:

Bit location	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM address	0	0	0	0	0	1	0	0	m3	m2	m1	m0

ROM addressing mode

1. Direct addressing:

Bit location	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ROM address	k3	k2	k1	k0	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0

Example: LBR label ;label is an absolute address complied by the assembler

2. Zero page addressing:

Bit location	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ROM address	0	0	0	0	0	0	0	0	a5	a4	a3	a2	a1	a0

Example: CAL addr ;addr = a0~5

3. Short branch addressing:

Bit location	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ROM address							x7	x6	x5	x4	x3	x2	x1	x0

Example: Lab1: BR addr ;addr = x0~7, local page address (256 addresses per page).
;If Lab1 is the last address of that page (Lab1 = $XXFF),
;the branch address will be pointer to that address (x0~7) of the next page.

4. Table jump addressing:

Bit location	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ROM address	0	0	p3	p2	p1	p0	B3	B2	B1	B0	A3	A2	A1	A0

Example: TJMP p ;p = p0~3, A0~3 = content of A register, B0~3 = content of B register

5. Table data addressing:

Bit location	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ROM address	0	0	p3	p2	p1	p0	B3	B2	B1	B0	A3	A2	A1	A0

Let ROM data = M9, M8, M7, M6, M5, M4, M3, M2, M1, M0
If R08 = 1, then Register B ← M4~7 and Register A ← M0~3
If R09 = 1, then Port3 ← M4~7 and Port2 ← M0~3

Example: T p ;p = p0~3, A0~3 = content of A register, B0~3 = content of B register

Instruction Set

1. Transfer instruction

1a. Immediate instruction
1b. Register to register instruction
1c. RAM address instruction
1d. RAM register instruction

2. Bit operation instruction

3. Compare instruction

4. Arithmetic and logical instruction

5. Control instruction

5a. Branch instruction
5b. Subroutine stack control instruction
5c. CPU control instruction
5d. Table data generation instruction

Symbol	Descriptions	
CY	Carry Flag	
SF	Status Flag	
PC	Program Counter	
NZ	Virtual Flag for non zero result (result $\neq$ 0)	☞ Virtual Flag is not a real one, but would reflect a 1 to Status Flag in some operations.
NB	Virtual Flag for result without borrowed (result $\geq$ 0)	
OVF	Virtual Flag for overflowed result (result $>$ 15)	
W/C	Word / Execution Cycle	
$\leftarrow$	Transfer to (Copy to)	
$\leftrightarrow$	Exchange with	
k	4-bit block address (1 block = 1024 memory address)	
p	4-bit page address (1 page = 256 memory address)	
a	6-bit address	
x	8-bit address	
d	10-bit address	
i	Immediate data	
m	Memory register index (0~15)	
n	2-bit data that indicates the bit location of a memory data or register	
M	A specific memory bit representation	
N	The current no of level of subroutine	
M.n	A specific memory bit representation	
$data	Hexadecimal data	☞ Data without '$' sign or ':' sign is assumed to be decimal data
:data	Binary data	

Descriptions

1. Transfer instruction:

1a. Immediate Instructions

Operation	Mnemonic	Code	SF	W/C	Function
Store immediate to A	ITA i	130 + i		1/1	A ← i
Store immediate to B	ITB i	100 + i		1/1	B ← i
Store immediate to memory, Increment Y	ITMIY i	190 + i	NZ	1/1	M ← i, Y ← Y + 1
Store immediate to direct memory	ITMD i, d	2A0 + i d		2/2	M (direct) ← i

1b. Register to register instructions

Operation	Mnemonic	Code	SF	W/C	Function
Store B to A	BTA	044		1/1	A ← B
Store V to A	VTA	200 000		2/2	A ← V
Store Y to A	YTA	0AF		1/1	A ← Y
Store EX to A	EXTA	064		1/1	A ← EX
Store EY to A	EYTA	054		1/1	A ← EY
Store Rm to A	RTA m	170 + m		1/1	A ← Rm
Store A to B	ATB	0C4		1/1	B ← A
Exchange A and Rm	XAR m	1F0 + m		1/1	A ↔ Rm

1c. RAM address instructions

Operation	Mnemonic	Code	SF	W/C	Function
Store immediate to V	ITV i	0F0 + i		1/1	V ← i
Store immediate to X	ITX i	120 + i		1/1	X ← i
Store immediate to Y	ITY i	110 + i		1/1	Y ← i
Store A to X	ATX	0E4		1/1	X ← A
Store A to Y	ATY	0D4		1/1	Y ← A
Store A to V	ATV	210 000		2/2	V ← A
Increment Y	IY	05C	NZ	1/1	Y ← Y + 1
Decrement Y	DY	0DF	NB	1/1	Y ← Y - 1
Y add A	YAA	058	OVF	1/1	Y ← Y + A
Subtract A from Y	YSA	0D8	NB	1/1	Y ← Y - A
Exchange X and EX	XEX	001		1/1	X ↔ EX
Exchange Y and EY	XEY	002		1/1	Y ↔ EY
Exchange (X, Y) and (EX, EY)	XEXY	003		1/1	X ↔ EX, Y ↔ EY

1. Transfer instruction: (continued)

1d. RAM Register instructions

Operation	Mnemonic	Code	SF	W/C	Function
Store memory to A	MTA	090		1/1	A ← M
Store memory to A, Exchange X and EX	MTAX	091		1/1	A ← M, X ↔ EX
Store memory to A, Exchange Y and EY	MTAY	092		1/1	A ← M, Y ↔ EY
Store memory to A, Exchange X and EX, Exchange Y and EY	MTAXY	093		1/1	A ← M, X ↔ EX, Y ↔ EY
Store direct memory to A	MTAD addr	290 d		2/2	A ← M (direct)
Store memory to B	MTB	040		1/1	B ← M
Store memory to B, Exchange X and EX	MTBX	041		1/1	B ← M, X ↔ EX
Store memory to B, Exchange Y and EY	MTBY	042		1/1	B ← M, Y ↔ EY
Store memory to B, Exchange X and EX, Exchange Y and EY	MTBXY	043		1/1	B ← M, X ↔ EX, Y ↔ EY
Store A to memory	ATM	098		1/1	M ← A
Store A to memory Exchange X and EX	ATMX	099		1/1	M ← A, X ↔ EX
Store A to memory Exchange Y and EY	ATMY	09A		1/1	M ← A, Y ↔ EY
Store A to memory, Exchange X and EX, Exchange Y and EY	ATMXY	09B		1/1	M ← A, X ↔ EX, Y ↔ EY
Store A to direct memory	ATMD addr	298 d		2/2	M (direct) ← A
Store A to memory, Increment Y	ATMIY	050	NZ	1/1	M ← A, Y ← Y + 1
Store A to memory, Increment Y, Exchange X and EX	ATMIYX	051	NZ	1/1	M ← A, Y ← Y + 1, X ↔ EX
Store A to memory, Decrement Y	ATMDY	0D0	NB	1/1	M ← A, Y ← Y - 1
Store A to memory, Decrement Y, Exchange X and EX	ATMDYX	0D1	NB	1/1	M ← A, Y ← Y - 1, X ↔ EX

1. Transfer instruction: (continued)

1d. RAM Register Instructions (continued)

Operation	Mnemonic	Code	SF	W/C	Function
Exchange A and memory	XAM	080		1/1	A ↔ M
Exchange A and memory, Exchange X and EX	XAMX	081		1/1	A ↔ M, X ↔ EX
Exchange A and memory, Exchange Y and EY	XAMY	082		1/1	A ↔ M, Y ↔ EY
Exchange A and memory, Exchange X and EX, Exchange Y and EY	XAMXY	083		1/1	A ↔ M, X ↔ EX, Y ↔ EY
Exchange A and direct memory	XAMD addr	280 d		2/2	A ↔ M (direct)
Exchange B and memory	XBM	0C0		1/1	B ↔ M
Exchange B and memory, Exchange X and EX	XBMX	0C1		1/1	B ↔ M, X ↔ EX
Exchange B and memory, Exchange Y and EY	XBMY	0C2		1/1	B ↔ M, Y ↔ EY
Exchange B and memory, Exchange X and EX, Exchange Y and EY	XBMXY	0C3		1/1	B ↔ M, X ↔ EX, Y ↔ EY

2. Bit Operation Instructions

Operation	Mnemonic		Code	SF	W/C	Function
Set Memory Bit	SM	n	088 + n		1/1	M.n ← 1
Set direct Memory Bit	SMD	n, addr	288 + n d		2/2	M.n (direct) ← 1
Reset Memory Bit	RM	n	084 + n		1/1	M.n ← 0
Reset direct Memory Bit	RMD	n, addr	284 + n d		2/2	M.n (direct) ← 0
Test Memory Bit	TM	n	08C + n	M.n	1/1	SF ← M.n
Test direct Memory Bit	TMD	n, addr	28C + n d	M.n	2/2	SF ← M.n (direct)

3. Compare Instructions

Operation	Mnemonic		Code	SF	W/C	Function
Immediate does not equal to Memory	INEM	i	020 + i	NZ	1/1	If i ≠ M then SF ← 1 else SF ← 0
Immediate does not equal to direct Memory	INEMD	i, addr	020 + i d	NZ	2/2	If i ≠ M (direct) then SF ← 1 else SF ← 0
A does not equal to Memory	ANEM		008	NZ	1/1	If A ≠ M then SF ← 1 else SF ← 0
A does not equal to direct Memory	ANEMD	addr	208 d	NZ	2/2	If A ≠ M (direct) then SF ← 1 else SF ← 0
B does not equal to Memory	BNEM		048	NZ	1/1	If B ≠ M then SF ← 1 else SF ← 0
Y does not equal to Immediate	YNEI	i	070 + i	NZ	1/1	If Y ≠ I then SF ← 1 else SF ← 0
Immediate is less than or equals to Memory	ILEM	i	030 + i	NZ	1/1	If i ≤ M then SF ← 1 else SF ← 0
Immediate is less than or equals to direct Memory	ILEMD	i, addr	230 + i d	NZ	2/2	If i ≤ M (direct) then SF ← 1 else SF ← 0
A is less than or equals to Memory	ALEM		018	NZ	1/1	If A ≤ M then SF ← 1 else SF ← 0
A is less than or equals to direct Memory	ALEMD	addr	218 d	NZ	2/2	If A ≤ M (direct) then SF ← 1 else SF ← 0
A is less than or equals to Immediate	ALEI	i	1B0 + i	NZ	1/1	If A ≤ I then SF ← 1 else SF ← 0
B is less than or equals to Memory	BLEM		0C8	NZ	1/1	If B ≤ M then SF ← 1 else SF ← 0

4. Arithmetic and Logical Instructions

Operation	Mnemonic	Code	SF	W/C	Function
Add immediate to A	AAI i	180 + i	OVF	1/1	A ← A + i
Increment B	IB	04C	NZ	1/1	B ← B + 1
Decrement B	DB	0CF	NB	1/1	B ← B - 1
Decimal Adjust for Addition	DAA	0A6		1/1	See instruction manual
Decimal Adjust for Subtraction	DAS	0AA		1/1	See instruction manual
Negative of A	NEGA	060		1/1	A ← $\overline{A}$ + 1
Complement of B	NOTB	240		1/1	B ← $\overline{B}$
Rotate A to right with CY	RORC	0A0		1/1	Rotate A to right with CY
Rotate A to left with CY	ROLC	0A1		1/1	Rotate A to left with CY
Set CY	SC	0EF		1/1	CY ← 1
Reset CY	RC	0EC		1/1	CY ← 0
Test CY	TC	06F	CY	1/1	SF ← CY
Add Memory to A	AAM	004	OVF	1/1	A ← A + M
Add direct Memory to A	AAMD addr	204 d	OVF	2/2	A ← A + M (direct)
Add Memory to A with CY	AAMC	014	OVF	1/1	A ← A + M + CY, CY ← OVF
Add direct Memory to A with CY	AAMCD addr	214 d	OVF	2/2	A ← A + M (direct) + CY, CY ← OVF
Subtract A from Memory with CY	MSAC	094	NB	1/1	A ← M – A - $\overline{CY}$, CY ← NB
Subtract A from direct Memory with CY	MSACD	294 d	NB	2/2	A ← M (direct) - A - $\overline{CY}$, CY ← NB
OR A with B	ORB	248		1/1	A ← A OR B
AND A with Memory	ANDM	09C	NZ	1/1	A ← A AND M
AND A with direct Memory	ANDMD addr	29C d	NZ	2/2	A ← A AND M (direct)
OR A with Memory	ORM	00C	NZ	1/1	A ← A OR M
OR A with direct Memory	ORMD addr	20C d	NZ	2/2	A ← A OR M (direct)
XOR A with Memory	XORM	01C	NZ	1/1	A ← A XOR M
XOR A with direct Memory	XORMD addr	21C d	NZ	2/2	A ← A XOR M (direct)

5. Control Instructions

5a. Branch Instruction

Operation	Mnemonic	Code	SF	W/C	Function
Short branch on status flag = 1	BR addr	300 + x	1	1/1	if SF = 0 then PC ← PC + 1 else PC ← ((PC+1) & 3F00) + x
Long branch on status flag = 1	LBR addr	270 + k d	1	2/2	Branch if status = 1
Long jump	JMP addr	250 + k d		2/2	Unconditional jump for long distant
Table jump	TJMP p	0B0 + p		1/1	Unconditional jump with variable address assigned by register A, B and constant p

5b. Subroutine Stack Control Instruction

Operation	Mnemonic	Code	SF	W/C	Function
Zero-page subroutine call on status (Please refer to ROM MAP)	CAL addr	2C0 + a	1	1/2	Call subroutine if SF = 1
				1/1	Next instruction if SF = 0
Subroutine call on status	CALL addr	260 + k d	1	2/2	Call subroutine if SF = 1
Return from subroutine	RET	010		1/3	Recovers the previous address (PC_{N-1}) from stack and return to the upper level routine
Return from interrupt service	RETI	011	SF_{N-1}	1/3	IE ← 1, recovers the previous CY, SF and address (CY_{N-1}, SF_{N-1} & PC_{N-1}) from stack and return to the upper level routine

5c. CPU Control Instruction

Operation	Mnemonic	Code	SF	W/C	Function
No operation	NOP	000		1/1	No operation
HALT mode	HALT	24C		1/1	Enter Halt Mode
STOP mode	STOP	24D		1/1	Enter Stop Mode
Start serial transmission	STS	244		1/1	Enter Serial Transmission

5d. Table Data Generation Instruction

Operation	Mnemonic	Code	SF	W/C	Function
Table pattern generation	T p	2B0 + p		1/2	Extract the ROM data from the address assigned by register A, B and constant p

Application Circuit (for reference only)

■ 40-pins DIP connector assignment of OTP writer LP-10

Pin No.	Designation
1	VPP
2	XIN
3	
4	
5	VPX
6	
7	
8	RESET
9	PDAT9
10	PDAT8
11	GND
12	PDAT7
13	PDAT6
14	PDAT5
15	PDAT4
16	PDAT3
17	PDAT2
18	PDAT1
19	PDAT0
20	OEB

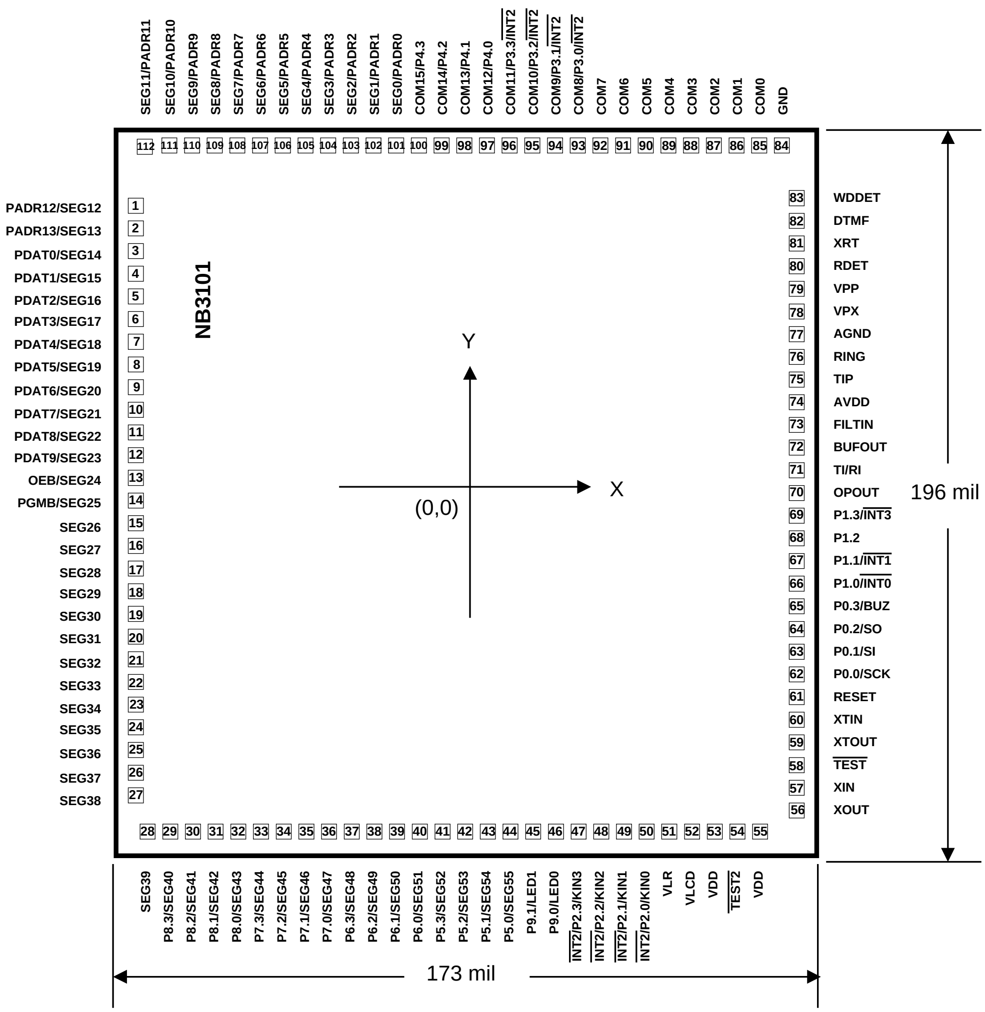
Pin No.	Designation
40	VDD
39	PGMB
38	TEST
37	TEST2
36	
35	PADR13
34	PADR12
33	PADR11
32	PADR10
31	PADR9
30	GND
29	PADR8
28	PADR7
27	PADR6
26	PADR5
25	PADR4
24	PADR3
23	PADR2
22	PADR1
21	PADR0

Ordering Information

Part No.	Package
SH93P423AH	CHIP FORM
SH93P423AF	128 QFP

Bonding Diagram

Chip size (X * Y)	= (173.2mils * 195.6mils)
Pad pitch (min, max)	= (120, 140µm)
Pad size	= 100µm * 100µm
Chip thickness	= 20mils or 25mils
Substrate polarity	= GROUND

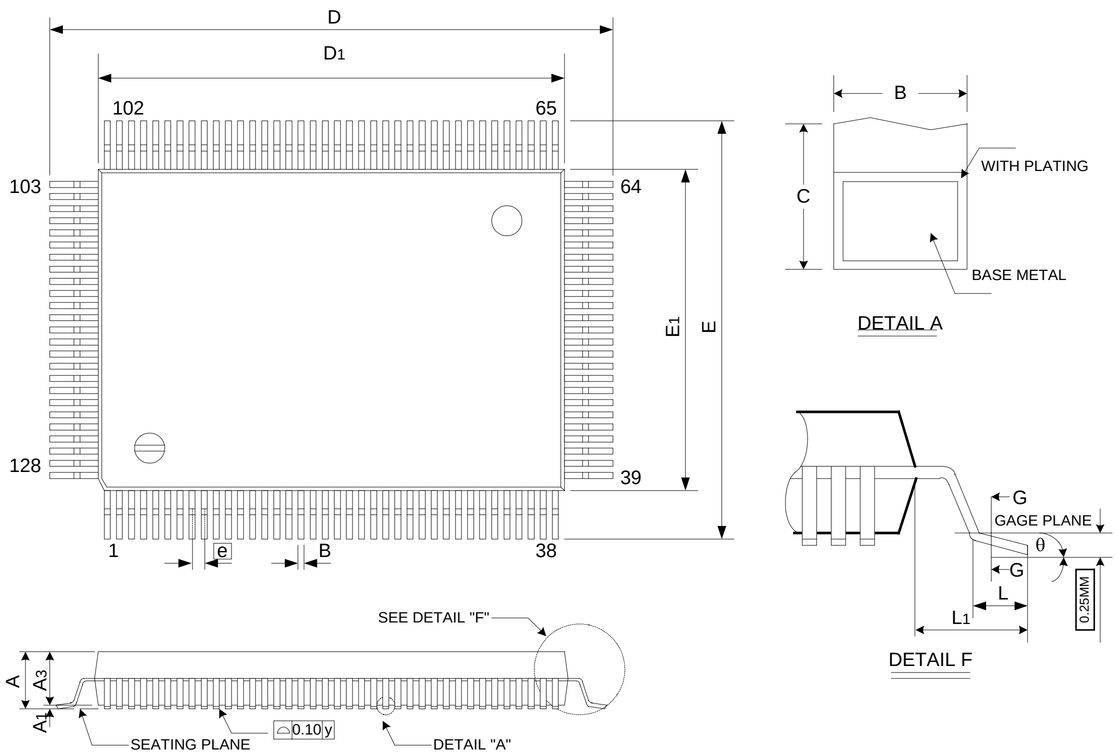


Note: For pad assignment, please refer to the following page.

Pad #	Primary Name	X coordinate	Y-coordinate	Pad #	Primary Name	X coordinate	Y-coordinate
1	SEG12	-2056.5	2103.8	57	XIN	2056.5	-2119.05
2	SEG13	-2056.5	1903.8	58	TEST	2056.5	-1969.05
3	SEG14	-2056.5	1703.8	59	XTOUT	2056.5	-1819.05
4	SEG15	-2056.5	1543.8	60	XTIN	2056.5	-1674.05
5	SEG16	-2056.5	1383.8	61	RESET	2056.5	-1539.05
6	SEG17	-2056.5	1223.8	62	P0.0	2056.5	-1404.05
7	SEG18	-2056.5	1063.8	63	P0.1	2056.5	-1269.05
8	SEG19	-2056.5	903.8	64	P0.2	2056.5	-1134.05
9	SEG20	-2056.5	743.8	65	P0.3	2056.5	-999.05
10	SEG21	-2056.5	583.8	66	P1.0	2056.5	-864.05
11	SEG22	-2056.5	423.8	67	P1.1	2056.5	-729.05
12	SEG23	-2056.5	263.8	68	P1.2	2056.5	-594.05
13	SEG24	-2056.5	103.8	69	P1.3	2056.5	-459.05
14	SEG25	-2056.5	-56.2	70	OPOUT	2056.5	-324.05
15	SEG26	-2056.5	-216.2	71	TI/RI	2056.5	-189.05
16	SEG27	-2056.5	-376.2	72	BUFOUT	2056.5	-54.05
17	SEG28	-2056.5	-536.2	73	FILTIN	2056.5	80.95
18	SEG29	-2056.5	-696.2	74	AVDD	2056.5	215.95
19	SEG30	-2056.5	-856.2	75	TIP	2056.5	391.4
20	SEG31	-2056.5	-1016.2	76	RING	2056.5	591.4
21	SEG32	-2056.5	-1176.2	77	AGND	2056.5	791.4
22	SEG33	-2056.5	-1336.2	78	VPX	2045.3	991.4
23	SEG34	-2056.5	-1496.2	79	VPP	2045.3	1250.1
24	SEG35	-2056.5	-1656.2	80	RDET	2056.5	1533.8
25	SEG36	-2056.5	-1816.2	81	XRT	2056.5	1703.8
26	SEG37	-2056.5	-1976.2	82	DTMF	2056.5	1903.8
27	SEG38	-2056.5	-2193.65	83	WDDET	2056.5	2103.8
28	SEG39	-2002.4	-2339.15	84	GND	1977	2339.2
29	P8.3/SEG40	-1782.4	-2339.15	85	COM0	1807	2339.2
30	P8.2/SEG41	-1597.4	-2339.15	86	COM1	1652	2339.2
31	P8.1/SEG42	-1442.4	-2339.15	87	COM2	1497	2339.2
32	P8.0/SEG43	-1292.4	-2339.15	88	COM3	1347	2339.2
33	P7.3/SEG44	-1152.4	-2339.15	89	COM4	1207	2339.2
34	P7.2/SEG45	-1017.4	-2339.15	90	COM5	1067	2339.2
35	P7.1/SEG46	-882.4	-2339.15	91	COM6	927	2339.2
36	P7.0/SEG47	-745.4	-2339.15	92	COM7	787	2339.2
37	P6.3/SEG48	-610.4	-2339.15	93	COM8	647	2339.2
38	P6.2/SEG49	-475.4	-2339.15	94	COM9	507	2339.2
39	P6.1/SEG50	-340.4	-2339.15	95	COM10	367	2339.2
40	P6.0/SEG51	-205.4	-2339.15	96	COM11	227	2339.2
41	P5.3/SEG52	-70.4	-2339.15	97	COM12	87	2339.2
42	P5.2/SEG53	64.6	-2339.15	98	COM13	-53	2339.2
43	P5.1/SEG54	199.6	-2339.15	99	COM14	-193	2339.2
44	P5.0/SEG55	334.6	-2339.15	100	COM15	-333	2339.2
45	P9.1/LED1	469.6	-2339.15	101	SEG0	-473	2339.2
46	P9.0/LED0	604.6	-2339.15	102	SEG1	-613	2339.2
47	P2.3	739.55	-2339.15	103	SEG2	-753	2339.2
48	P2.2	874.55	-2339.15	104	SEG3	-893	2339.2
49	P2.1	1009.55	-2339.15	105	SEG4	-1033	2339.2
50	P2.0	1139.55	-2339.15	106	SEG5	-1173	2339.2
51	VLR	1269.55	-2339.15	107	SEG6	-1313	2339.2
52	VLCD	1422.5	-2339.15	108	SEG7	-1453	2339.2
53	VDD	1575.45	-2339.15	109	SEG8	-1593	2339.2
54	TEST2	1733.9	-2339.15	110	SEG9	-1738	2339.2
55	VDD	1892.35	-2339.15	111	SEG10	-1883	2339.2
56	XOUT	2056.5	-2284.05	112	SEG11	-2028	2339.2

Package Information

QFP 128L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.134	--	--	3.40
A1	0.010	--	--	0.25	--	--
A2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	--	0.008	0.09	--	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.667	0.685	17.00	17.20	17.40
E1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L1	0.063 BSC			1.60 BSC		
Y	--	--	0.004	--	--	0.10
θ	0°	--	7°	0°	--	7°

Notes:
1.Dimensions D & E do not include resin fins.
2.Dimensions F are for reference of surface mount PC Board design only.

Revision History

Version 0.1

- Preliminary specification

Version 1.0

- **Features**
  Power System
  - Operating voltage range: For CPU: 2.8V to 5.5V

- **Pad Configuration**
  Pad 78: VPX
  Pad 79: VPP

- **Pin Configuration**
  Pin 90: VPX
  Pin 92: VPP

- **Pad Description**
  Pad 78: VPX
  Pad 79: VPP

- **OTP Operation**: OTP mode selection table
- **40-pins DIP connector assignment of OTP writer LP-10**
- **Pad X-Y coordinates**
  Pad 78: VPX
  Pad 79: VPP
- **DC Electrical Characteristics**
  V_{CPU}: 2.8V to 5.5V

Version 1.01

- **Package Information**

Version 1.04

- **Drive/Sink current of general output pins for Port3 and Port4**

Drive/Sink current of general output pins	I_{OH2}	1.0	2.0		mA	V_{OH} = 4.0V, V_{OL} = 0.6V Port3 and Port4
	I_{OL2}	–1.5	–2.0		mA	