THIS DOCUMENT IS FOR MAINTENANCE PURPOSES ONLY AND IS NOT RECOMMENDED FOR NEW DESIGNS

SL6442

1GHZ AMPLIFIER/MIXER

(Supersedes May 1992 Edition)

The SL6442 UHF Amplifier and Mixer is designed for use in cordless telephones, cellular telephones, pagers and low-power receivers operating at frequencies up to 1GHz. It contains a low noise amplifier (LNA) with AGC facility and two mixers for use in I and Q direct conversion receivers or image cancelling in superheterodyne receivers.

Operating from a single supply of 5V, the SL6442 requires a current of 4.6mA (typ.) when powered up and only 11µA (typ.) when powered down using the battery economy facility.

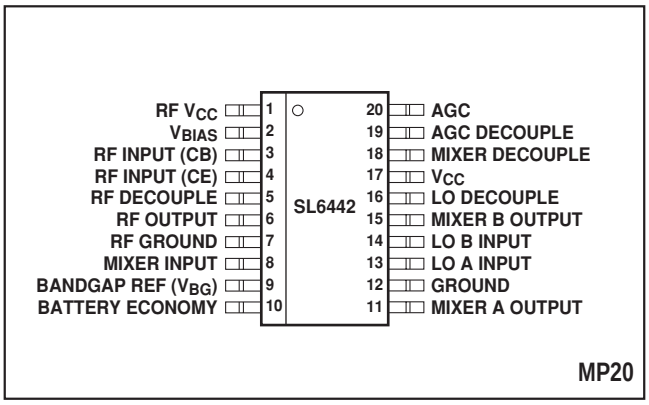


Fig.1 Pin connections - top view

FEATURES

- 1GHz Operation
- Very Low Power
- Suitable for Direct Conversion or Superhet Systems
- On-Chip RF Amplifier
- Power Down Facility for Battery Economy
- AGC Capability

ORDERING INFORMATION

SL6442 NA MP Miniature Plastic DIL Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	−55°C to+150°C
Operating temperature	0°C to +70°C

This device has static-sensitive terminations, sensitivity measured as typically 400V using MIL-STD-883 Method 3015. Therefore, ESD handling precautions are essential in order to avoid degradation of performance or permanent damage to the device.

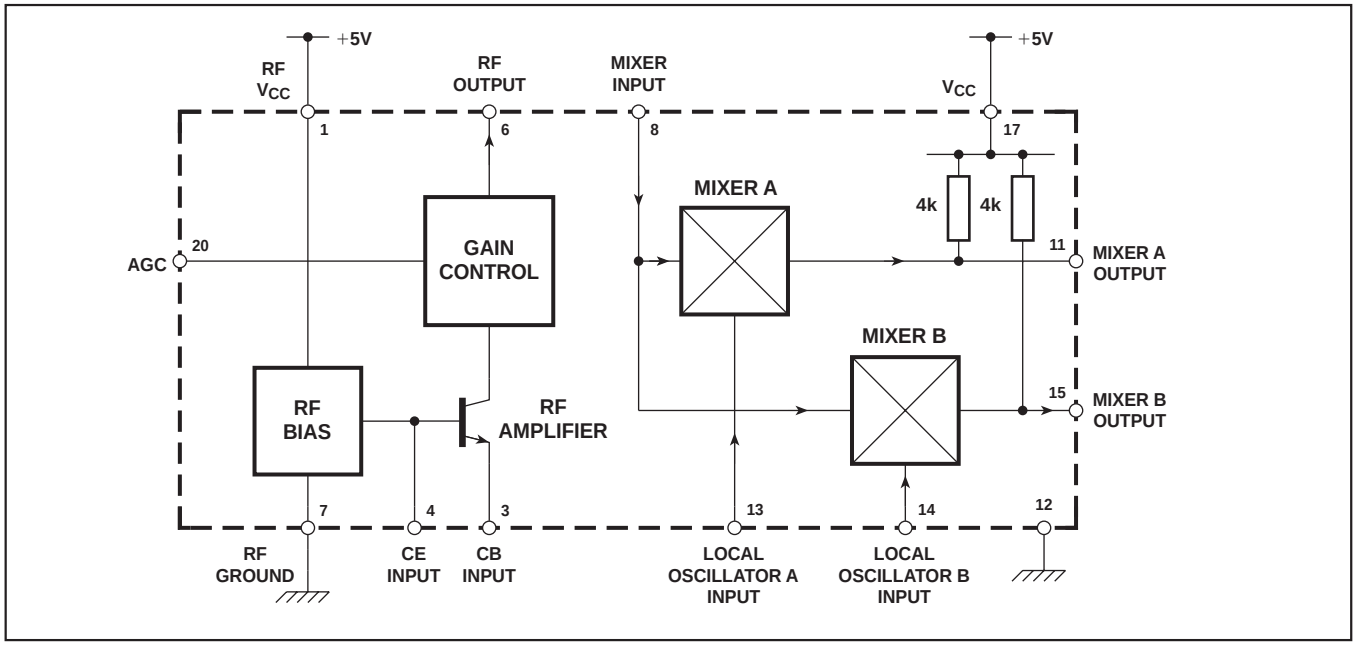


Fig.2 block diagram

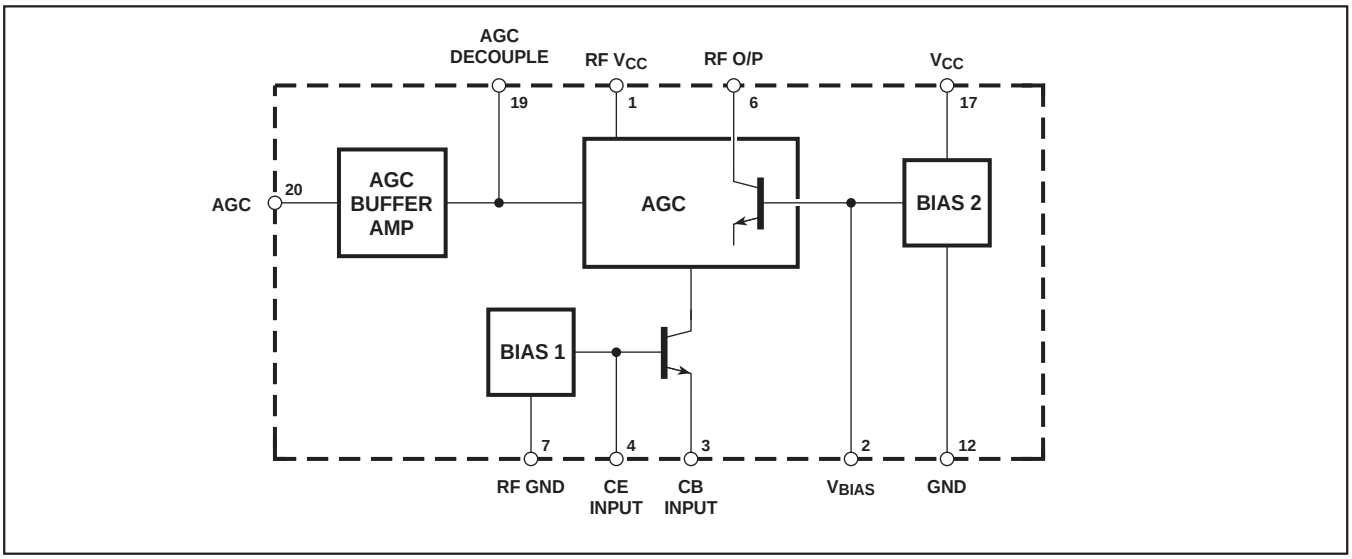


Fig.3 Circuit schematic of LNA

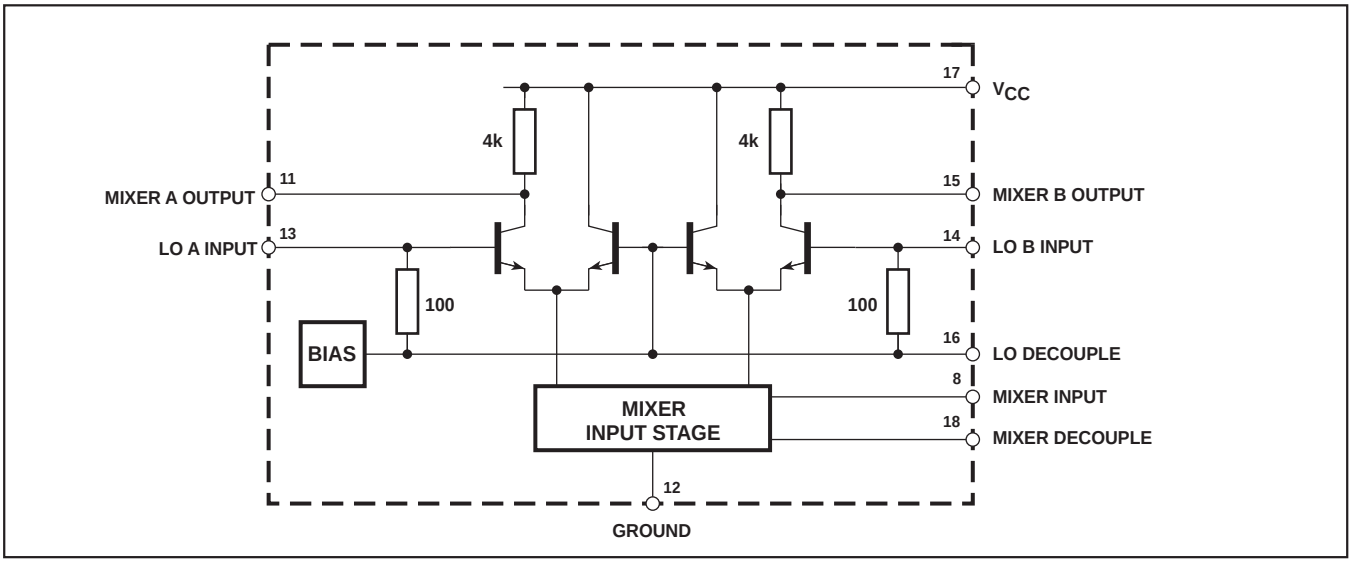


Fig.4 Circuit schematic of mixer

PIN DESCRIPTIONS

Pin no.	Name	Description
1	RF V_{CC}	Power supply to the RF amplifier. Normally connected to +5V, it should be adequately bypassed.
2	V_{BIAS}	A 1·6V bias source capable of supplying up to 0·5mA.
3	RF input (CB)	Common base input to the emitter of the RF transistor. It should be returned to ground for DC using an RF choke or tuned circuit when in common base mode. In common emitter mode it should be connected directly to ground.
4	RF input (CE)	Common emitter input to the base of the RF transistor. It is DC biased internally but should be decoupled in common base mode.
5	RF decouple	Decoupling of DC bias line.
6	RF output	Output port of the RF amplifier. It should be returned to +5V via an RF load. A current of 2mA will flow if pin 20 (AGC) is connected to pin 9 (V_{BG}).

PIN DESCRIPTIONS (Continued)

Pin no.	Name	Description
7	RF ground	A separate ground is provided for the RF amplifier to improve stability.
8	Mixer input	This is coupled externally to the output of the RF amplifier (pin 6). It should be decoupled to V_{BIAS} via an RF choke.
9	Bandgap ref. (V_{BG})	Temperature compensated DC reference voltage. It should not be loaded.
10	Battery economy	Turns device 'off' when HIGH (>3V), 'on' when LOW (<1·5V).
11	Mixer A output	The output impedance is about 4kΩ; quiescent voltage is approximately 4V (V_{CC}=5V).
12	Ground	Mixer and biasing ground.
13	Local osc. A input	Input level of −10dBm. DC level is approximately 2·3V.
14	Local osc. B input	Input level of −10dBm. DC level is approximately 2·3V.
15	Mixer B output	The output impedance is about 4kΩ; quiescent voltage is approximately 4V (V_{CC}=5V).
16	LO decouple	Decoupling of DC bias line.
17	V_{CC}	+5V supply; it should be bypassed effectively.
18	Mixer decouple	Decoupling of DC bias line.
19	AGC decouple	Decoupling of AGC input line.
20	AGC	Varies RF amplifier gain. Gain reduces with increasing voltage, with RF gain reduced by 6dB when AGC=V_{BIAS}. Full range of AGC requires only typically 300mV DC range (see Fig. 9). This pin should be connected to V_{BG} if the AGC facility is not required.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:

T_{AMB}=25°C, V_{CC}=4·5V and at V_{CC}=6·5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Total supply current	1, 6, 11, 15, 17	3·5	4·6	5·5	mA	Pin 10 at 0V
Total supply current (economised)	1, 6, 11, 15, 17		11·0	15·0	µA	Pin 10 at V_{CC}
Battery economiser input current	10	−1·0		+1·0	µA	
Total RF amplifier current	1, 5		2·0	2·75	mA	
Maximum RF amplifier current	6		2·0	2·75	mA	V_{AGC} =1·2V
Minimum RF amplifier current	6			10·0	µA	V_{AGC} =2·0V
AGC amplifier offset voltage	20, 19	−20·0	0	+20·0	mV	
Bandgap voltage, V_{BG}	9	1·00	1·23	1·40	V	
V_{BIAS}	2	1·40	1·64	1·80	V	
V_{BIAS} supply regulation	2		+24·0	+50	mV	Step V_{CC} from 4·50V to 5·50V,
V_{BIAS} load regulation	2		−17·0	−50	mV	Step load from 0mA to 0·5mA,
Mixer conversion gain	11, 15	10·0	12·7	16·0	dB	$f_{CARRIER}$=50MHz at −10dBm, f_{SIGNAL}=50·01MHz at −34dBm, IF=10kHz, Z_L (EXT)=1MΩ//20pF
Mixer A/B gain match	11, 15	−1·0	0	+1·0	dB	$f_{CARRIER}$=50MHz at −10dBm, f_{SIGNAL}=50·01MHz at −34dBm, IF=10kHz, Z_L (EXT)=1MΩ//20pF

NOTE: Typical figures are for a V_{CC} of 5·0V

ELECTRICAL CHARACTERISTICS OF THE SL6442 DEMONSTRATION BOARD (PAGES 8-10)

These characteristics are guaranteed over the following conditions unless otherwise stated:

T_{AMB} = 25° C, V_{CC} =5·0V, V_{AGC} = V_{BG}, LO = −5dBm, Input/Output = 50Ω, f_{IN} = 950MHz, f_{LO} = 930MHz (IF = 20MHz), f_{LO} = 949·990MHz (IF = 10kHz)

Overall performance	Typ.	Units	Conditions
Noise figure	8·3	dB	DSB (20MHz IF)
Third order input intercept	−22	dBm	20MHz IF
Power gain	7·5	dB	20MHz IF
Voltage gain	30	dB	Z_L > 100kΩ , IF = 10kHz

NOTE: Refer to Figs. 5, 6 and 7 for typical performance of overall low noise amplifier and mixer configuration (demonstration board) across temperature and supply voltage 4·0V, 5·0V and 7·0V).

SUPPLEMENTARY INFORMATION

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage range		4·5	5·0	6·5	V	
RF Amplifier Common emitter						
Power gain			14		dB	Matched input and output.
AGC range	20		25		dB	V_{BIAS} ±150mV typ. (see Fig. 9).
Input intercept			−9		dBm	Third order.
1dB gain compression			−23		dBm	At input
Noise figure			4·5		dB	Common emitter.
Input impedance						See Fig. 8.
Optimum operating frequency range	4	400		1000	MHz	
Mixers (950MHz)						
Voltage conversion gain			19		dB	At IF = 50kHz, matched input.
Power conversion gain			−7		dB	At IF = 20kHz. Matched input and output.
LO drive level	13,14		−10		dBm	Measured at pins 13 and 14.
Input intercept point	8		−6		dBm	Third order.
1dB gain compression			−12		dBm	At input
Mixer 'A' to Mixer 'B' gain input match				±1·0	dB	Equal LO level at pins 13 and 14
Mixer 'A' to Mixer 'B' phase input match				±4	deg	LO inputs 90 ± 0·1° phase
Input impedance						See Fig. 10.
Noise figure			21		dB	
Optimum operating frequency range	8			1000	MHz	Low frequency operation dependent on external components.
IF output bandwidth	11,15		20		MHz	Can be extended by external tuned circuit.
Output impedance			4		kΩ	
Isolation LO to mix RF I/P		25			dB	All ports terminated with 50Ω
Reverse isolation of RF amp		14			dB	All ports terminated with 50Ω
Isolation LO to IF		50			dB	All ports terminated with 50Ω
Isolation RF to IF		37			dB	All ports terminated with 50Ω

PERFORMANCE CHARACTERISTICS OF THE SL6442 DEMONSTRATION BOARD

Test conditions:

Input frequency = 950MHz, LO frequency = 930MHz, LO amplitude = −5dBm, intermediate frequency = 20MHz, $V_{AGC} = V_{BG}$, input/output 50Ω matched.

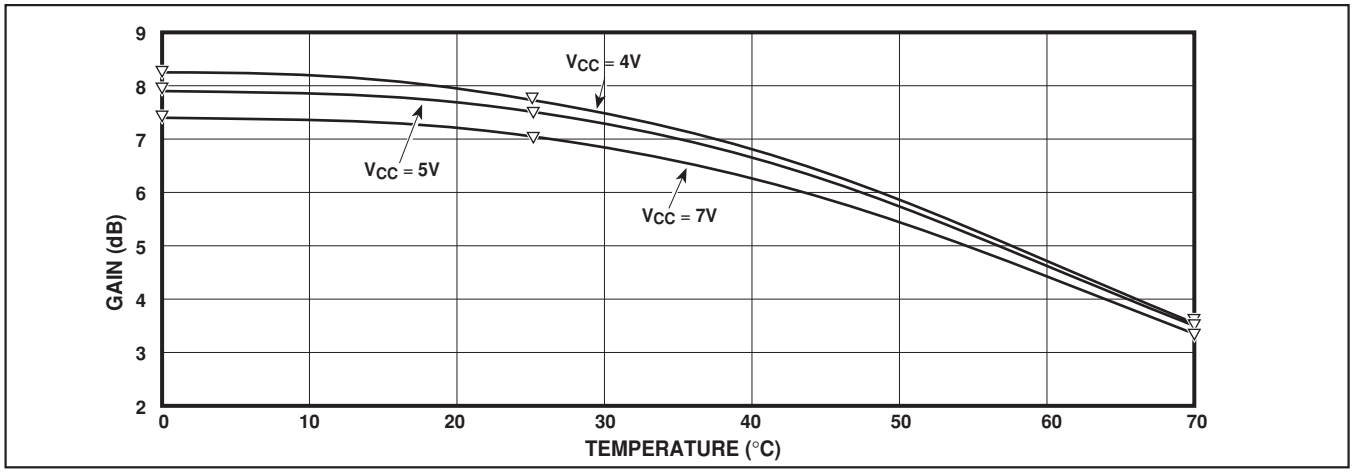


Fig. 5 Typical overall power gain

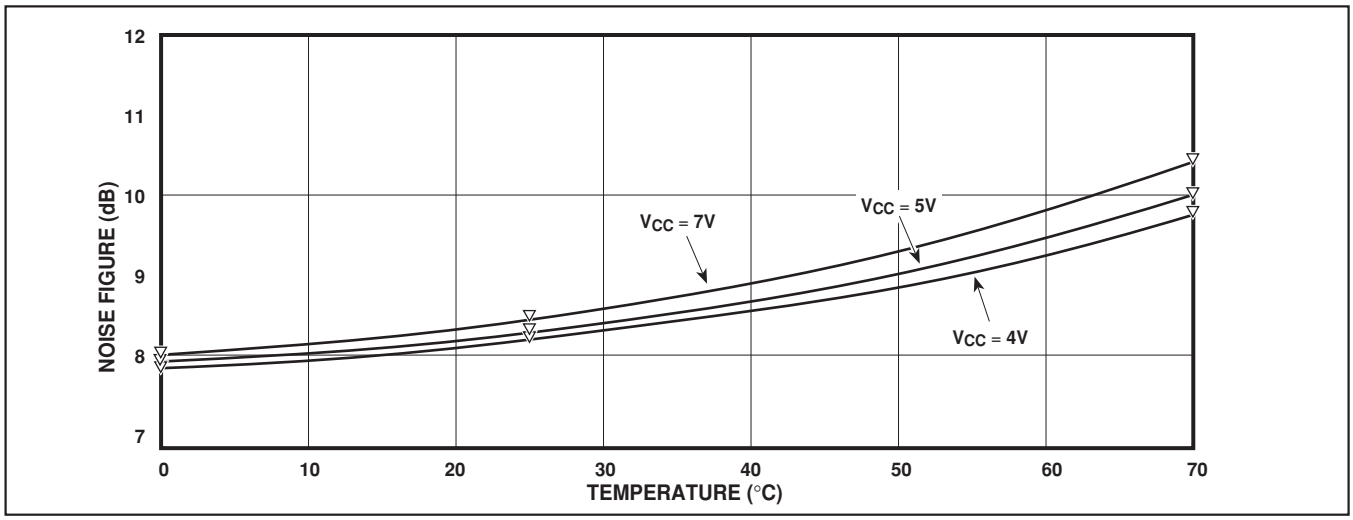


Fig. 6 Typical overall noise figure

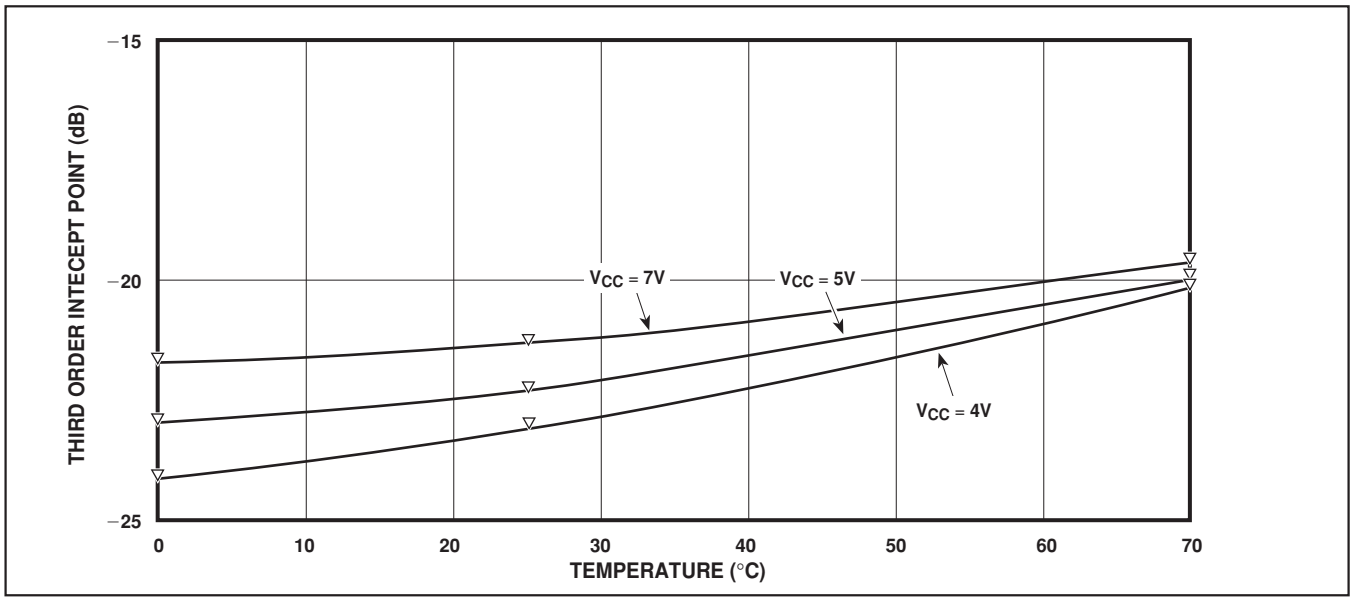
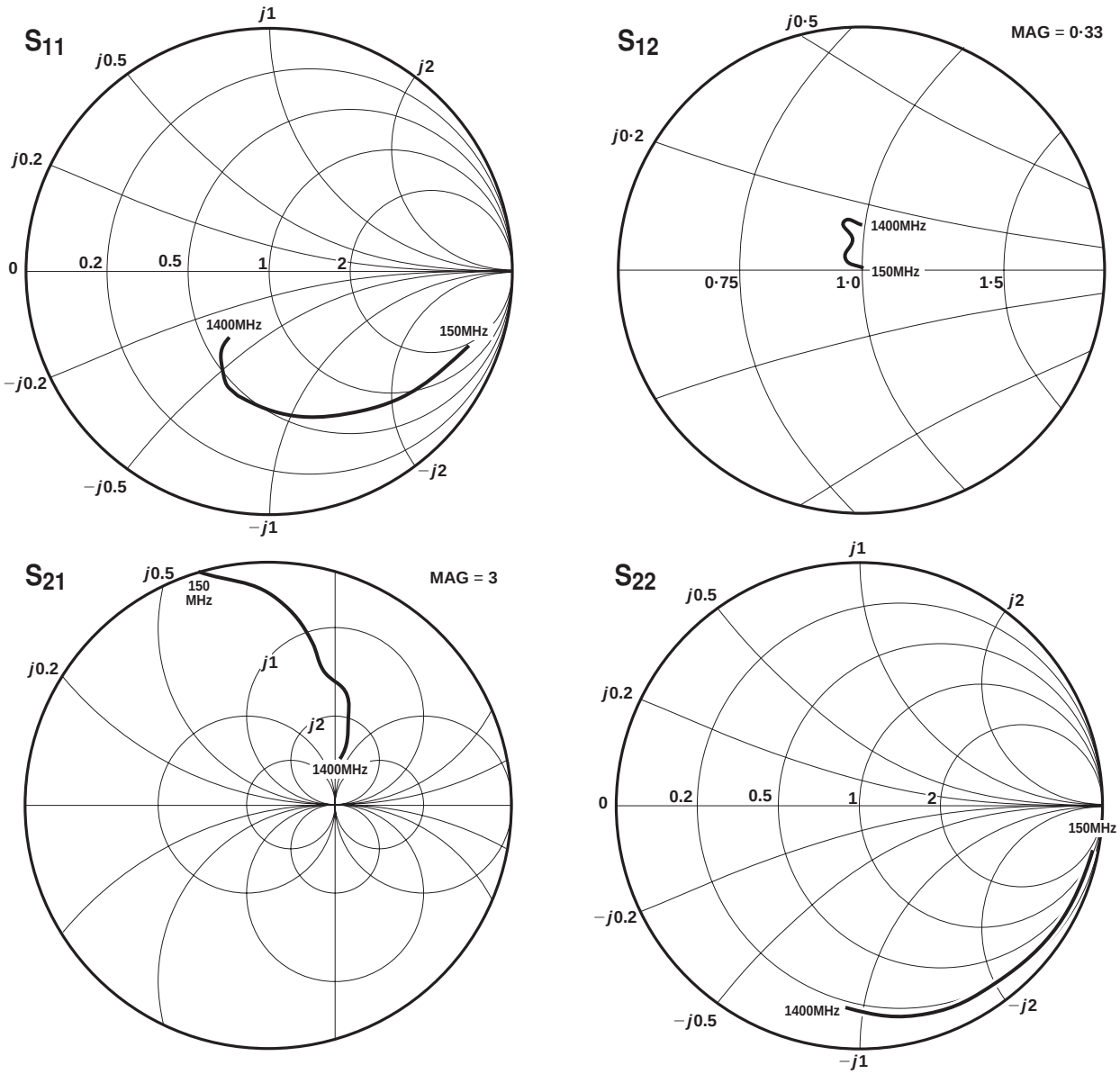


Fig. 7 Typical overall third order intercept



	S_{11}		S_{12}		S_{21}		S_{22}	
f (MHz)	Mag.	Ang. (°)	Mag.	Ang. (°)	Mag.	Ang. (°)	Mag.	Ang. (°)
150	0·869	−22·1	0·006	69·0	5·126	149·7	0·994	−11·3
200	0·829	−28·5	0·002	134·0	4·763	138·6	0·991	−15·5
300	0·765	−40·1	0·008	111·8	4·140	121·9	0·986	−22·7
400	0·712	−49·2	0·004	131·2	3·567	108·8	0·967	−29·5
500	0·679	−57·7	0·010	138·1	3·123	96·6	0·963	−36·7
600	0·640	−66·5	0·019	140·3	2·672	87·7	0·945	−44·0
700	0·608	−74·0	0·027	143·7	2·428	79·2	0·921	−49·8
800	0·582	−82·2	0·036	130·8	2·197	71·7	0·909	−54·7
900	0·561	−90·4	0·041	118·7	1·935	62·4	0·912	−59·8
1000	0·531	−100·0	0·043	113·5	1·729	56·3	0·913	−66·4
1100	0·496	−114·0	0·063	115·9	1·636	47·2	0·885	−74·6
1200	0·401	−118·5	0·050	100·0	1·512	41·4	0·877	−80·2
1300	0·334	−120·6	0·050	98·1	1·385	34·3	0·853	−87·6
1400	0·304	−117·8	0·049	97·0	1·208	28·4	0·824	−95·2

Fig. 8 RF amplifier common emitter S-parameters

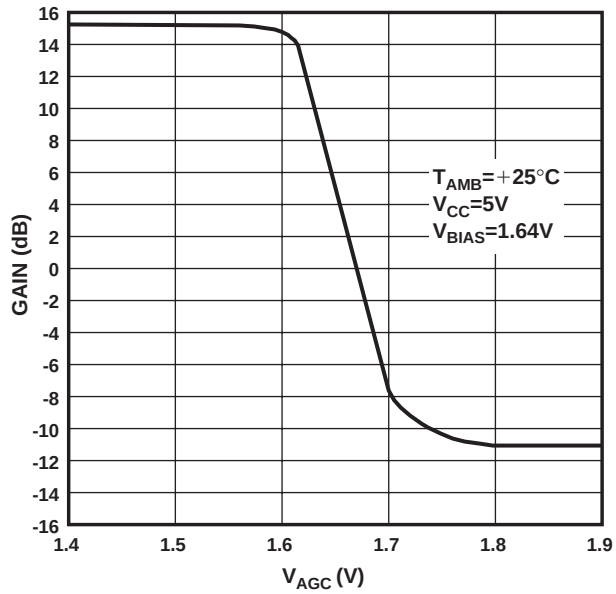
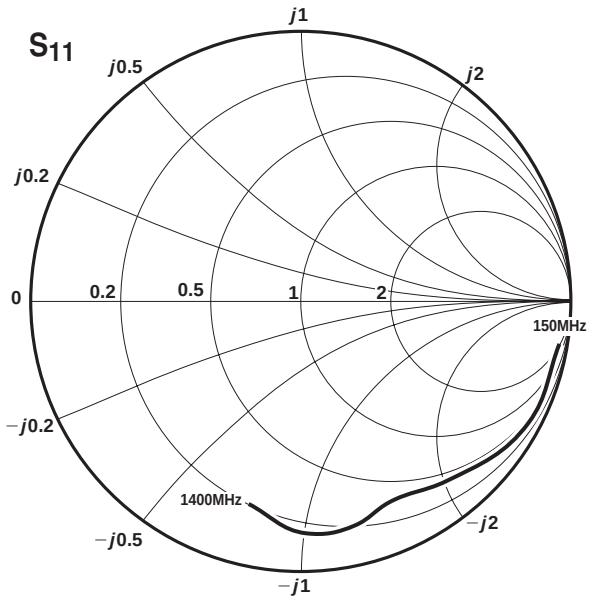


Fig. 9 SL6442 AGC characteristic



f (MHz)	Mag.	Ang. (°)
150	0·967	−12·1
200	0·967	−15·9
300	0·949	−24·5
400	0·960	−30·0
500	0·922	−39·3
600	0·887	−46·3
700	0·868	−53·0
800	0·836	−58·8
900	0·826	−63·6
1000	0·849	−70·4
1100	0·866	−78·6
1200	0·856	−88·5
1300	0·817	−98·2
1400	0·768	−107·3

Fig. 10 Mixer RF input impedance, S_{11} (pin 8)

APPLICATION CIRCUIT FOR USE AT 950MHz

This Application Note describes a circuit which demonstrates the functions and performance of the SL6442 in a 950MHz amplifier/mixer receiver front end configuration.

Fig. 11 is a schematic diagram which illustrates the arrangement of the ancillary components required for optimum performance at 950MHz. Component layout, PCB track and ground plane are shown in Figs. 12, 13 and 14, respectively. Approximate starting values for the components were obtained using Smith charts and data derived from S-parameter analysis (see Figs. 8 and 10).

The actual component values were determined by using a linear circuit simulator such as Touchstone™. In this case the circuit is optimised for maximum stable gain and minimum input reflection coefficient at the required frequency.

The input match is achieved using a stripline shorted-stub network. The LNA output to mixer input match is achieved by using a series inductor, and the mixer output to 50Ω match consists of a tunable LC network.

To prevent possible RF instability, pin 2 (V_{BIAS}) is decoupled with a series RC network as well as a 2·2µF capacitor. The quadrature phase shift components consist of phase lead (R3, C18) and phase lag (R2, C17) networks, which are capacitively coupled to the LO input pins. Inductor L3 serves to resonate out the parasitic capacitance between the two ports.

The exact values of the phase shift components were determined empirically and achieve a maximum amplitude and phase imbalance of about 1dB and 4 degrees respectively.

The variable capacitors VC1 and VC2 are adjusted to give a maximum output level at an IF of 20MHz. Other intermediate frequencies may require different values of VC1 and VC2 and/or L4 and L5. At zero IF, as in direct conversion receivers, the output matching network is transparent.

If the AGC facility is not required it is necessary to connect pin 20 to pin 9 (V_{BG}). The battery economy pin (10) may be connected directly to ground if the power down facility is not required.

NOTE: Ensure adequate decoupling is used close to the chip, especially when designing for maximum power gain. Refer to LNA S-parameters to avoid possible stability problems when designing the LNA close to maximum gain.

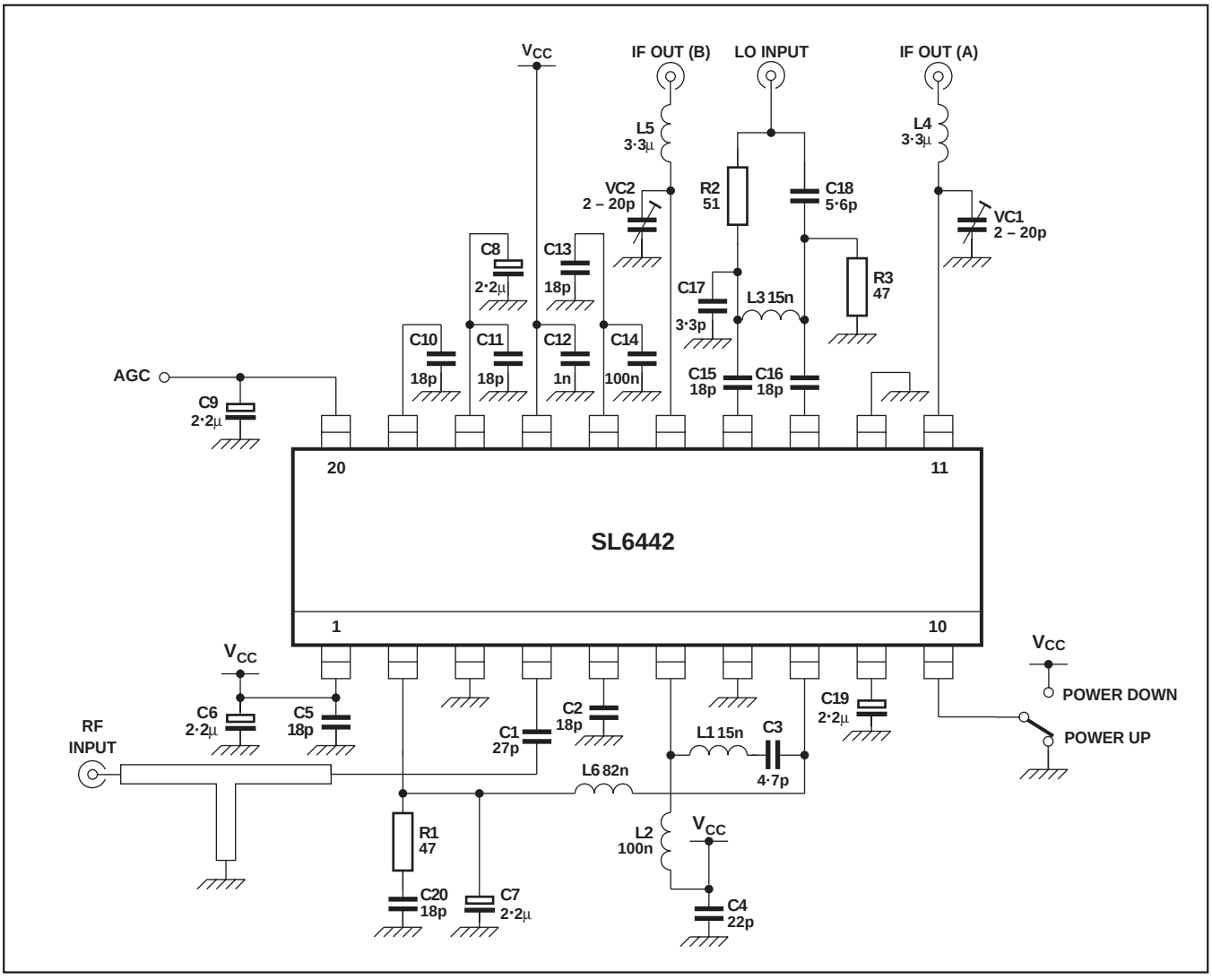
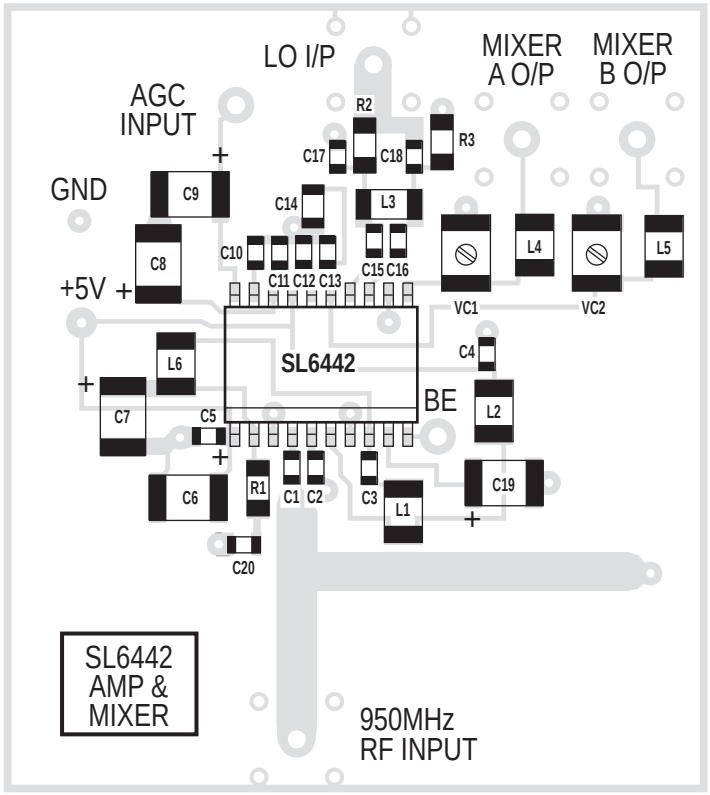


Fig. 11 SL6442 demonstration board circuit



COMPONENT LIST

R1, R3	47Ω
R2	51Ω
C1	27pF
C2,C5,C10, C11,C13, C15	18pF
C3	4·7p
C4, C6, C7,C8	22pF
C9, C19	2·2µF
C12	1nF
C14	100nF
C17	3·3pF
C18	5·6pF
L1, L3	15nH
L2	100nH
L4, L5	3·3µH
L6	82nH
VC1, VC2	2 - 20pF

Fig. 12 SL6442 demonstration board component layout. Scale=2 x full size. Input and output coaxial connectors are mounted on the ground plane side of the board.

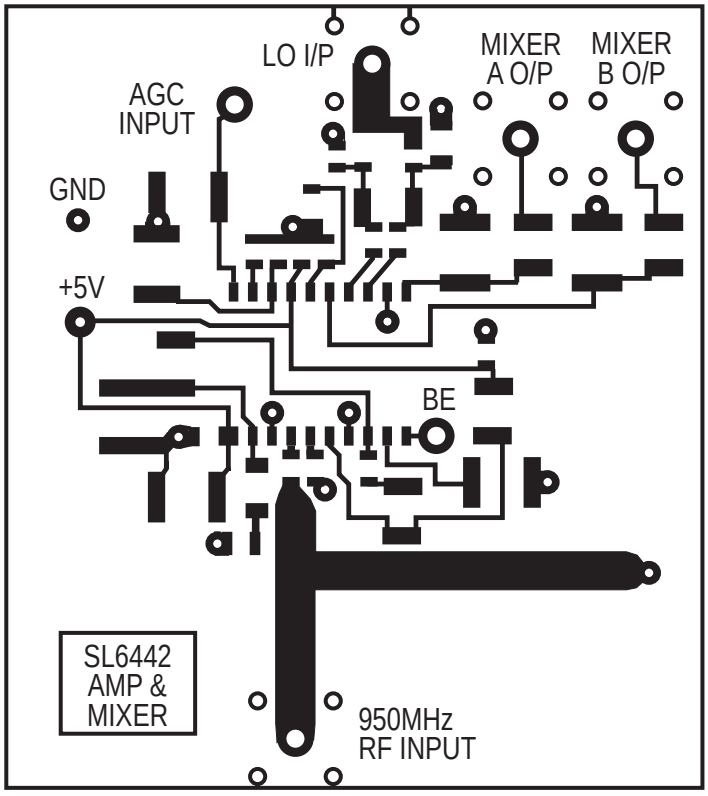


Fig. 13 SL6442 demonstration board track. Scale=2 x full size

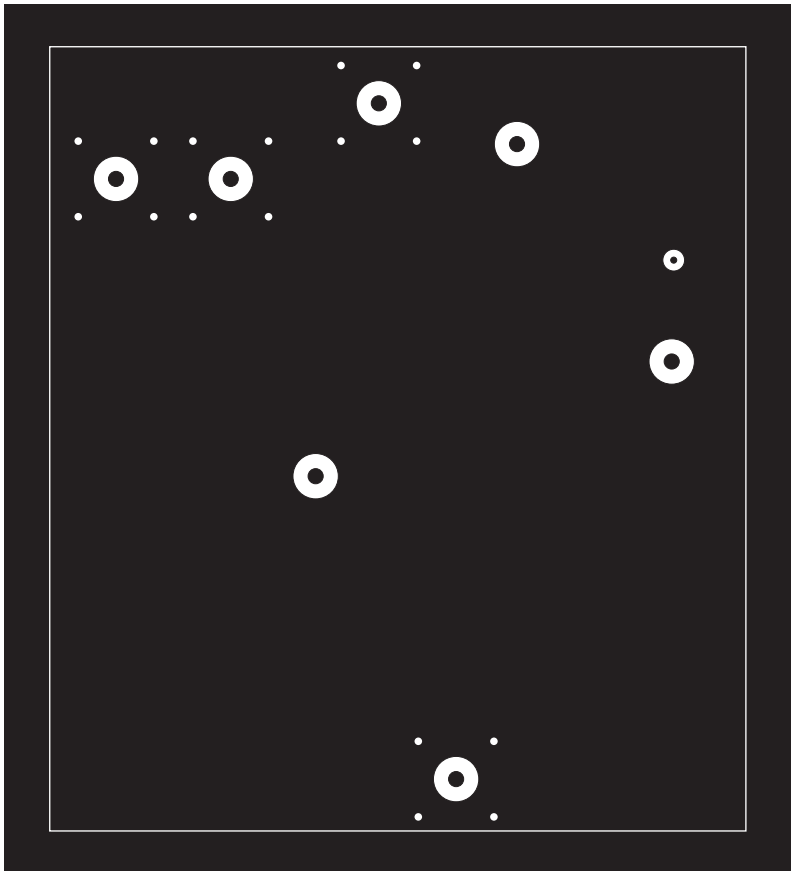
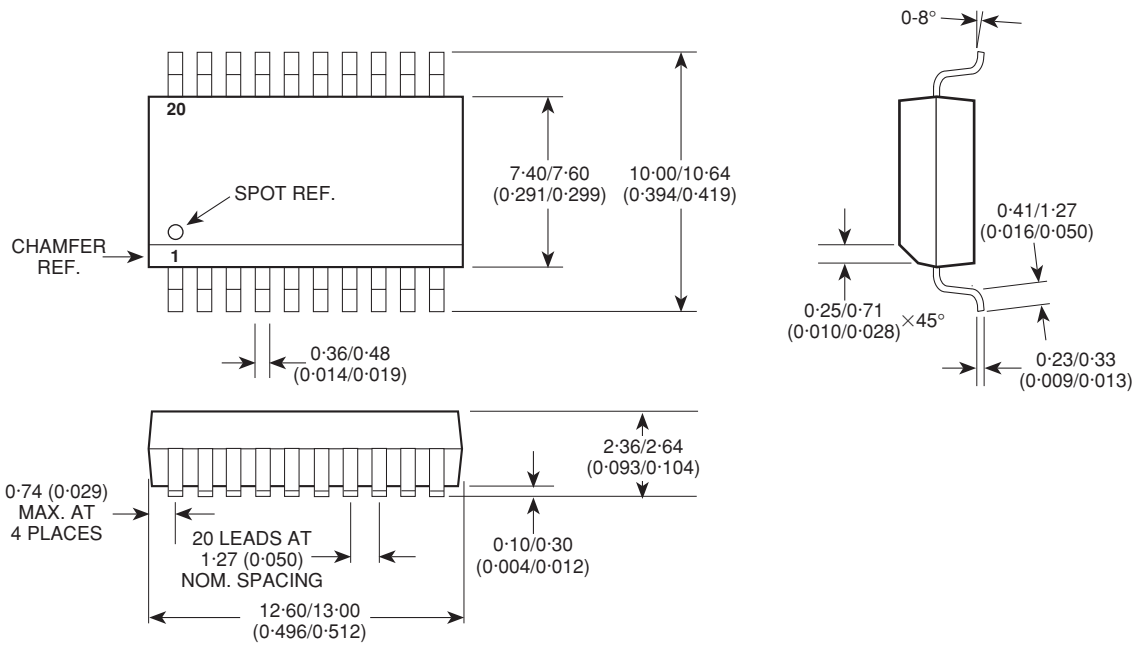


Fig. 14 SL6442 demonstration board ground plane. Scale=2 x full size.

CUSTOMER NOTES

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



20-LEAD MINIATURE PLASTIC DIL - MP20

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