PRELIMINARY

SFF450M
SFF450Z

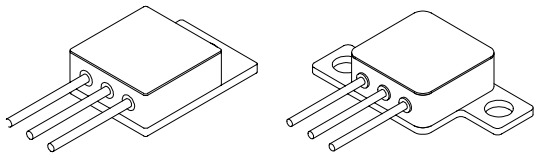
SOLID STATE DEVICES, INC.
14830 Valley View Blvd * La Mirada, Ca 90638
Phone: (562) 404-7855 * Fax: (562) 404-1773

DESIGNER'S DATA SHEET

13 AMPS
500 VOLTS
0.4Ω
N-CHANNEL
POWER MOSFET

FEATURES:
- Rugged construction with poly silicon gate
- Low RDS (on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available
- Replaces IRFM450 Types

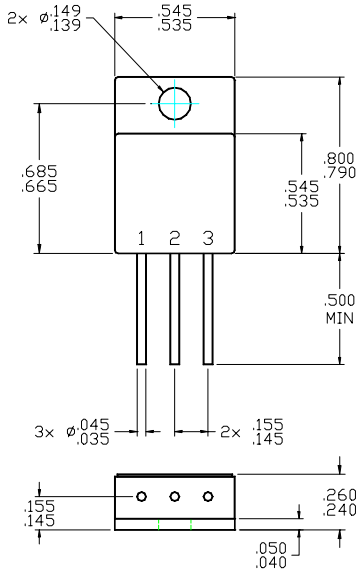
TO-254 (M) **TO-254Z (Z)**



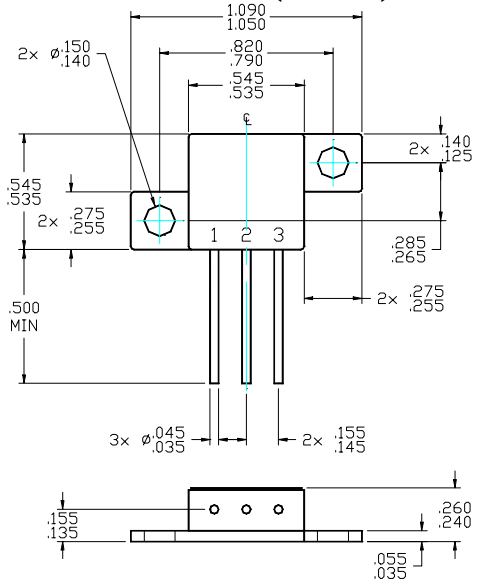
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V_{DS}	500	Volts
Gate to Source Voltage	V_{GS}	±20	Volts
Continuous Drain Current	I_D	13	Amps
Operating and Storage Temperature	T_{op} & T_{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Total Device Dissipation @ TC = 25°C @ TC = 55°C	P_D	125 95	Watts

CASE OUTLINE: TO-254 (Sufix M)



CASE OUTLINE: TO-254Z (Sufix Z)



For Pin Out Configuration and Optional Lead Bend See Page 2.

NOTE: All specifications are subject to change without notification.
SCDs for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00097D

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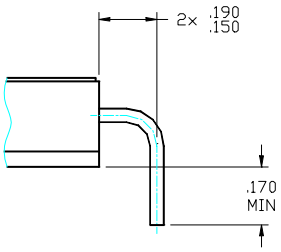
ELECTRICAL CHARACTERISTICS @ T_J =25°C (Unless Otherwise Specified)

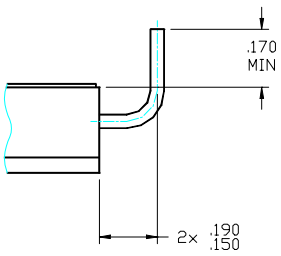
RATING		SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage (VGS =0 V, ID = 250µA)		**BV_{DSS}**	500	-	-	**V**
Drain to Source ON State Resistance (VGS = 10 V, ID = 7.2 A)		**$R_{DS(on)}$**	-	0.35	0.40	Ω
ON State Drain Current (VDS > ID(on) x RDS(on) Max, VGS = 10 V)		**$I_{D(on)}$**	13	-	-	**A**
Gate Threshold Voltage (VDS = VGS, ID = 250µA)		**$V_{GS(th)}$**	2.0	-	4.0	**V**
Forward Transconductance (VDS ≥ 50 V, IDS = 7.2 A)		**gf_s**	8.7	131	-	**S(℧)**
Zero Gate Voltage Drain Current (V_{DS} = max rated Voltage, V_{GS} = 0V) (V_{DS} = 80% rated V_{DS}, V_{GS} = 0V, T_A = 125°C)		**I_{DSS}**	- -	- -	250 1000	**µA**
Gate to Source Leakage Forward **Gate to Source Leakage Reverse**	At rated VGS	**I_{GSS}**	- -	- -	+100 -100	**nA**
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	VGS = 10 V 80% rated VDS Rated ID	**Qg** **Qgs** **Qgd**	- - -	83 11 42	120 17 64	**nC**
Turn on Delay Time **Rise Time** **Turn off DELAY Time** **Fall Time**	VDD =50% rated VDS 50% rated ID RG=6.2Ω, PD=20W	**$t_{d\ (on)}$** **tr** **$t_{d\ (off)}$** **tf**	- - - -	18 44 70 40	27 66 100 60	**nsec**
Diode Forvard Voltage (I_S = rated I_D, V_{GS} = 0V, T_J = 25°C)		**V_{SD}**	-	-	1.4	**V**
Diode Reverse Recovery Time **Reverse Recovery Charge**	TJ =25°C IF = rated ID di/dt = 100A/µsec	**t_{rr}** **Q_{RR}**	280 3.2	580 6.7	1200 14	**nsec** **µC**
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	VGS =0 Volts VDS =25 Volts f =1 MHz	**Ciss** **Coss** **Crss**	- - -	2700 350 75	- - -	**pF**

For thermal derating curves and other characteristic curves please contact SSDI Marketing Department.

OPTIONAL LEAD BEND CONFIGURATION



SUFIX MDB & ZDB



SUFIX MUB & ZUB

PIN ASSIGNMENT

CODE	Configuration	PIN 1	PIN 2	PIN 3
--	Standard	Drain	Source	Gate