Data Sheet, V1.3, Sep. 2002

TC11IB

32-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

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TC11IB
Advance Information
Revision History: 2002-09 V1.3

Previous Version: V1.1, 2002-03
V1.2, 2002-04

Page	Subjects (major changes since last revision)
24	V_{SS} pins are corrected.
76	SDRAM data input hold time is corrected.
65	CPU_ID address is corrected.

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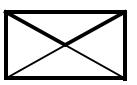


32-Bit Single-Chip Microcontroller **TC11IB**
TriCore Family

Advance Information

- High Performance 32-bit TriCore CPU with 4-Stage Pipeline running at 96MHz Clock
- Dual Issue super-scalar implementation
  - MAC Instruction maximum triple issue
- Circular Buffer and bit-reverse addressing modes for DSP algorithms
- Flexible multi-master interrupt system
- Very fast interrupt response time
- Hardware controlled context switch for task switch and interrupts
- Windows CE compliant Memory Management Unit (MMU)
- 64 kByte of on-chip SRAM for data and time critical code
- Independent Peripheral Control Processor (PCP) for low level driver support with 20 kByte code / parameter memory
- eDRAM Local Memory Unit (LMU) with 512 KBytes Code/data Memory.
- ComDRAM with 1MBytes DRAM Memory
- High Performance Local Memory Bus (LMB) for fast access between Caches and on-local memories and Fast-FPI Interface.
- Two On-chip Flexible Peripheral Interface Buses (Fast FPI Bus and Slow FPI Bus) for interconnections of functional units
- Flexible External Bus Interface Unit (EBU) used for communication with external data memories such as PC 100 SDRAM, Burst Flash and SRAM etc. and external peripheral units, including Intel style and Motorola style peripherals.
- On-Chip Peripheral Units
  - Two Multifunctional General Purpose Timer Units (GPTU0 & GPTU1) with three 32-bit timer/counters each
  - Asynchronous/Synchronous Serial Channels (ASC) with IrDA data transmission, receive/transmit FIFOs, parity, framing and overrun error detection
  - High Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Asynchronous Serial Interface (16X50) with programmable XON/XOFF characters, Baudrate generator, receive/transmit FIFOs and standard modem interface support.
  - 16 MHz MultiMediaCard Interface (MMCI), a glueless interface to MultiMediaCard Bus, with bus clock generation, CRC protection and up to 2 MByte/s data communication.
  - Fast Ethernet Controller with 10/100 Mbps MII-Based physical devices support.
  - PCI V2.2 Interface with PCI Bus Power Management and DMA data transfer.
  - Watchdog Timer and System Timer
- Six 16-bit digital I/O ports
- On-Chip Debug Support (OCDS)

- Power Management System
- Clock Generation Unit with PLL
- Ambient temperature under bias: -25 °C to +85 °C
- P-BGA-388-2 package

Block Diagram

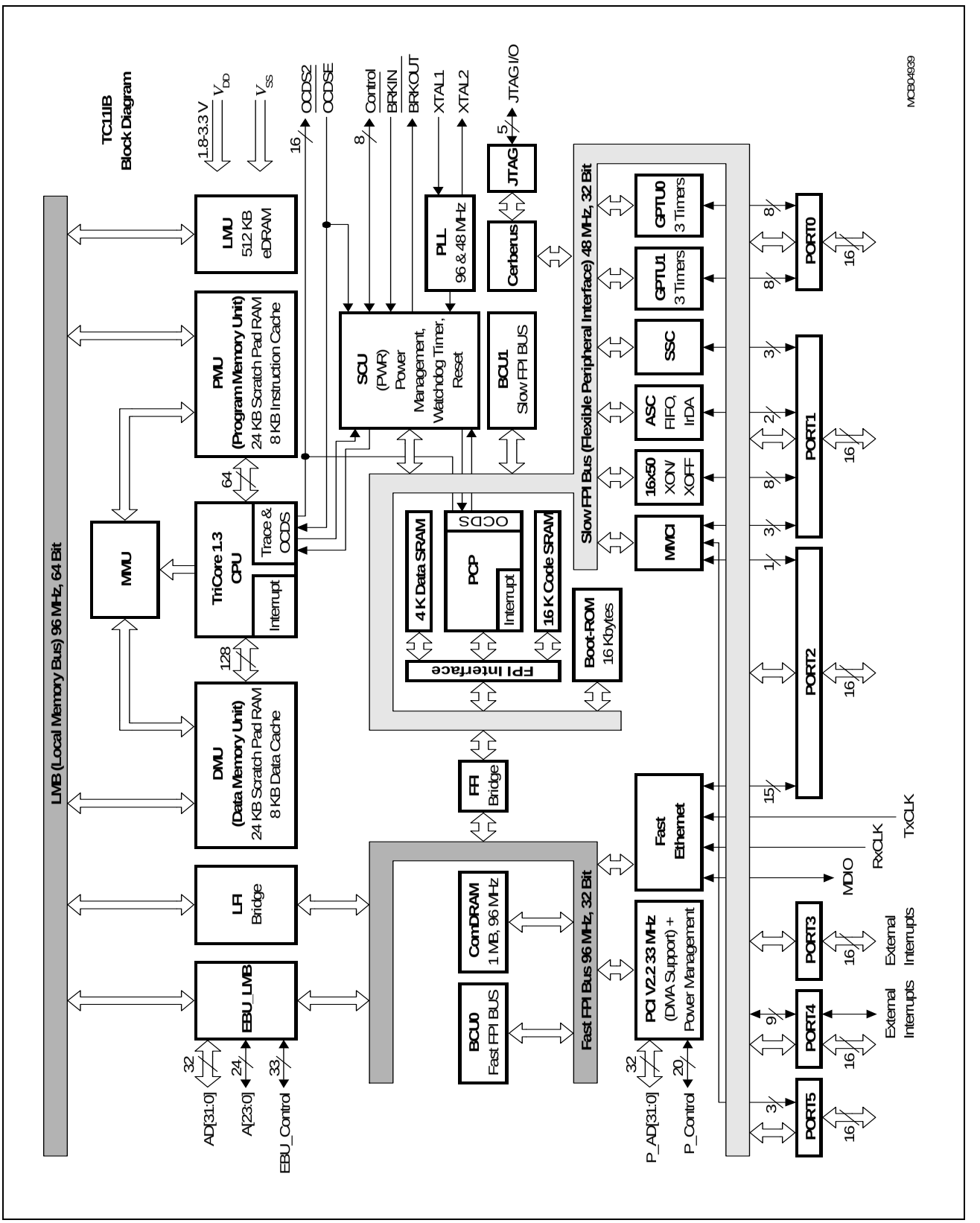


Figure 1 TC11IB Block Diagram

Logic Symbol

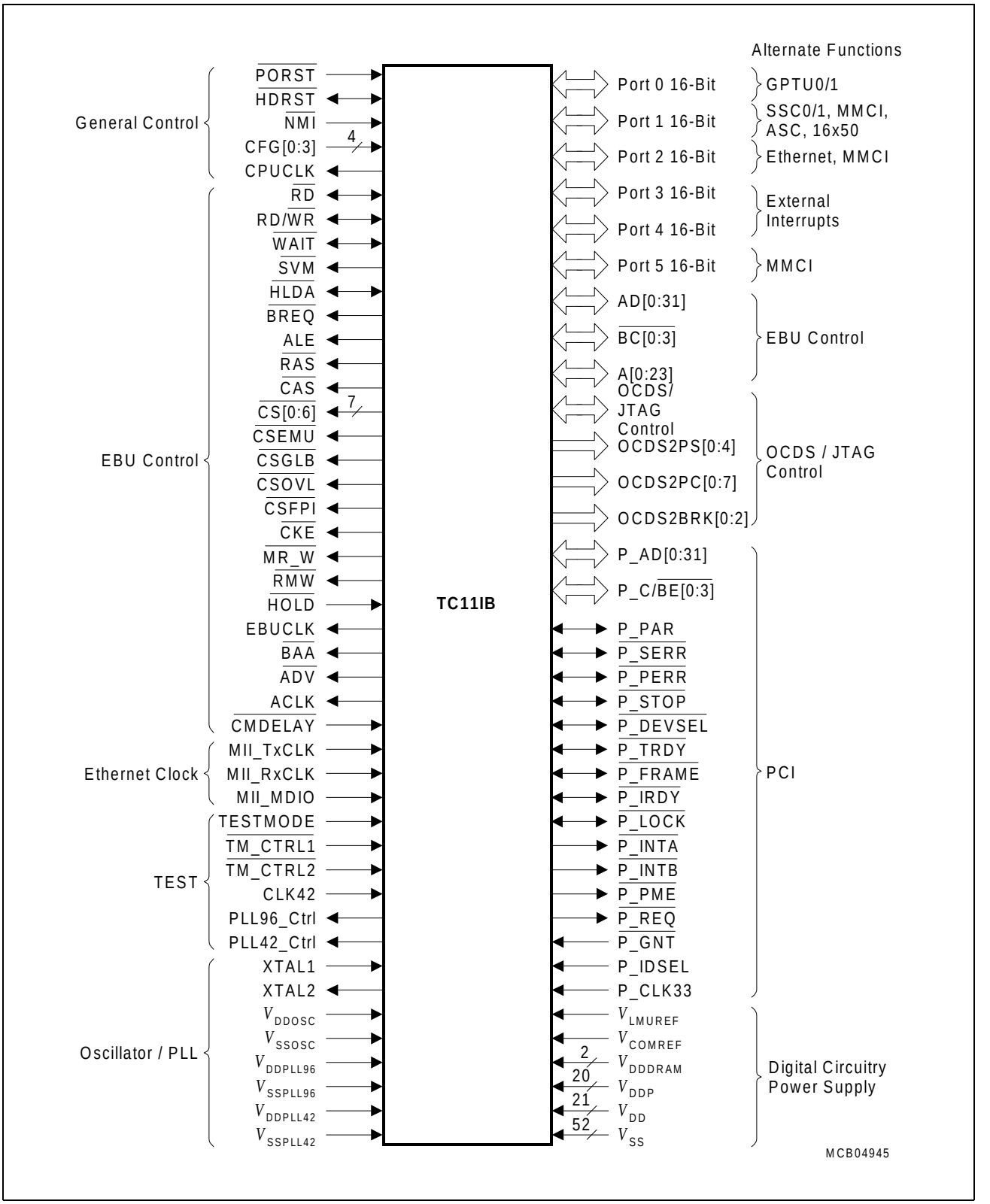


Figure 2 TC11IB Logic Symbol

Pin Configuration

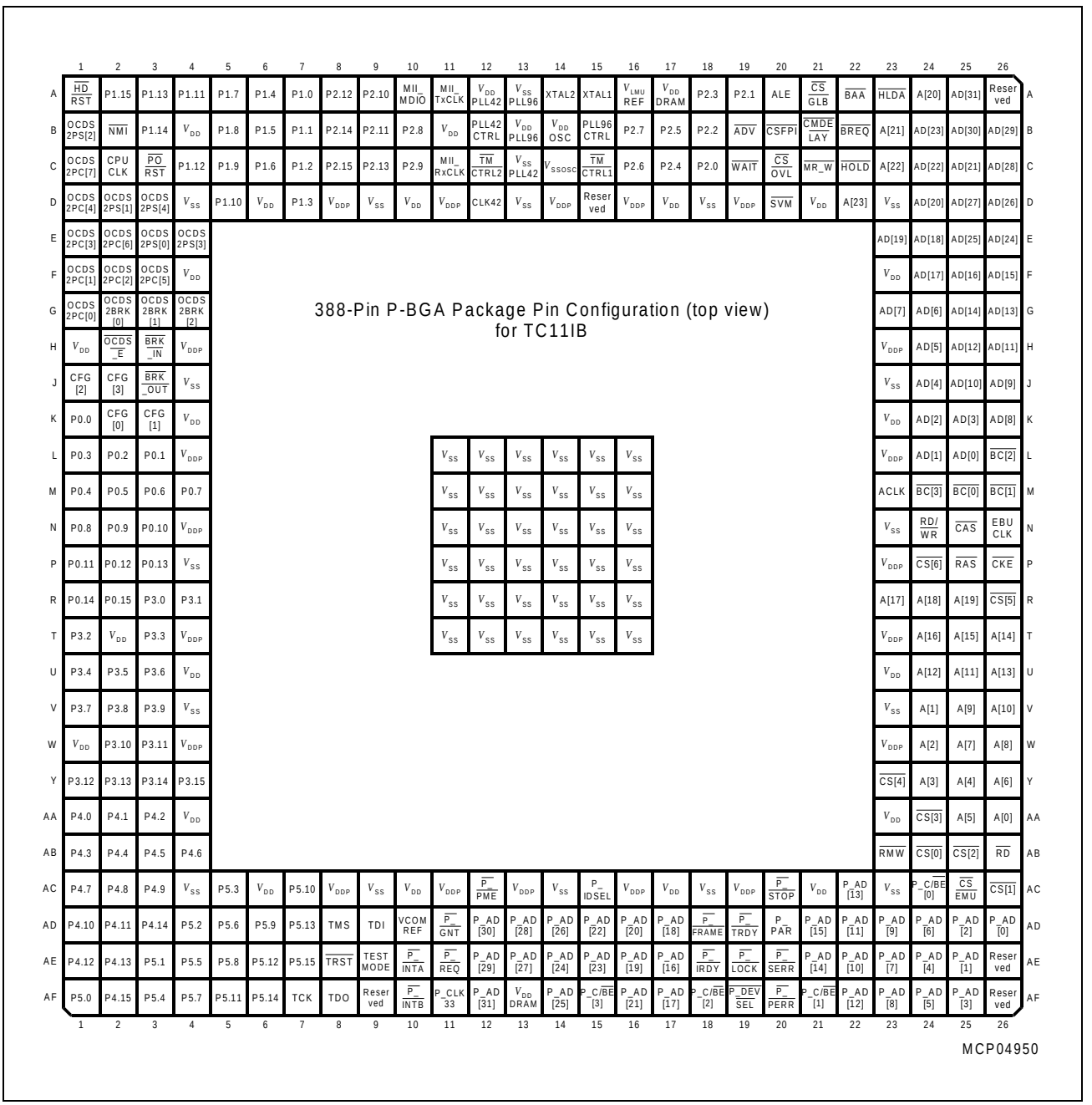


Figure 3 TC11IB Pinning: P-BGA-388 Package (top view)

Table 1 Pin Definitions and Functions

Symbol	Pin	In Out	PU/ PD[1)]	Functions
P0		I/O		**Port 0** Port 0 serves as 16-bit general purpose I/O port, which is also used as input/output for the General Purpose Timer Units (GPTU0 & GPTU1)
P0.0	K1	I/O	PUB	GPTU0_IO0 GPTU0 I/O line 0
P0.1	L3	I/O	PUB	GPTU0_IO1 GPTU0 I/O line 1
P0.2	L2	I/O	PUB	GPTU0_IO2 GPTU0 I/O line 2
P0.3	L1	I/O	PUB	GPTU0_IO3 GPTU0 I/O line 3
P0.4	M1	I/O	—	GPTU0_IO4 GPTU0 I/O line 4
P0.5	M2	I/O	—	GPTU0_IO5 GPTU0 I/O line 5
P0.6	M3	I/O	—	GPTU0_IO6 GPTU0 I/O line 6
P0.7	M4	I/O	—	GPTU0_IO7 GPTU0 I/O line 7
P0.8	N1	I/O	PUC	GPTU1_IO0 GPTU1 I/O line 0
P0.9	N2	I/O	PDC	GPTU1_IO1 GPTU1 I/O line 1
P0.10	N3	I/O	PDC	GPTU1_IO2 GPTU1 I/O line 2
P0.11	P1	I/O	PUC	GPTU1_IO3 GPTU1 I/O line 3
P0.12	P2	I/O	PUC	GPTU1_IO4 GPTU1 I/O line 4
P0.13	P3	I/O	PUC	GPTU1_IO5 GPTU1 I/O line 5
P0.14	R1	I/O	PUC	GPTU1_IO6 GPTU1 I/O line 6
P0.15	R2	I/O	PUC	GPTU1_IO7 GPTU1 I/O line 7

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P1		I/O		**Port 1** Port 1 serves as 16-bit general purpose I/O port, which also is used as input/output for the serial interfaces (SSC,ASC,16X50) and MultiMediaCard Interface (MMCI)	
P1.0	A7	I/O	PUC	SCLK	SSC clock input/output line
P1.1	B7	I/O	PUC	MRST	SSC master receive / slave transmit input/output
P1.2	C7	I/O	PUC	MTSR	SSC master transmit / slave receive input/output
P1.3	D7	O	PUC	MMCI_CLK	MMCI clock output line
P1.4	A6	I/O	PUC	MMCI_CMD	MMCI command input/output line
P1.5	B6	I/O	PUC	MMCI_DAT	MMCI data input/output line
P1.6	C6	I/O	PUC	ASC_RXD	ASC receiver input/output line
P1.7	A5	O	PUC	ASC_TXD	ASC transmitter output line
P1.8	B5	I	PUC	16X50_RXD	16X50 receiver input line
P1.9	C5	O	PUC	16X50_TXD	16X50 transmitter output line
P1.10	D5	O	PUC	16X50_$\overline{\text{RTS}}$	16X50 request to send output line
P1.11	A4	I	PUC	16X50_$\overline{\text{DCD}}$	16X50 data carrier detection input line
P1.12	C4	I	PUC	16X50_$\overline{\text{DSR}}$	16X50 data set ready input line
P1.13	A3	O	PUC	16X50_$\overline{\text{DTR}}$	16X50 data terminal ready output line
P1.14	B3	I	PUC	16X50_$\overline{\text{CTS}}$	16X50 clear to send input line
P1.15	A2	I	PUC	16X50_$\overline{\text{RI}}$	16X50 ring indicator input line

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P2		I/O		**Port 2** Port 2 serves as 16-bit general purpose I/O port, which is also used as input/output for Ethernet controller and MultiMediaCard (MMCI).	
P2.0	C18	O	—	MII_TXD0	Ethernet controller transmit data output line 0
P2.1	A19	O	—	MII_TXD1	Ethernet controller transmit data output line 1
P2.2	B18	O	—	MII_TXD2	Ethernet controller transmit data output line 2
P2.3	A18	O	—	MII_TXD3	Ethernet controller transmit data output line 3
P2.4	C17	O	—	MII_TXER	Ethernet controller transmit error output line
P2.5	B17	O	—	MII_TXEN	Ethernet controller transmit enable output line
P2.6	C16	O	—	MII_MDC	Ethernet controller management data clock output line
P2.7	B16	O	PUC	MMCI_VDDEN	MMCI power supply enable output line
P2.8	B10	I	PDC	MII_RXDV	Ethernet Controller receive data valid input line
P2.9	C10	I	PDC	MII_CRS	Ethernet Controller carrier input line
P2.10	A9	I	PUC	MII_COL	Ethernet Controller collision input line
P2.11	B9	I	PDC	MII_RXD0	Ethernet Controller receive data input line 0
P2.12	A8	I	PDC	MII_RXD1	Ethernet Controller receive data input line 1
P2.13	C9	I	PDC	MII_RXD2	Ethernet Controller receive data input line 2
P2.14	B8	I	PDC	MII_RXD3	Ethernet Controller receive data input line 3
P2.15	C8	I	PDC	MII_RXER	Ethernet Controller receive error input line

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P3		I/O		**Port 3** Port 3 serves as 16-bit general purpose I/O port, which is also used as input for external interrupts.	
P3.0	R3	I	—	INT0	External interrupt input line 0
P3.1	R4	I	—	INT1	External interrupt input line 1
P3.2	T1	I	—	INT2	External interrupt input line 2
P3.3	T3	I	—	INT3	External interrupt input line 3
P3.4	U1	I	—	INT4	External interrupt input line 4
P3.5	U2	I	—	INT5	External interrupt input line 5
P3.6	U3	I	—	INT6	External interrupt input line 6
P3.7	V1	I	—	INT7	External interrupt input line 7
P3.8	V2	I	—	INT8	External interrupt input line 8
P3.9	V3	I	—	INT9	External interrupt input line 9
P3.10	W2	I	—	INT10	External interrupt input line 10
P3.11	W3	I	—	INT11	External interrupt input line 11
P3.12	Y1	I	—	INT12	External interrupt input line 12
P3.13	Y2	I	—	INT13	External interrupt input line 13
P3.14	Y3	I	—	INT14	External interrupt input line 14
P3.15	Y4	I	—	INT15	External interrupt input line 15

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P4		I/O		**Port 4** Port 4 is used as general purpose I/O port, 8 pins of which (P4.0 ~ P4.7) also serve as inputs for external interrupts.	
P4.0	AA1	I	PDC	INT16	External interrupt input line 16
P4.1	AA2	I	PDC	INT17	External interrupt input line 17
P4.2	AA3	I	PDC	INT18	External interrupt input line 18
P4.3	AB1	I	PDC	INT19	External interrupt input line 19
P4.4	AB2	I	PUC	INT20	External interrupt input line 20
P4.5	AB3	I	PUC	INT21	External interrupt input line 21
P4.6	AB4	I	PUC	INT22	External interrupt input line 22
P4.7	AC1	I	PUC	INT23	External interrupt input line 23
P4.8	AC2	I/O	PUC		
P4.9	AC3	I/O	PUC		
P4.10	AD1	I/O	PUC		
P4.11	AD2	I/O	PUC		
P4.12	AE1	I/O	PUC		
P4.13	AE2	I/O	PUC		
P4.14	AD3	I/O	PUC		
P4.15	AF2	I/O	PUC		

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
P5		I/O		**Port 5** Port 5 serves as 16-bit general purpose I/O port, 3 pins of which (P5.0, P5.2 and P5.15) serve as output lines for MultiMediaCard Interface (MMCI) also.
P5.0	AF1	O	PUC	MMCI_DATRW MMCI data direction indicator output line
P5.1	AE3	I/O	PUC	
P5.2	AD4	O	PUC	MMCI_CMDRW MMCI command direction indicator output line
P5.3	AC5	I/O	PUC	
P5.4	AF3	I/O	PUC	
P5.5	AE4	I/O	PDC	
P5.6	AD5	I/O	PUC	
P5.7	AF4	I/O	PUC	
P5.8	AE5	I/O	PDC	
P5.9	AD6	I/O	PUC	
P5.10	AC7	I/O	—	
P5.11	AF5	I/O	—	
P5.12	AE6	I/O	—	
P5.13	AD7	I/O	—	
P5.14	AF6	I/O	—	
P5.15	AE7	O	PUC	MMCI_ROD MMCI command line mode indicator output line
$\overline{\text{HDRST}}$	A1	I/O	—	**Hardware Reset Input/Reset Indication Output** Assertion of this bidirectional open-drain pin causes a synchronous reset of the chip through external circuitry. This pin must be driven for a minimum duration. The internal reset circuitry drives this pin in response to a power-on, hardware, watchdog, power-down wake-up reset and eDRAM reset for a specific period of time. For a software reset, activation of this pin is programmable.
$\overline{\text{PORST}}$	C3	I	PUC	**Power-on Reset Input** A low level on $\overline{\text{PORST}}$ causes an asynchronous reset of the entire chip. $\overline{\text{PORST}}$ is a fully asynchronous level sensitive signal.

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
$\overline{\text{NMI}}$	B2	I	PUB	**Non-Maskable Interrupt Input** A high-to-low transition on this pin causes a NMI-Trap request to the CPU.
CFG0 **CFG1** **CFG2** **CFG3**	K2 K3 J1 J2	I I I I	PDC PDC PUC PUC	**Operation Configuration Inputs** The configuration inputs define the boot options of the TC11IB after a hardware-invoked reset operation.
CPU CLK	C2	O	PUC	**Clock Output**
$\overline{\text{TRST}}$	AE8	I	PDC	**JTAG Module Reset/Enable Input** A low level at this pin resets and disables the JTAG module. A high level enables the JTAG module.
TCK	AF7	I	PUC	**JTAG Module Clock Input**
TDI	AD9	I	PUC	**JTAG Module Serial Data Input**
TDO	AF8	O	—	**JTAG Module Serial Data Output**
TMS	AD8	I	PUC	**JTAG Module State Machine Control Input**
$\overline{\text{OCDSE}}$	H2	I	PUC	**OCDS Enable Input** A low level on this pin during power-on reset ($\overline{\text{PORST}}$ = 0) enables the on-chip debug support (OCDS). In addition, the level of this pin during power-on reset determines the boot configuration.
$\overline{\text{BRKIN}}$	H3	I	PUC	**OCDS Break Input** A low level on this pin causes a break in the chip's execution when the OCDS is enabled. In addition, the level of this pin during power-on reset determines the boot configuration.
$\overline{\text{BRKOUT}}$	J3	O	—	**OCDS Break Output** A low level on this pin indicates that a programmable OCDS event has occurred.

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
OCDS2 PS0	E3	O	PUC	**Pipeline Status Signal Outputs**
OCDS2 PS1	D2	O	PUC	
OCDS2 PS2	B1	O	PUC	
OCDS2 PS3	E4	O	PUC	
OCDS2 PS4	D3	O	PUC	
OCDS2 PC0	G1	O	PUC	**Indirect PC Address Outputs**
OCDS2 PC1	F1	O	PUC	
OCDS2 PC2	F2	O	PUC	
OCDS2 PC3	E1	O	PUC	
OCDS2 PC4	D1	O	PUC	
OCDS2 PC5	F3	O	PUC	
OCDS2 PC6	E2	O	PUC	
OCDS2 PC7	C1	O	PUC	
OCDS2 BRK0	G2	O	PUC	**Break Qualification Lines outputs**
OCDS2 BRK1	G3	O	PUC	
OCDS2 BRK2	G4	O	PUC	

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				PCI Interface Address /Data Bus Input / Output Lines
P_AD0	AD26	I/O	—	PCI Interface Address / Data Bus Line 0
P_AD1	AE25	I/O	—	PCI Interface Address / Data Bus Line 1
P_AD2	AD25	I/O	—	PCI Interface Address / Data Bus Line 2
P_AD3	AF25	I/O	—	PCI Interface Address / Data Bus Line 3
P_AD4	AE24	I/O	—	PCI Interface Address / Data Bus Line 4
P_AD5	AF24	I/O	—	PCI Interface Address / Data Bus Line 5
P_AD6	AD24	I/O	—	PCI Interface Address / Data Bus Line 6
P_AD7	AE23	I/O	—	PCI Interface Address / Data Bus Line 7
P_AD8	AF23	I/O	—	PCI Interface Address / Data Bus Line 8
P_AD9	AD23	I/O	—	PCI Interface Address / Data Bus Line 9
P_AD10	AE22	I/O	—	PCI Interface Address / Data Bus Line 10
P_AD11	AD22	I/O	—	PCI Interface Address / Data Bus Line 11
P_AD12	AF22	I/O	—	PCI Interface Address / Data Bus Line 12
P_AD13	AC22	I/O	—	PCI Interface Address / Data Bus Line 13
P_AD14	AE21	I/O	—	PCI Interface Address / Data Bus Line 14
P_AD15	AD21	I/O	—	PCI Interface Address / Data Bus Line 15
P_AD16	AE17	I/O	—	PCI Interface Address / Data Bus Line 16
P_AD17	AF17	I/O	—	PCI Interface Address / Data Bus Line 17
P_AD18	AD17	I/O	—	PCI Interface Address / Data Bus Line 18
P_AD19	AE16	I/O	—	PCI Interface Address / Data Bus Line 19
P_AD20	AD16	I/O	—	PCI Interface Address / Data Bus Line 20
P_AD21	AF16	I/O	—	PCI Interface Address / Data Bus Line 21
P_AD22	AD15	I/O	—	PCI Interface Address / Data Bus Line 22
P_AD23	AE15	I/O	—	PCI Interface Address / Data Bus Line 23
P_AD24	AE14	I/O	—	PCI Interface Address / Data Bus Line 24
P_AD25	AF14	I/O	—	PCI Interface Address / Data Bus Line 25
P_AD26	AD14	I/O	—	PCI Interface Address / Data Bus Line 26
P_AD27	AE13	I/O	—	PCI Interface Address / Data Bus Line 27
P_AD28	AD13	I/O	—	PCI Interface Address / Data Bus Line 28
P_AD29	AE12	I/O	—	PCI Interface Address / Data Bus Line 29
P_AD30	AD12	I/O	—	PCI Interface Address / Data Bus Line 30
P_AD31	AF12	I/O	—	PCI Interface Address / Data Bus Line 31
P_PAR	AD20	I/O	—	**PCI Interface Parity Input / Output**
$\overline{\text{P\_SERR}}$	AE20	I/O	—	**PCI Interface System Error Input / Output**
$\overline{\text{P\_PERR}}$	AF20	I/O	—	**PCI Interface Parity Error Input / Output**

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
P_STOP	AC20	I/O	—	**PCI Interface Stop Input / Output**
P_C/BE0 **P_C/BE1** **P_C/BE2** **P_C/BE3**	AC24 AF21 AF18 AF15	I/O I/O I/O I/O	— — — —	**PCI Interface Command / Byte Enable Inputs / Outputs**
P_IDSEL	AC15	I	—	**PCI Interface ID Select Input**
P_CLK33	AF11	I	—	**PCI Interface Clock Input**
P_REQ	AE11	O	—	**PCI Interface Bus Request Output**
P_GNT	AD11	I	—	**PCI Interface Bus Grant Input**
P_DEVSEL	AF19	I/O	—	**PCI Interface Device Select Input / Output**
P_TRDY	AD19	I/O	—	**PCI Interface Target Ready Input / Output**
P_FRAME	AD18	I/O	—	**PCI Interface Frame Input / Output**
P_IRDY	AE18	I/O	—	**PCI Interface Initiator Ready Input / Output**
P_LOCK	AE19	I	—	**PCI Interface Lock Input**
P_INTA	AE10	O	—	**PCI Interface Interrupt A Output**
P_INTB	AF10	O	—	**PCI Interface Interrupt B Output**
P_PME	AC12	O	—	**PCI Interface Power Management Event Output**
MII_ TXCLK	A11	I	PDC	**Ethernet Controller Transmit Clock** MII_TXD[3:0] and MII_TXEN are driven off the rising edge of the MII_TXCLK by the core and sampled by the PHY on the rising edge of the MII_TXCLK.
MII_ RXCLK	C11	I	PDC	**Ethernet Controller Receive Clock** MII_RXCLK is a continuous clock. Its frequency is 25 MHz for 100 Mbps operation, and 2.5 MHz for 10Mbps. MII_RXD[3:0], MII_RXDV and MII_EXER are driven by the PHY off the falling edge of MII_RXCLK and sampled on the rising edge of MII_RXCLK.

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
MII_ MDIO	A10	I/O	PDA	**Ethernet Controller Management Data Input / Output** When a read command is being executed, data which is clocked out of the PHY will be presented on the input line. When the Core is clocking control or data onto the MII_MDIO line, the signal will carry the information.
$\overline{CS0}$ **$\overline{CS1}$** **$\overline{CS2}$** **$\overline{CS3}$** **$\overline{CS4}$** **$\overline{CS5}$** **$\overline{CS6}$**	AB24 AC26 AB25 AA24 Y23 R26 P24	O O O O O O O	PUC PUC PUC PUC PUC PUC PUC	**EBU_LMB Chip Select Output Line 0** **EBU_LMB Chip Select Output Line 1** **EBU_LMB Chip Select Output Line 2** **EBU_LMB Chip Select Output Line 3** **EBU_LMB Chip Select Output Line 4** **EBU_LMB Chip Select Output Line 5** **EBU_LMB Chip Select Output Line 6** Each corresponds to a programmable region. Only one can be active at one time.
$\overline{CSEMU}$	AC25	O	PUC	**EBU_LMB Chip Select Output for Emulator Region**
$\overline{CSGLB}$	A21	O	PUC	**EBU_LMB Chip Select Global Output**
$\overline{CSOVL}$	C20	O	PUC	**EBU_LMB Chip Select Output for Overlay Memory**
$\overline{CSFPI}$	B20	I	PUC	**EBU_LMB Chip Select Input for Internal FPI Bus** For external master to select EBU_LMB as target in the slave mode
EBUCLK	N26	O	—	**EBU_LMB External Bus Clock Output** Derived from LMBCLK as equal, half or one-fourth of the frequency.

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				EBU_LMB Address / Data Bus Input / Output Lines
AD0	L25	I/O	PUC	EBU_LMB Address / Data Bus Line 0
AD1	L24	I/O	PUC	EBU_LMB Address / Data Bus Line 1
AD2	K24	I/O	PUC	EBU_LMB Address / Data Bus Line 2
AD3	K25	I/O	PUC	EBU_LMB Address / Data Bus Line 3
AD4	J24	I/O	PUC	EBU_LMB Address / Data Bus Line 4
AD5	H24	I/O	PUC	EBU_LMB Address / Data Bus Line 5
AD6	G24	I/O	PUC	EBU_LMB Address / Data Bus Line 6
AD7	G23	I/O	PUC	EBU_LMB Address / Data Bus Line 7
AD8	K26	I/O	PUC	EBU_LMB Address / Data Bus Line 8
AD9	J26	I/O	PUC	EBU_LMB Address / Data Bus Line 9
AD10	J25	I/O	PUC	EBU_LMB Address / Data Bus Line 10
AD11	H26	I/O	PUC	EBU_LMB Address / Data Bus Line 11
AD12	H25	I/O	PUC	EBU_LMB Address / Data Bus Line 12
AD13	G26	I/O	PUC	EBU_LMB Address / Data Bus Line 13
AD14	G25	I/O	PUC	EBU_LMB Address / Data Bus Line 14
AD15	F26	I/O	PUC	EBU_LMB Address / Data Bus Line 15
AD16	F25	I/O	PUC	EBU_LMB Address / Data Bus Line 16
AD17	F24	I/O	PUC	EBU_LMB Address / Data Bus Line 17
AD18	E24	I/O	PUC	EBU_LMB Address / Data Bus Line 18
AD19	E23	I/O	PUC	EBU_LMB Address / Data Bus Line 19
AD20	D24	I/O	PUC	EBU_LMB Address / Data Bus Line 20
AD21	C25	I/O	PUC	EBU_LMB Address / Data Bus Line 21
AD22	C24	I/O	PUC	EBU_LMB Address / Data Bus Line 22
AD23	B24	I/O	PUC	EBU_LMB Address / Data Bus Line 23
AD24	E26	I/O	PUC	EBU_LMB Address / Data Bus Line 24
AD25	E25	I/O	PUC	EBU_LMB Address / Data Bus Line 25
AD26	D26	I/O	PUC	EBU_LMB Address / Data Bus Line 26
AD27	D25	I/O	PUC	EBU_LMB Address / Data Bus Line 27
AD28	C26	I/O	PUC	EBU_LMB Address / Data Bus Line 28
AD29	B26	I/O	PUC	EBU_LMB Address / Data Bus Line 29
AD30	B25	I/O	PUC	EBU_LMB Address / Data Bus Line 30
AD31	A25	I/O	PUC	EBU_LMB Address / Data Bus Line 31
$\overline{BC0}$	M25	I/O	PUC	**EBU_LMB Byte Control Line 0**
$\overline{BC1}$	M26	I/O	PUC	**EBU_LMB Byte Control Line 1**
$\overline{BC2}$	L26	I/O	PUC	**EBU_LMB Byte Control Line 2**
$\overline{BC3}$	M24	I/O	PUC	**EBU_LMB Byte Control Line 3**

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				EBU_LMB Address Bus Input / Output Lines
A0	AA26	I/O	PUC	EBU_LMB Address Bus Line 0
A1	V24	I/O	PUC	EBU_LMB Address Bus Line 1
A2	W24	I/O	PUC	EBU_LMB Address Bus Line 2
A3	Y24	I/O	PUC	EBU_LMB Address Bus Line 3
A4	Y25	I/O	PUC	EBU_LMB Address Bus Line 4
A5	AA25	I/O	PUC	EBU_LMB Address Bus Line 5
A6	Y26	I/O	PUC	EBU_LMB Address Bus Line 6
A7	W25	I/O	PUC	EBU_LMB Address Bus Line 7
A8	W26	I/O	PUC	EBU_LMB Address Bus Line 8
A9	V25	I/O	PUC	EBU_LMB Address Bus Line 9
A10	V26	I/O	PUC	EBU_LMB Address Bus Line 10
A11	U25	I/O	PUC	EBU_LMB Address Bus Line 11
A12	U24	I/O	PUC	EBU_LMB Address Bus Line 12
A13	U26	I/O	PUC	EBU_LMB Address Bus Line 13
A14	T26	I/O	PUC	EBU_LMB Address Bus Line 14
A15	T25	I/O	PUC	EBU_LMB Address Bus Line 15
A16	T24	I/O	PUC	EBU_LMB Address Bus Line 16
A17	R23	I/O	PUC	EBU_LMB Address Bus Line 17
A18	R24	I/O	PUC	EBU_LMB Address Bus Line 18
A19	R25	I/O	PUC	EBU_LMB Address Bus Line 19
A20	A24	I/O	PUC	EBU_LMB Address Bus Line 20
A21	B23	I/O	PUC	EBU_LMB Address Bus Line 21
A22	C23	I/O	PUC	EBU_LMB Address Bus Line 22
A23	D22	I/O	PUC	EBU_LMB Address Bus Line 23
$\overline{RD}$	AB26	I/O	PUC	**EBU_LMB Read Control Line** Output in the master mode Input in the slave mode.
RD/$\overline{WR}$	N24	I/O	PUC	**EBU_LMB Write Control Line** Output in the master mode Input in the slave mode.
$\overline{WAIT}$	C19	I/O	PUC	**EBU_LMB Wait Control Line**
$\overline{SVM}$	D20	O	PUB	**EBU_LMB Supervisor Mode Output**
ALE	A20	O	PDC	**EBU_LMB Address Latch Enable Output**
$\overline{RAS}$	P25	O	PUC	**EBU_LMB SDRAM Row Address Strobe Output**
$\overline{CAS}$	N25	O	PUC	**EBU_LMB SDRAM Column Address Strobe Output**

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
$\overline{\text{CKE}}$	P26	O	PUC	**EBU_LMB SDRAM Clock Enable Output**
MR/$\overline{\text{W}}$	C21	O	PUC	**EBU_LMB Motorola-style Read / Write Output**
$\overline{\text{HOLD}}$	C22	I	PUC	**EBU_LMB Hold Request Input** In External Master Mode: While $\overline{\text{HOLD}}$ is high, Tricore is operating in normal mode (is owner of the external bus). A high-to-low transition indicates a hold request from an external master.Tricore backs off the bus and activates $\overline{\text{HLDA}}$ and goes into hold mode. A low-to-high transitions causes an exit from hold mode.Tricore deactivates $\overline{\text{HLDA}}$ and takes over the bus and enters the normal operation again. In External Slave Mode: While both $\overline{\text{HOLD}}$ and $\overline{\text{HLDA}}$ are high, Tricore is in hold mode, the external bus interface signals are tristated. When Tricore is released out of hold mode ($\overline{\text{HLDA}}$ =0) and has completely taken over control of the external bus, a low level at this pin requests Tricore to go into hold mode again. But in any case Tricore will perform at least one external bus cycle before going into hold mode again.
$\overline{\text{HLDA}}$	A23	I/O	PUC	**EBU_LMB Hold Acknowledge Input / Output** In External Master Mode: OutPut. High during normal operation.When Tricore enters hold mode, it sets $\overline{\text{HLDA}}$ to low after releasing the bus. On exit of hold mode, Tricore first sets $\overline{\text{HLDA}}$ to high and then goes onto the bus again (to avoid collisions). In External Slave Mode: Input. A high-to-low transition at this pin releases Tricore from hold mode.

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
$\overline{\text{BREQ}}$	B22	O	PUC	**EBU_LMB Bus Request Output** In External Master Mode: High during normal operation.Tricore activates $\overline{\text{BREQ}}$ earliest one clock cycle after activating $\overline{\text{HLDA}}$, if it has to perform an external bus access. If Tricore has regained the bus, $\overline{\text{BREQ}}$ is set to high one clock cycle after deactivation of $\overline{\text{HLDA}}$. In External Slave Mode: This signal is high as long as Tricore operates from internal memory. When it detects that an external access is required, it sets $\overline{\text{BREQ}}$ to low and waits for signal $\overline{\text{HLDA}}$ to become low. $\overline{\text{BREQ}}$ will go back to high when the slave has backed off the bus after it was requested to go into hold mode.
$\overline{\text{RMW}}$	AB23	I/O	PUC	**EBU_LMB Read-Modify-Write Signal Line**
$\overline{\text{BAA}}$	A22	O	PUC	**EBU_LMB Burst Address Advance Output** For advancing address in a burst flash access
$\overline{\text{ADV}}$	B19	O	PUC	**EBU_LMB Burst Flash Address Valid Output**
ACLK	M23	O	—	**EBU_LMB Additional Clock Output** Additional clock running equal, 1/2, 1/3 or 1/4 frequency of EBUCLK
$\overline{\text{CMDELAY}}$	B21	I	PUC	**EBU_LMB Command Delay Input** For inserting delays between address and command.
TEST MODE	AE9	I	PDC	**Test Mode Select Input** For normal operation of the TC11IB, this pin should be connected to V_{SS}.
$\overline{\text{TM CTRL1}}$	C15	I	PUB	**Test Mode Control Input 1** For normal operation of the TC11IB, this pin should be connected to V_{DDP}.
$\overline{\text{TM CTRL2}}$	C12	I	PUB	**Test Mode Control Input 2** For normal operation of the TC11IB, this pin should be connected to V_{DDP}.

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
CLK42	D12	I	PDC	**Test Clock 42 MHz Input** For normal operation of the TC11IB, this pin should be connected to V_{SS}.
PLL96 CTRL	B15	O	—	**Test PLL96 Analog Output** For normal operation of the TC11IB, this pin must not be connected.
PLL42 CTRL	B12	O	—	**Test PLL42 Analog Output** For normal operation of the TC11IB, this pin must not be connected.
XTAL1 **XTAL2**	A15 A14	I O	— —	**Oscillator/PLL/Clock Generator Input/Output Pins** XTAL1 is the input to the main oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the main oscillator amplifier circuit. For clocking the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
V_{DDOSC}	B14	—	—	**Main Oscillator Power Supply (1.8V)**
V_{SSOSC}	C14	—	—	**Main Oscillator Ground**
$V_{DDPLL96}$	B13	—	—	**PLL96 Power Supply (1.8V)**
$V_{SSPLL96}$	A13	—	—	**PLL96 Ground**
$V_{DDPLL42}$	A12	—	—	**Test PLL42 Power Supply (1.8V)** For normal operation of the TC11IB, this pin must not be connected.
$V_{SSPLL42}$	C13	—	—	**Test PLL42 Ground** For normal operation of the TC11IB, this pin must be connected to V_{SS}.
V_{LMUREF}	A16	—	—	**LMU Reference Voltage** This pin has to be connected to V_{SS}
V_{COMREF}	AD10	—	—	**ComDRAM Reference Voltage** This pin has to be connected to V_{SS}
V_{DDDRAM}	A17, AF13	—	—	**eDRAM Power Supply (1.8V)**

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
V_{DD}	H1 W1 T2,B4 B11 D6,F4 D10 D17 D21 F23 K4 K23 U4 U23 AA4 AA23 AC6 AC10 AC17 AC21	—	—	**Core and Logic Power Supply (1.8V)**

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
V_{DDP}	D8, D11, D14, D16, D19, H4, H23, L4, L23, N4, P23, T4, T23, W4, W23, AC8, AC11, AC13, AC16, AC19	—	—	**Ports Power Supply (3.3V)**

Table 1 Pin Definitions and Functions(cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
V_{SS}	D4 D9 D13 D18 D23 J4 J23 N23 P4,V4 V23 AC4 AC9 AC14 AC18 AC23 L11 to L16, M11 to M16, N11 to N16, P11 to P16, R11 to R16, T11 to T16	—	—	**Ground**
N.C.	D15, A26, AE26, AF9, AF26	—	—	**Not Connected** These pins must not be connected.

1) Refers to internal pull-up or pull-down device connected and corresponding type. The notation '—' indicates that the internal pull-up or pull-down device is not enabled.

Parallel Ports

The TC11IB has 96 digital input/output port lines, which are organized into six parallel 16-bit ports, Port P0 to Port P5 with 3.3V nominal voltage.

The digital parallel ports can be all used as general purpose I/O lines or they can perform input/output functions for the on-chip peripheral units. An overview on the port-to-peripheral unit assignment is shown in **Figure 4**.

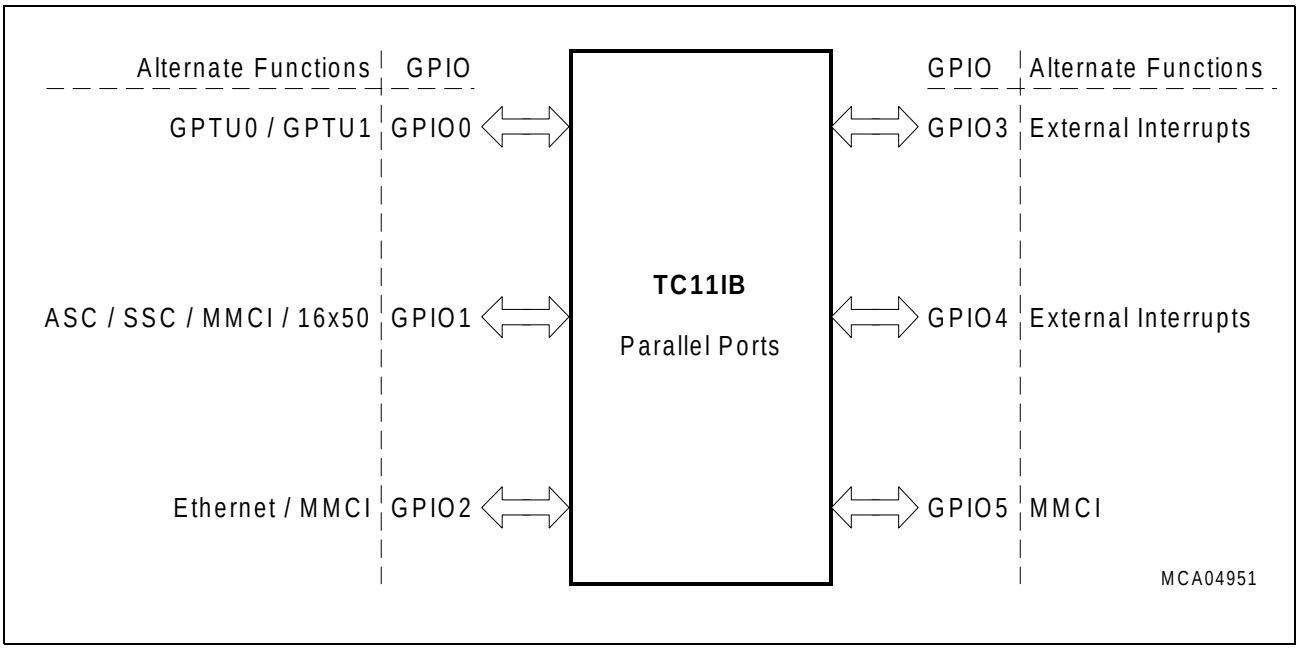


Figure 4 Parallel Ports of the TC11IB

Serial Interfaces

The TC11IB includes three serial peripheral interface units:

- Asynchronous/Synchronous Serial Interface (ASC)
- High-Speed Synchronous Serial Interface (SSC)
- Asynchronous Serial Interface (16X50)

Asynchronous/Synchronous Serial Interface

Figure 5 shows a global view of the functional blocks of the Asynchronous/Synchronous Serial interface ASC.

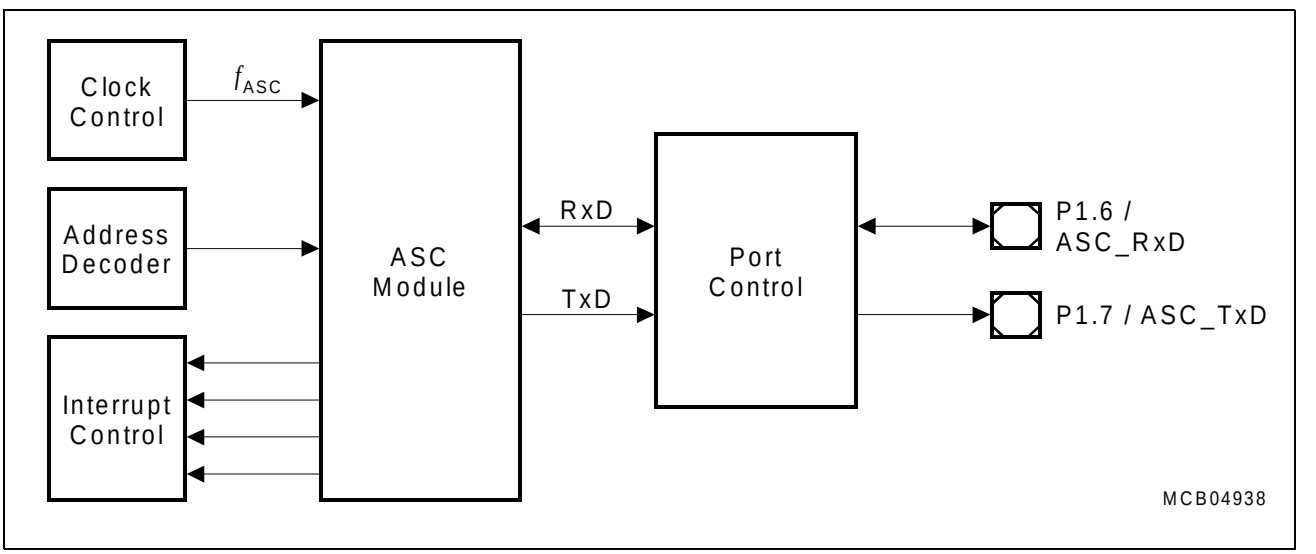


Figure 5 General Block Diagram of the ASC Interfaces

ASC Module communicates with the external world via one pair of I/O lines. The RXD line is the receive data input signal (in Synchronous Mode also output). TXD is the transmit output signal. Clock control, address decoding, and interrupt service request control are managed outside the ASC Module kernel.

The Asynchronous/Synchronous Serial Interface provides serial communication between the TC11IB and other microcontrollers, microprocessors or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock which is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data are double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator

provides the ASC with a separate serial clock signal that can be very accurately adjusted by a prescaler implemented as a fractional divider.

Features:

- Full duplex asynchronous operating modes
  - 8- or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baudrate from 3 MBaud to 0.71 Baud (@ 48 MHz clock)
- Multiprocessor mode for automatic address/data byte detection
- Loop-back capability
- Support for IrDA data transmission up to 115.2 KBaud maximum
- Half-duplex 8-bit synchronous operating mode
  - Baudrate from 6 MBaud to 488.3 Baud (@ 48 MHz clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - On a transmitter buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receiver buffer full condition
  - On an error condition (frame, parity, overrun error)
- FIFO
  - 8 bytes receive FIFO (RXFIFO)
  - 8 bytes transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 9-bit FIFO data width
  - Programmable Receive/Transmit Interrupt Trigger Level
  - Receive and transmit FIFO filling level indication
  - Overrun error generation
- Two pin pair RXD/TXD available at Port 1

High-Speed Synchronous Serial Interface

Figure 6 shows a global view of the functional blocks of the High-Speed Synchronous Serial interface SSC.

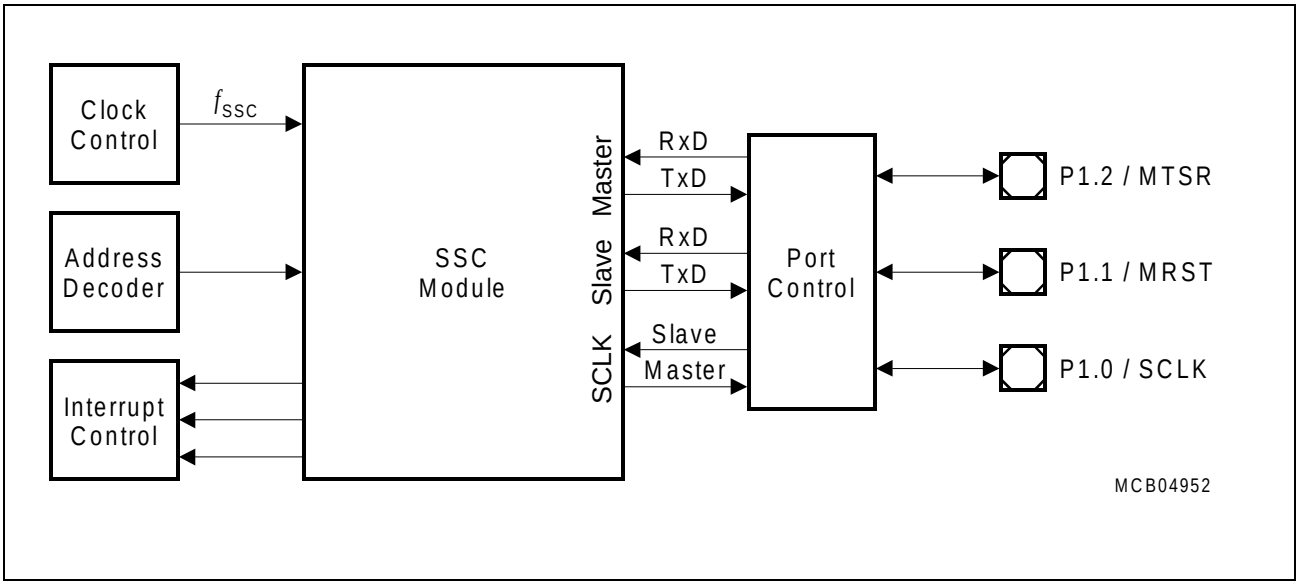


Figure 6 General Block Diagram of the SSC Interfaces

The SSC Module has three I/O lines, located at Port 1. The SSC Module is further supplied by separate clock control, interrupt control, address decoding, and port control logic.

The SSC supports full-duplex and half-duplex serial synchronous communication up to 24 MBaud (@ 48 MHz module clock). The serial clock signal can be generated by the SSC itself (master mode) or can be received from an external master (slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data are double-buffered. A 16-bit baud rate generator provides the SSC with a separate serial clock signal.

Features:

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Flexible data format
  - Programmable number of data bits: 2 to 16 bit
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate generation from 24 MBaud to 366.2 Baud (@ 48 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Three-pin interface
  - Flexible SSC pin configuration

Asynchronous Serial Interface (16X50)

The 16X50 is a universal asynchronous receiver/transmitter (UART) which is fully prorammable.It supports word lengths from five to eight bits, an optional parity bit and one or two stop bits.If enabled, the parity can be odd, even or forced to a defined state. The 16X50 includes a 16-bit programmable baud rate generator and an 8-bit scratch register, together with two 16-byte FIFOs -one for transmit and one for receive. It has six modem control lines and supports a diagnostic loop-back mode. An interrupt can be generated from any one of 10 sources. **Figure 7** shows a global view of the functional blocks of the Asynchronous Serial Interface (16X50).

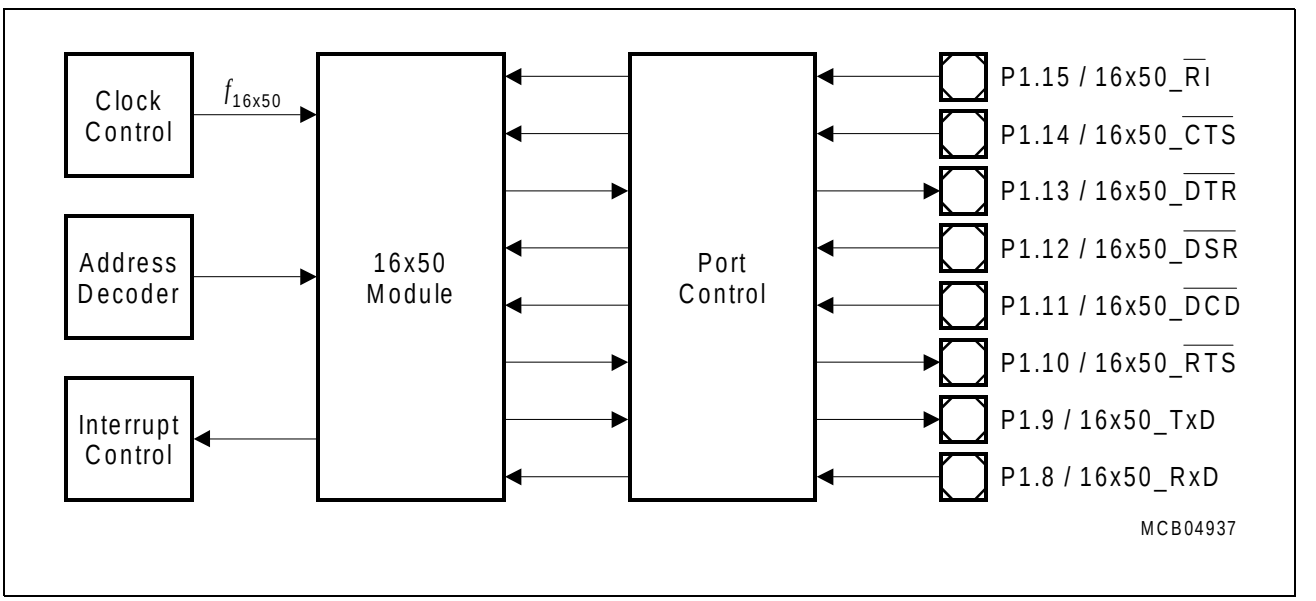


Figure 7 General Block Diagram of the 16X50 Interface

The 16X50 Module communicates with the external world via five input and three output lines located at Port 1.

The 16X50 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The 16X50 represents such an integration with greatly enhanced features.

The 16X50 is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of 1 byte provided in the 16C450. The 16X50 is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 16X50 by the larger transmit and receive

FIFO's. This allows the external processor to handle more networking tasks within a given time. The 4 selectable levels of FIFO trigger provided for maximum data throughput performance especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The 16X50 is capable of operation to 3 Mbps with a 48 MHz clock input (f_{16X50}).

Features:

- Software upward compatible with the NS16550A
- Standard modem interface
- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Interrupt generation
- Diagnostic loop-back mode
- Scratch register
- Automatic hardware/software flow control
- Programmable XON/XOFF characters
- Independent transmit and receive control
- FIFO
  - 16 byte transmit FIFO
  - 16 byte receive FIFO with error flags
  - Four selectable receive FIFO interrupt trigger levels

General Purpose Timer Units

Figure 8 shows a global view of all functional blocks of the two General Purpose Timer Unit (GPTU0 & GPTU1) Modules.

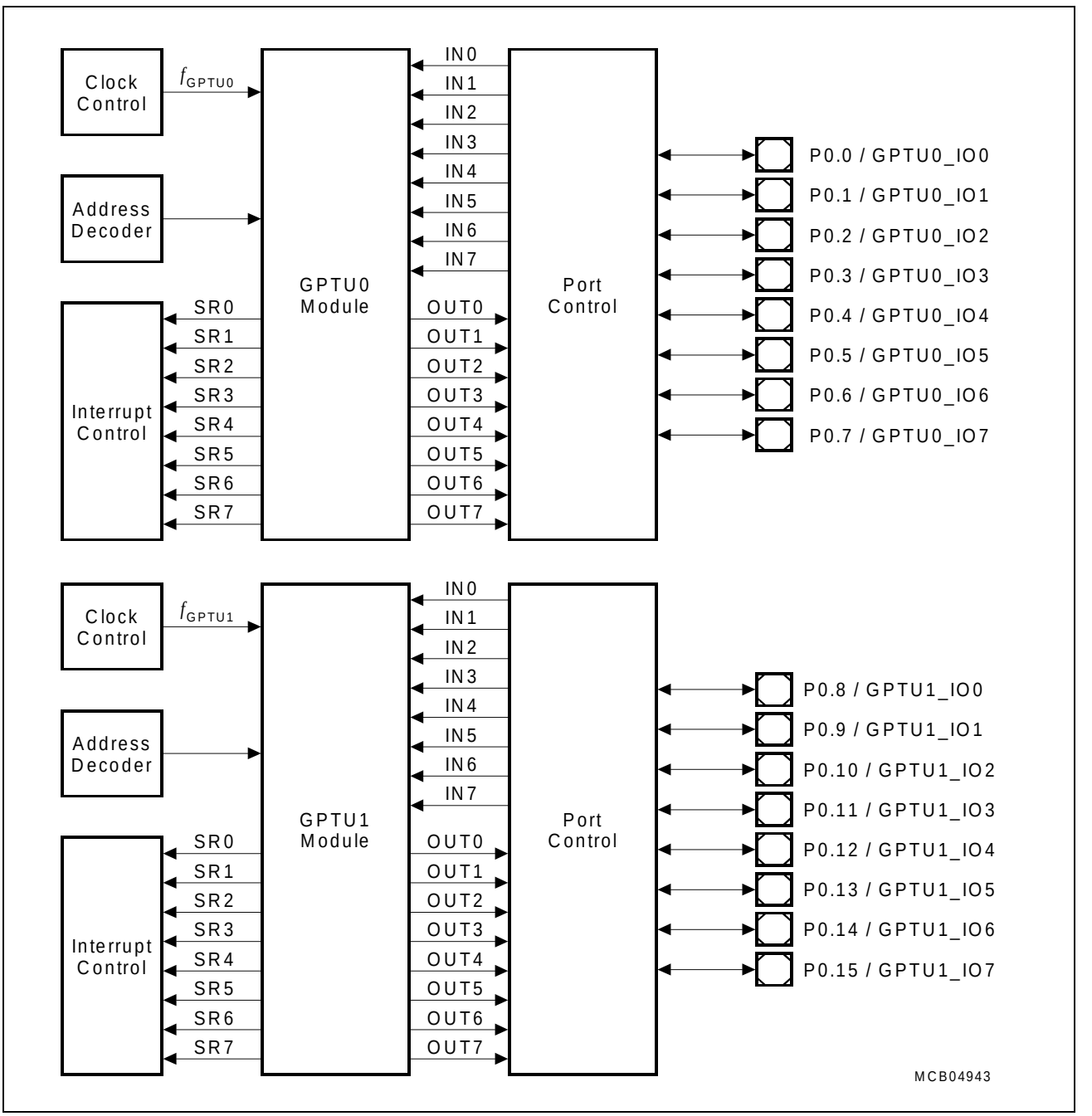


Figure 8 General Block Diagram of the GPTU Interface

Each GPTU module, GPTU0 and GPTU1, consists of three 32-bit timers designed to solve such application tasks as event timing, event counting, and event recording. And each GPTU module communicates with the external world via eight I/O lines located at Port 1.

The three timers in each GPTU Module T0, T1, and T2, can operate independently from each other or can be combined:

General Features:

- All timers are 32-bit precision timers with a maximum input frequency of f_{GPTU}.
- Events generated in T0 or T1 can be used to trigger actions in T2
- Timer overflow or underflow in T2 can be used to clock either T0 or T1
- T0 and T1 can be concatenated to form one 64-bit timer

Features of T0 and T1:

- Each timer has a dedicated 32-bit reload register with automatic reload on overflow
- Timers can be split into individual 8-, 16-, or 24-bit timers with individual reload registers
- Overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events
- Two input pins can determine a count option

Features of T2:

- Count up or down is selectable
- Operating modes:
  - Timer
  - Counter
  - Quadrature counter (incremental/phase encoded counter interface)
- Options:
  - External start/stop, one-shot operation, timer clear on external event
  - Count direction control through software or an external event
  - Two 32-bit reload/capture registers
- Reload modes:
  - Reload on overflow or underflow
  - Reload on external event: positive transition, negative transition, or both transitions
- Capture modes:
  - Capture on external event: positive transition, negative transition, or both transitions
  - Capture and clear timer on external event: positive transition, negative transition, or both transitions
- Can be split into two 16-bit counter/timers
- Timer count, reload, capture, and trigger functions can be assigned to input pins. T0 and T1 overflow events can also be assigned to these functions.
- Overflow and underflow signals can be used to trigger T0 and/or T1 and to toggle output pins
- T2 events are freely assignable to the service request nodes.

MultiMediaCard Interface (MMCI)

The MultiMediaCard Interface module provides interface to MultiMediaCard bus. It supports the full MultiMediaCard bus protocol as defined in MultiMediaCard system specification version 1.3. **Figure 9** shows a global view of the MMCI module with the module specific interface connections.

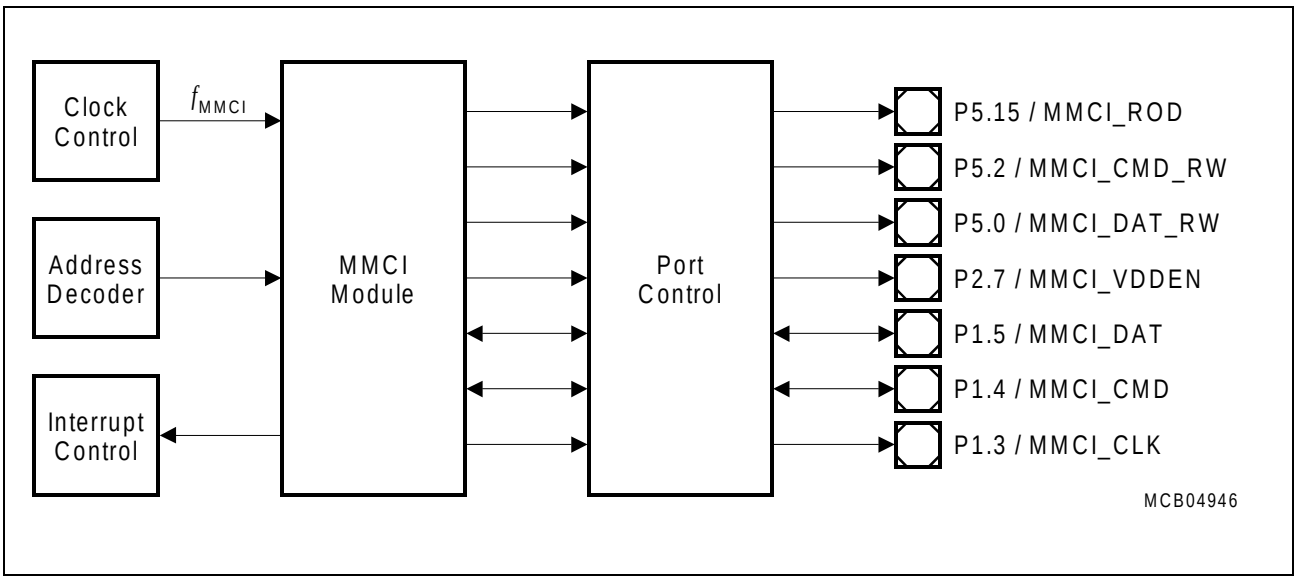


Figure 9 General Block Diagram of MMCI Interface

The MMCI module communicates with external world via two IO lines and five output lines which are located at Port 1, 2 and 5. Clock control, interrupt service and address decoding are managed outside the MMCI module Kernel.

MMCI handles the data transfer on CMD and DAT of the MMC Bus. It performs the transfer from bit serial to byte parallel or vice versa and sustains a 16Mbps data rate. To fulfil the MMC Bus protocol, special bytes are modified via inserting start and stop bits or CRC bits. A clock controller is implemented to divide the clock to the necessary MMC Bus clock frequency.

Features

- 3 line serial interface --- Glueless interface to MultiMediaCard Bus
- Pointer based data transfer
- Block and sequential card access
- 16MHz MultiMediaCard bus clock generation
- CRC protection for the MultiMediaCard bus communication
- Optional programming voltage control
- Buffered data transfer
- Power management
- Data communication with a data rate up to 2 Mbyte/s

Ethernet Controller

The MAC controller implements the IEEE 802.3 and operates either at 100 Mbps or 10 Mbps. **Figure 10** shows a global view of the Ethernet Controller module with the module specific interface connections.

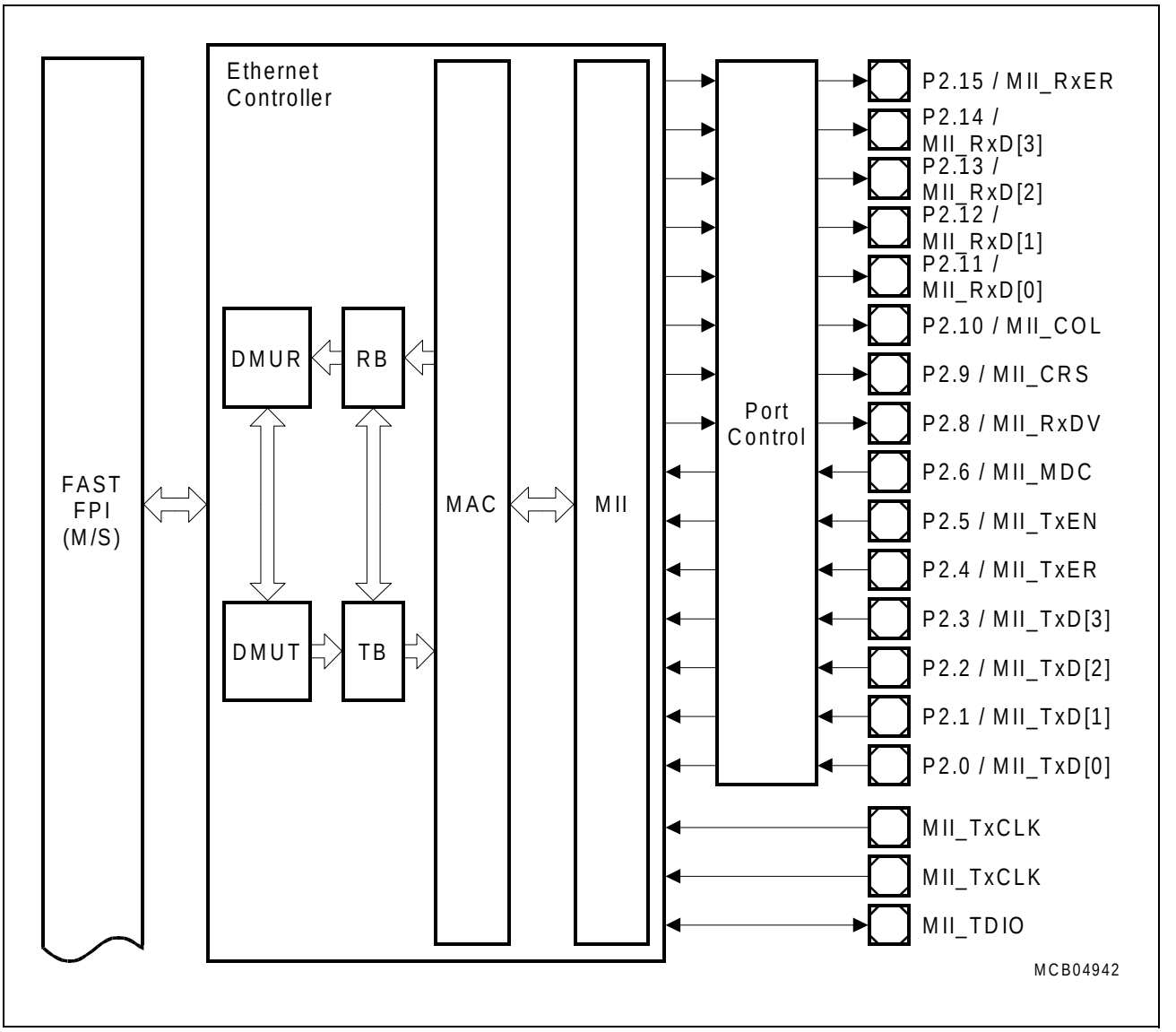


Figure 10 General Block Diagram of the Ethernet Controller

The Ethernet controller comprises the following functional blocks:

1. Media Access Controller (MAC)
2. Receive Buffer (RB)
3. Transmit Buffer (TB)
4. Data Management Unit in Receive Direction (DMUR)
5. Data Management Unit in Transmit Direction (DMUT)

RB as well as TB provides on-chip data buffering whereas DMUR and DMUT perform data transfer from/to the shared memory.

Two interfaces are provided by the Ethernet Controller Module:

1. MII interface for connection of Ethernet PHYs via eighteen Input / Output lines
2. Master/slave FPI bus interface for connection to the on-chip system bus for data transfer as well as configuration.

Features

- Media Independent Interface (MII) according to IEEE 802.3
- Support 10 or 100 Mbps MII-based Physical devices.
- Support Full Duplex Ethernet.
- Support data transfer between Ethernet Controller and COM-DRAM.
- Support data transfer between Ethernet Controller and SDRAM via EBU.
- 256 x 32 bit Receive buffer and Transmit buffer each.
- Support burst transfers up to 8 x 32 Byte.

Media Access Controller (MAC)

- 100/10-Mbps operations
- Full IEEE 802.3 compliance
- Station management signaling
- Large on-chip CAM (Content Addressable Memory)
- Full duplex mode
- 80-byte transmit FIFO
- 16-byte receive FIFO
- PAUSE Operation
- Flexible MAC Control Support
- Support Long Packet Mode and Short Packet Mode
- PAD generation

Media Independent Interface (MII)

- Media independence.
- Multi-vendor point of interoperability.
- Support connection of MAC layer and Physical (PHY) layer devices.
- Capable of supporting both 100 Mb/s and 10 Mb/s data rates.
- Data and delimiters are synchronous to clock references.
- Provides independent four bit wide transmit and receive data paths.
- Support connection of PHY layer and Station Management (STA) devices.
- Provides a simple management interface.
- Capable of driving a limited length of shielded cable.

PCI

The PCI Interface module of the TC11IB basically is a bus bridge between the on-chip FPI bus and the external PCI bus of the system. The PCI Interface is fully compliant to PCI Local Bus Specification Rev. 2.2. **Figure 11** shows a global view of the PCI module with the module specific pin connections.

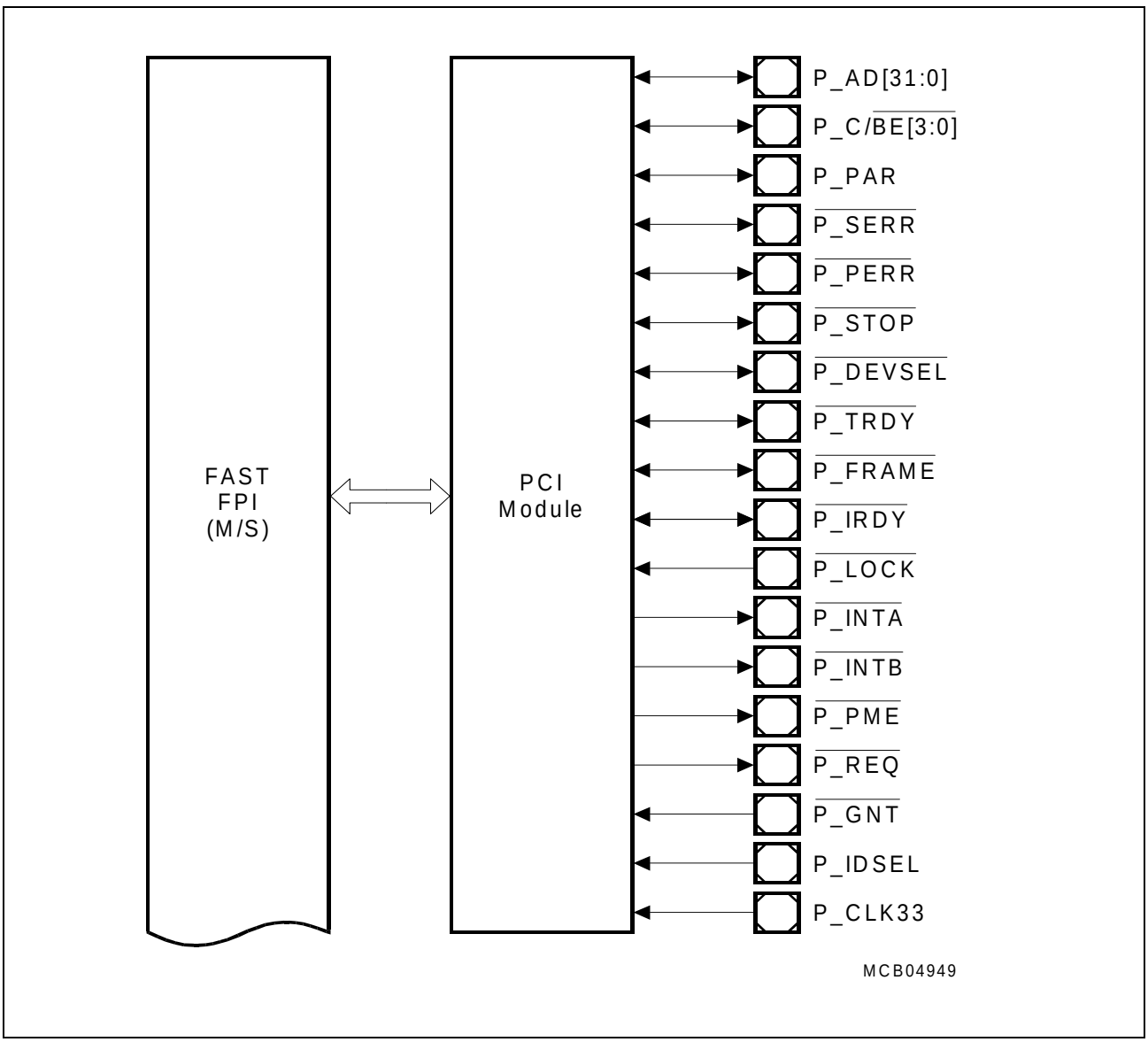


Figure 11 General Block Diagram of the PCI Interface

The PCI-FPI bridge is able to execute a number of various data transfers between the FPI bus and the PCI bus. Beside the standard PCI functions (configuration transactions), there are two main types of transfers which the bridge supports. Firstly, it will forward a transaction that any PCI initiator directs to the PCI interface of the TC11IB to the on-chip FPI bus. Secondly the bridge will forward certain transactions that a FPI master initiates on the FPI bus to the PCI bus. Depending on configuration, these transfers may be a

single data or burst transfers on both PCI and FPI bus. In addition, the bridge is able to handle a direct data transfer between PCI bus and FPI bus utilizing it's programmable DMA channel. The DMA channel can only be activated by a FPI master. In order to work as a PCI host bridge on the PCI bus, the variety of PCI transactions issued by the bridge includes configuration transactions of type 0 and type 1 when acting as a PCI master.

Features

- PCI V2.2 compliant, 32 bit, 33 MHz
- Multifunction Device, Support both PCI Master/Host functions. These functions can be activated by:
  - TriCore
  - Fast Ethernet
  - DMA Channel
- Support Burst Transfer from PCI to ComDRAM, SDRAM and LMU.
- Support DMA Channel data transfers between PCI and FPI
- Loading of PCI Configuration Registers done by TriCore via FPI Bus access
- Support PCI Command
- Support Card-Bus.
- Power management
  - according to PCI Bus Power Management Interface Specification V1.1
  - Support Multiple PCI power management states D0, D1, D2, $D3_{cold}$
  - PME#-Signalling from Fast Ethernet in D1, D2.
- PCI Reset
  - All tristatable PCI outputs of the bridge are set to "Tristate" upon PCI Reset, compliant to PCI Local Bus Specification V2.2

On-Chip Memories

The TC11IB provides the following on-chip memories:

- Program Memory Unit (PMU) with
  - 24 KBytes Scratch-pad Code RAM (SRAM)
  - 8 KBytes Instruction Cache Memory (I-CACHE)
- Data Memory Unit (DMU) with
  - 24 KBytes Scratch-pad Data RAM (SRAM)
  - 8 KBytes Data Cache Memory (D-CACHE)
- 16 KBytes Boot ROM (BROM)
- eDRAM Local Memory Unit (LMU) with
  - 512 KBytes Code/Data Memory
- ComDRAM with
  - 1MBytes Code/Data Memory
- Peripheral Control Processor (PCP) with
  - 16 KBytes Data Memory (PCODE)
  - 4 KBytes Parameter RAM (PRAM)

Address Map

Table 2 defines the specific segment oriented address blocks of the TC11IB with its address range, size, and PMU/DMU access view. Table 3 shows the block address map of the Segment 15 which includes on-chip peripheral units and ports.

Table 2 TC11IB Block Address Map

Segment	Address Range	Size	Description	DMU Acc.	PMU Acc.	
0 – 7	0000 0000$_H$ – 7FFF FFFF$_H$	2 GB	MMU/ FPI Space	via F_FPI	via F_ FPI	cached
8	8000 0000$_H$ – 8FFF FFFF$_H$	256 MB	External Memory Space mapped from Segment 10	via LMB	via LMB	
9	9000 0000$_H$ – 9FDF FFFF$_H$	254 MB	PCI Space mapped from Segment 11	via F_FPI	via F_FPI	
	9FE0 0000$_H$ – 9FEF FFFF$_H$	1 MB	ComDRAM Space mapped from Segment 11			
	9FF0 0000$_H$ – 9FFF FFFF$_H$	1 MB	Reserved	–	–	
10	A000 0000$_H$ – AFBF FFFF$_H$	252 MB	External Memory Space	via LMB	via LMB	non-cached
	AFC0 0000$_H$ – AFC7 FFFF$_H$	512 KB	LMU Space	via LMB	via LMB	
	AFC8 0000$_H$ – AFFF FFFF$_H$	3.5 MB	Reserved	–	–	
11	B000 0000$_H$ – BFDF FFFF$_H$	254 MB	PCI Space mappable into segment 9	via F_FPI	via F_FPI	
	BFE0 0000$_H$ – BFEF FFFF$_H$	1 MB	ComDRAM Space			
	BFF0 0000$_H$ – BFFF FFFF$_H$	1 MB	Reserved	–	–	
12	C000 0000$_H$ – C007 FFFF$_H$	512 KB	Local Memory Unit eDRAM Space	via LMB	via LMB	cached
	C008 0000$_H$ – CFFF FFFF$_H$	255.5 MB	Reserved	–	–	

Table 2 TC11IB Block Address Map(cont'd)

Seg-ment	Address Range	Size	Description	DMU Acc.	PMU Acc.	
13	D000 0000$_H$ – D000 5FFF$_H$	24 KB	Local Data Scratchpad Memory (SRAM)	DMU local	via LMB	non-cached
	D000 6000$_H$ – D3FF FFFF$_H$	~ 64 MB	Reserved	–	–	
	D400 0000$_H$ – D400 5FFF$_H$	24 KB	Local Code Scratchpad Memory (SRAM)	via LMB	PMU local	
	D400 6000$_H$ – D7FF FFFF$_H$	~64 MB	Reserved	–	–	
	D800 0000$_H$ – DDFF FFFF$_H$	96 MB	External Memory Space	via LMB	via LMB	
	DE00 0000$_H$ – DEFF FFFF$_H$	16 MB	Emulator Memory Space			
	DF00 0000$_H$ – DFFF BFFF$_H$	~16 MB	Reserved	–	–	
	DFFF C000$_H$ – DFFF FFFF$_H$	16 KB	Boot ROM Space	via S_FPI	via S_FPI	
14	E000 0000$_H$ – E7FF FFFF$_H$	128 MB	External Memory Space	via LMB	–	
	E800 0000$_H$ – E807 FFFF$_H$	512 KB	Local Memory Space mapped to LMB Segment 12	–		
	E808 0000$_H$ – E83F FFFF$_H$	3.5 MB	Reserved			
	E840 0000$_H$ – E840 7FFF$_H$	32 KB	Local Data Memory (SRAM) mapped to LMB Segment 13			
	E840 8000$_H$ – E84F FFFF$_H$	~1 MB	Reserved			
	E850 0000$_H$ – E850 7FFF$_H$	32 KB	Local Code Memory (SRAM) mapped to LMB Segment 13			
	E850 8000$_H$ – EFFF FFFF$_H$	~123 MB	Reserved			

Table 2 TC11IB Block Address Map(cont'd)

Seg-ment	Address Range	Size	Description	DMU Acc.	PMU Acc.	
15	F000 0000$_H$ – F00F FFFF$_H$	1 MB	On-Chip Peripherals & Ports	via S_FPI	via S_FPI	non-cached
	F010 0000$_H$ – F017 FFFF$_H$ [1)]	512 KB	Reserved	–	–	
	F018 0000$_H$ – F018 FFFF$_H$	64 KB	ComDRAM Control Registers	via S_FPI	via S_FPI	
	F019 0000$_H$ – F03F FFFF$_H$ [1)]	2.4375 MB	Reserved	–	–	
	F040 0000$_H$ – F04F FFFF$_H$	1 MB	PCI/FPI-Bridge Registers	via F_FPI	–	
	F050 0000$_H$ – F0FF FFFF$_H$	~11 MB	Reserved	–		
	F100 0000$_H$ – F1FF FFFF$_H$	16 MB	PCI Configuration Space	via F_FPI		
	F200 0000$_H$ – F200 05FF$_H$	6 x 256 B	BCU0 and Fast Ethernet Registers			
	F200 0600$_H$ – F7E0 FEFF$_H$	~94 MB	Reserved	–		
	F7E0 FF00$_H$ – F7E0 FFFF$_H$	256 B	CPU Slave Interface Registers (CPS)	via F_FPI		
	F7E1 0000$_H$ – F7E1 FFFF$_H$	64 KB	Core SFRs			
	F7E2 0000$_H$ – F7FF FFFF$_H$	15 x 128 KB	Reserved	–		
	F800 0000$_H$ – F87F FFFF$_H$	8 MB	LMB Peripheral Space (EBU_LMB and local memory eDRAM control registers)	via LMB		
	F880 0000$_H$ – FFFF FFFF$_H$	120 MB	Reserved	–		

1) Any access to this area will result in unpredicted behaviors of PORTs.

*Note: Accesses to address defined as "Reserved" in **Table 2** lead to a bus error. The exceptions are marked with 1)*

Table 3 Block Address Map of Segment 15

Symbol	Description	Address Range	Size
SCU	System Control Unit	F000 0000$_H$ – F000 00FF$_H$	256 Bytes
PCISIR	PCI Software Interrupt Request	F000 0100$_H$ – F000 01FF$_H$	256 Bytes
BCU1	Slow FPI Bus Control Unit 1	F000 0200$_H$ – F000 02FF$_H$	256 Bytes
STM	System Timer	F000 0300$_H$ – F000 03FF$_H$	256 Bytes
OCDS	On-Chip Debug Support	F000 0400$_H$ – F000 04FF$_H$	256 Bytes
–	Reserved	F000 0500$_H$ – F000 05FF$_H$	–
GPTU0	General Purpose Timer Unit 0	F000 0600$_H$ – F000 06FF$_H$	256 Bytes
GPTU1	General Purpose Timer Unit 1	F000 0700$_H$ – F000 07FF$_H$	256 Bytes
ASC	Async./Sync. Serial Interface	F000 0800$_H$ – F000 08FF$_H$	256 Bytes
16X50	Asynchronous Serial Interface	F000 0900$_H$ – F000 09FF$_H$	256 Bytes
SSC	High-Speed Synchronous Serial Interface	F000 0A00$_H$ – F000 0AFF$_H$	256 Bytes
MMCI	MultiMediaCard Interface	F000 0B00$_H$ – F000 0BFF$_H$	256 Bytes
SRU	Service Request Unit	F000 0C00$_H$ – F000 0DFF$_H$	512 Bytes
–	Reserved	F000 0E00$_H$ – F000 27FF$_H$	–
P0	Port 0	F000 2800$_H$ – F000 28FF$_H$	256 Bytes
P1	Port 1	F000 2900$_H$ – F000 29FF$_H$	256 Bytes
P2	Port 2	F000 2A00$_H$ – F000 2AFF$_H$	256 Bytes
P3	Port 3	F000 2B00$_H$ – F000 2BFF$_H$	256 Bytes
P4	Port 4	F000 2C00$_H$ – F000 2CFF$_H$	256 Bytes
P5	Port 5	F000 2D00$_H$ – F000 2DFF$_H$	256 Bytes
–	Reserved	F000 2E00$_H$ – F000 3EFF$_H$	–
PCP	PCP Registers	F000 3F00$_H$ – F000 3FFF$_H$	256 Bytes
	Reserved	F000 4000$_H$ – F000 FFFF$_H$	–
	PCP Data Memory (PRAM)	F001 0000$_H$ – F001 0FFF$_H$	4 KBytes
	Reserved	F001 1000$_H$ – F001 FFFF$_H$	–
	PCP Code Memory (PCODE)	F002 0000$_H$ – F002 3FFF$_H$	16 KBytes
–	Reserved	F002 4000$_H$ – F017 FFFF$_H$	–[1)]
Com-DRAM	ComDRAM Control Registers	F018 0000$_H$ – F018 FFFF$_H$	64 KBytes
–	Reserved	F019 0000$_H$ – F03F FFFF$_H$	–[1)]

Table 3 Block Address Map of Segment 15(cont'd)

Symbol	Description	Address Range	Size
PCI	PCI Bridge Configuration Registers	F040 0000$_H$ – F04F FFFF$_H$	1 MBytes
–	Reserved	F050 0000$_H$ – F0FF FFFF$_H$	–
PCI_CSx(x=1,2)	PCI Configuration Space Registers	F100 0000$_H$ – F1FF FFFF$_H$	16 MBytes
BCU0	Fast FPI Bus Control Unit 0	F200 0000$_H$ – F200 00FF$_H$	256 Bytes
ECU	Ethernet Controller Unit	F200 0100$_H$ – F200 05FF$_H$	1280 Bytes
–	Reserved	F200 0600$_H$ – F7E0 FEFF$_H$	–
CPU	Slave Interface Registers (CPS)	F7E0 FF00$_H$ – F7E0 FFFF$_H$	256 Bytes
	Reserved	F7E1 0000$_H$ – F7E1 7FFF$_H$	–
	MMU	F7E1 8000$_H$ – F7E1 80FF$_H$	256 BYTES
	Reserved	F7E1 8100$_H$ – F7E1 BFFF$_H$	–
	Memory Protection Registers	F7E1 C000$_H$ – F7E1 EFFF$_H$	12 KBytes
	Reserved	F7E1 F000$_H$ – F7E1 FCFF$_H$	–
	Core Debug Register (OCDS)	F7E1 FD00$_H$ – F7E1 FDFF$_H$	256 Bytes
	Core Special Function Registers (CSFRs)	F7E1 FE00$_H$ – F7E1 FEFF$_H$	256 Bytes
	General Purpose Register (GPRs)	F7E1 FF00$_H$ – F7E1 FFFF$_H$	256 Bytes
–	Reserved	F7E2 0000$_H$ – F7FF FFFF$_H$	–
EBU	EBU_LMB External Bus Unit	F800 0000$_H$ – F800 01FF$_H$	512 Bytes
–	Reserved	F800 0200$_H$ – F800 03FF$_H$	–
LMU	Local Memory Unit	F800 0400$_H$ – F800 04FF$_H$	256 Bytes
–	Reserved	F800 0500$_H$ – F87F FBFF$_H$	–
DMU	Local Data Memory Unit	F87F FC00$_H$ – F87F FCFF$_H$	256 Bytes
PMU	Local Program Memory Unit	F87F FD00$_H$ – F87F FDFF$_H$	256 Bytes
LCU	LMB Bus Control Unit	F87F FE00$_H$ – F87F FEFF$_H$	256 Bytes
LFI	LMB to FPI Bus Bridge (LFI)	F87F FF00$_H$ – F87F FFFF$_H$	256 Bytes
–	Reserved	F880 0000$_H$ – FFFF FFFF$_H$	–

1) Any access to this area will result in unpredicted behaviors of PORTs.

*Note: Accesses to address defined as “Reserved” in **Table 3** lead to a bus error.The exceptions are marked with [1)]*

Memory Protection System

The TC11IB memory protection system specifies the addressable range and read/write permissions of memory segments available to the currently executing task. The memory protection system controls the position and range of addressable segments in memory. It also controls the kinds of read and write operations allowed within addressable memory segments. Any illegal memory access is detected by the memory protection hardware, which then invokes the appropriate Trap Service Routine (TSR) to handle the error. Thus, the memory protection system protects critical system functions against both software and hardware errors. The memory protection hardware can also generate signals to the Debug Unit to facilitate tracing illegal memory accesses.

In SAF-T11IB-64D96, TriCore supports two address spaces: The virtual address space and The physical address space. Both address space are 4GB in size and divided into 16 segments with each segment being 256MB. The upper 4 bits of the 32-bit address are used to identify the segment. Virtual segments are numbered 0 - 15. But a virtual address is always translated into a physical address before accessing memory. The virtual address is translated into a physical address using one of two translation mechanisms: (a) direct translation, and (b) Page Table Entry (PTE) based translation. If the virtual address belongs to the upper half of the virtual address space then the virtual address is directly used as the physical address (direct translation). If the virtual address belongs to the lower half of the address space, then the virtual address is used directly as the physical address if the processor is operating in Physical mode (direct translation) or translated using a Page Table Entry if the processor is operating in Virtual mode (PTE translation). These are managed by Memory Management Unit (MMU)

Memory protection is enforced using separate mechanisms for the two translation paths.

Protection for direct translation

Memory protection for addresses that undergo direct translation is enforced using the range based protection that has been used in the previous generation of the TriCore architecture. The range based protection mechanism provides support for protecting memory ranges from unauthorized read, write, or instruction fetch accesses. The TriCore architecture provides up to four protection register sets with the PSW.PRS field controlling the selection of the protection register set. Because the TC11IB uses a Harvard-style memory architecture, each Memory Protection Register Set is broken down into a Data Protection Register Set and a Code Protection Register Set. Each Data Protection Register Set can specify up to four address ranges to receive particular protection modes. Each Code Protection Register Set can specify up to two address ranges to receive particular protection modes.

Each of the Data Protection Register Sets and Code Protection Register Sets determines the range and protection modes for a separate memory area. Each contains register pairs which determine the address range (the Data Segment Protection Registers and Code Segment Protection Registers) and one register (Data Protection Mode Register) which determines the memory access modes which apply to the specified range.

Protection for PTE based translation

Memory protection for addresses that undergo PTE based translation is enforced using the PTE used for the address translation. The PTE provides support for protecting a process from unauthorized read, write, or instruction fetches by other processes. The PTE has the following bits that are provided for the purpose of protection:

- XE (Execute Enable) enables instruction fetch to the page.
- WE (Write Enable) enables data writes to the page.
- RE (Read Enable) enables data reads from the page.

Furthermore, User-0 accesses to virtual addresses in the upper half of the virtual address space are disallowed when operating in Virtual mode. In Physical mode, User-0 accesses are disallowed only to segments 14 and 15. Any User-0 access to a virtual address that is restricted to User-1 or Super-visor mode will cause a Virtual Address Protection (VAP) Trap in both the Physical and Virtual modes.

On-Chip Bus System

The TC11IB includes two bus systems:

– Local Memory Bus (LMB)
– On-Chip FPI Bus (Fast FPI and Slow FPI)

There are two bridges to interconnect these three buses. The LMB-to-FPI (LFI) interfaces the Fast FPI bus to LMB Bus. The FPI-to-FPI (FFI) interfaces slow FPI bus to Fast FPI bus.

Local Memory Bus (LMB)

The Local Memory Bus interconnects the memory units and functional units, such as CPU and LMU. The main target of the LMB bus is to support devices with fast response times, optimized for speed. This allows the DMU and PMU fast access to local memory and reduces load on the FPI bus. The Tricore system itself is located on LMB bus. Via External Bus Unit, it interconnects TC11IB and external components.

The Local Memory Bus is a synchronous, pipelined, split bus with variable block size transfer support. It supports 8,16,32 & 64 bits single beat transactions and variable length 64 bits block transfers.

Key Features

The LMB provides the following features:

- Synchronous, Pipelined, Multi-master, 64-bit high performance bus
- Support multiple bus masters
- Support Split transactions
- Support Variable block size transfer
- Burst Mode Read/Write to Memories
- Connect Caches and on-chip memory and Fast FPI Bus

On-Chip FPI Bus

The FPI Bus interconnects the functional units of the TC11IB, such as the PCP and on-chip peripheral components. The FPI Bus is designed to be quick to acquire by on-chip functional units, and quick to transfer data. The low setup overhead of the FPI Bus access protocol guarantees fast FPI Bus acquisition, which is required for time-critical applications.The FPI Bus is designed to sustain high transfer rates. For example, a peak transfer rate of up to 800 MBytes/s can be achieved with a 100 MHz bus clock and 32-bit data bus. Multiple data transfers per bus arbitration cycle allow the FPI Bus to operate at close to its peak bandwidth. Via External Bus Unit (EBU), FPI Bus also interconnects the external components to TC11IB.

There are two FPI buses in TC11IB, Fast FPI Bus and Slow FPI Bus. In order to improve the system performance, the peripherals are splitted into two FPI buses based on their performance. The fast FPI bus runs at a speed of 96 MHz where most of the high performance peripheral like ComDRAM, PCI-FPI, Ethernet Controller, LFI etc. are connected. The slow FPI bus runs at half speed of its fast counter part. And it is used to connect some standard peripherals. There is a FPI-FPI bridge between them to transfer data. Each of FPI buses has its own Bus Control Unit (BCU).

Features

- Supports multiple bus masters
- Supports demultiplexed address/data operation
- Address bus up to 32 bits and data buses are 64 bits wide
- Data transfer types include 8-, 16-, 32- and 64 bit sizes
- Supports Burst transfer
- Single- and multiple-data transfers per bus acquisition cycle
- Designed to minimize EMI and power consumption
- Controlled by an Bus Control Unit (BCU)
  - Arbitration of FPI Bus master requests
  - Handling of bus error.

FFI-Bridge Features

- Supports Single/Block* Data Read/Write Transactions (8/16/32 Bit)
- Supports FPI- Read Modify Write Transactions (RMW)
- Internal FIFO Interfaces between FPI master and FPI slave.
- Optimized for FPI-Bus frequency ratios 2:1
- Special Retry/Abort functionality

Note: Block Transaction support depends on generic settings and the depth of the bridge internal read- and write data buffer.

LFI

The LMB-to-FPI Interface (LFI) block provides the circuitry to interface (bridge) the FPI bus to the Local Memory Bus (LMB).

LFI Features

- Compatible with the FPI 3.2 and LMB bus Specification V2.4
- Supports Burst/Single transactions, from FPI to LMB.
- Supports Burst/Single transactions, from LMB to FPI
- High efficiency and performance:
  - fastest access across the bridge takes three cycles, using a bypass.
  - There are no dead cycles on arbitration.
- Acts as the default master on FPI side.
- Supports abort, error and retry conditions on both sides of the bridge.
- Supports FPI's clock the same, or half, as the LMB's clock frequency.
- LMB clock is shut when no transactions are issue to LFI from both buses and none are in process in the LFI to minimize the power consumption.

LMB External Bus Unit

The LMB External Bus Control Unit (EBU_LMB) of the TC11IB is the interface between external resources, like memories and peripheral units, and the internal resources connected to on-chip buses if enabled. The basic structure and external interconnections of the EBU are shown in **Figure 12**.

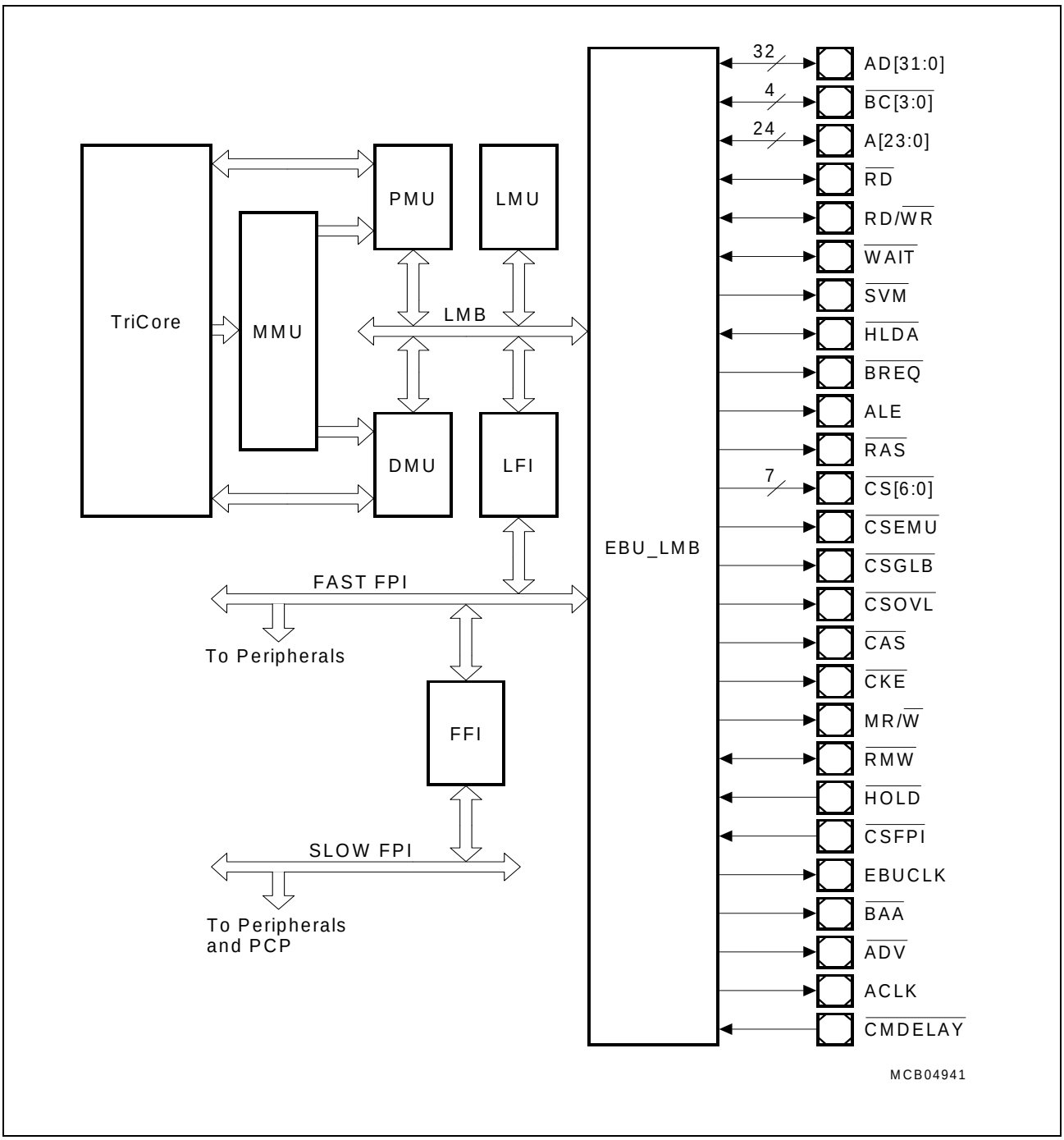


Figure 12 EBU Structure and Interfaces

The EBU is mainly used for the following two operations:

- Masters on LMB bus access external memories through EBU_LMB
- An external (off-chip) master access internal (on-chip) devices through FPI Bus.

The EBU controls all transactions required for these two operations and in particular handles the arbitration of the external bus between multi-masters.

The types of external resources accessed by the EBU are:

- INTEL style peripherals (separate $\overline{RD}$ and $\overline{WR}$ signals)
- Motorola style peripherals (MR/ $\overline{W}$ signals)
- ROMs, EPROMs
- Static RAMs
- PC 100 SDRAMs (Burst Read/Write Capacity / Multi-Bank/Page support)
- Specific types of Burst Mode Flashes (Intel 28F800F3/28F160F3, AMD 29BL162)
- Special support for external emulator/debug hardware

Features

- Support Local Memory Bus (LMB 64-bit)
- Support External bus frequency up to 96 MHz and internal LMB frequency up to 166 MHz. External bus frequency: LMB frequency =1:1 or 1:2 or 1:4
- Highly programmable access parameters
- Support Intel-and Motorola-style peripherals/devices
- Support PC 100 SDRAM (burst access, multibanking, precharge, refresh)
- Support 16-and 32-bit SDRAM data bus and 64,128 and 256MBit devices
- Support Burst flash (Intel 28F800F3/160F3,AMD 29BL162)
- Support Multiplexed access (address &data on the same bus) when PC 100 SDRAM is not implemented
- Support Address Alignment, external address space up to 64 MBytes.
- Support Data Buffering: Code Prefetch Buffer, Read/Write Buffer.
- External master arbitration compatible to C166 and other Tricore devices
- 8 programmable address regions (1 dedicated for emulator)
- Support Little-and Big-endian
- Signal for controlling data flow of slow-memory buffer
- Slave unit for external (off-chip) master to access devices on FPI bus

Peripheral Control Processor

The Peripheral Control Processor (PCP) performs tasks that would normally be performed by the combination of a DMA controller and its supporting CPU interrupt service routines in a traditional computer system. It could easily be considered as the host processor's first line of defense as an interrupt-handling engine. The PCP can off-load the CPU from having to service time-critical interrupts. This provides many benefits, including:

- Avoiding large interrupt-driven task context-switching latencies in the host processor
- Lessening the cost of interrupts in terms of processor register and memory overhead
- Improving the responsiveness of interrupt service routines to data-capture and data-transfer operations
- Easing the implementation of multitasking operating systems.

The PCP has an architecture which efficiently supports DMA type transactions to and from arbitrary devices and memory addresses within the TC11IB and also has reasonable stand alone computational capabilities.

The PCP is made up of several modular blocks as follows:

- PCP Processor Core
- Code Memory (PCODE)
- Parameter Memory (PRAM)
- PCP Interrupt Control Unit (PICU)
- PCP Service Request Nodes (PSRN)
- System bus interface to the slow FPI Bus

The PCP is fully interrupt-driven, meaning it is only activated through service requests; there is no main program running in the background as with a conventional processor.

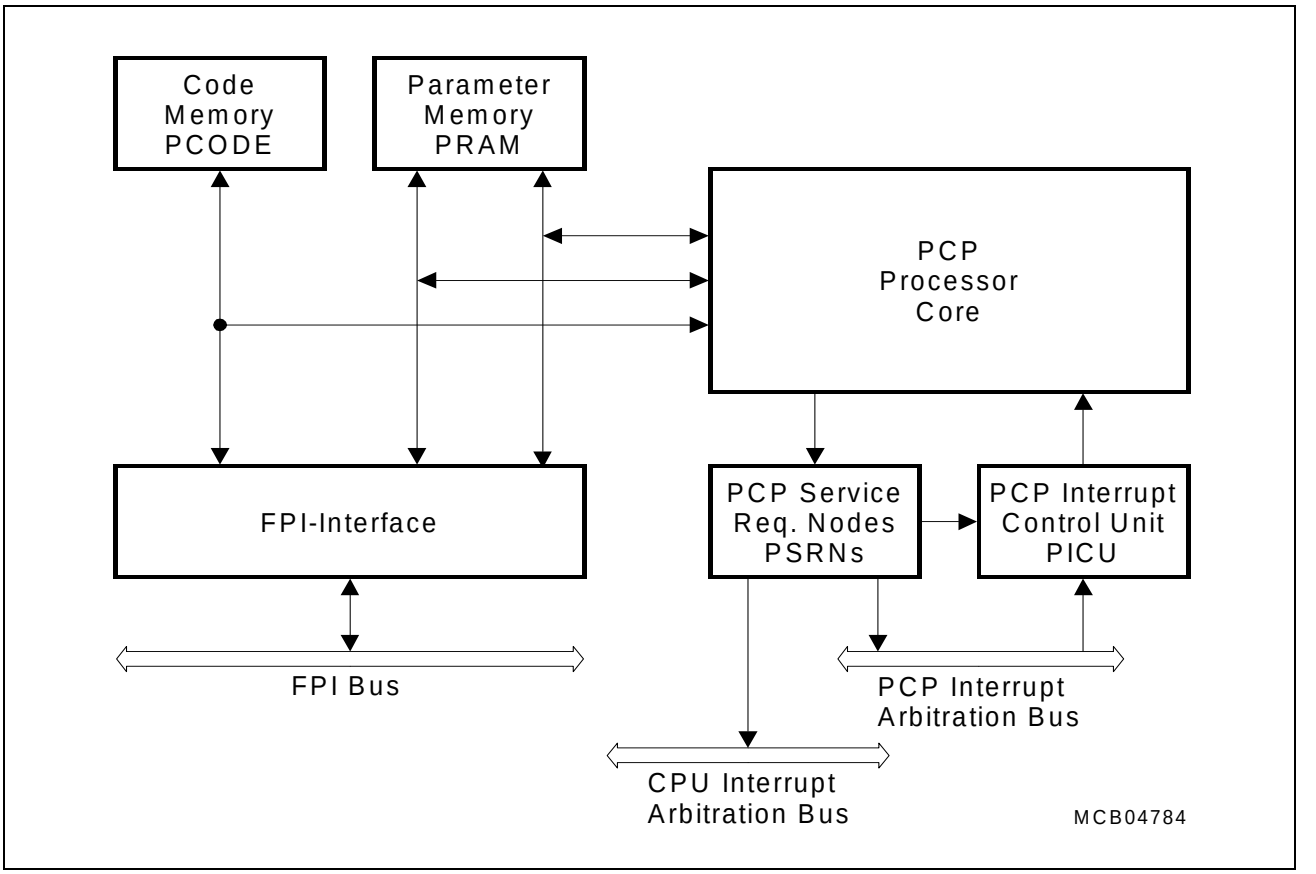


Figure 13 PCP Block Diagram

Table 4 PCP Instruction Set Overview

Instruction Group	Description
DMA primitives	Efficient DMA channel implementation
Load/Store	Transfer data between PRAM or FPI memory and the general purpose registers, as well as move or exchange values between registers
Arithmetic	Add, subtract, compare and complement
Divide/Multiply	Divide and multiply
Logical	And, Or, Exclusive Or, Negate, MCLR and MSET
Shift	Shift right or left, rotate right or left, prioritize
Bit Manipulation	Set, clear, insert and test bits
Flow Control	jump conditionally, jump long, exit, No operation
Miscellaneous	Debug

System Timer

The STM within the TC11IB is designed for global system timing applications requiring both high precision and long range. The STM provides the following features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Driven by clock, f_{STM} (identical with the system clock f_{SYS} = 48MHz).
- Counting begins at power-on reset
- Continuous operation is not affected by any reset condition except power-on reset

The STM is an upward counter, running with the system clock frequency. It is enabled per default after reset, and immediately starts counting up. Other than via reset, it is no possible to affect the contents of the timer during normal operation of the application, it can only be read, but not written to. Depending on the implementation of the clock control of the STM, the timer can optionally be disabled or suspended for power-saving and debugging purposes via a clock control register.

The maximum clock period is $2^{56} \times f_{STM}$. At f_{STM} = 48 MHz, for example, the STM counts 47.6 years before overflowing. Thus, it is capable of continuously timing the entire expected product life-time of a system without overflow.

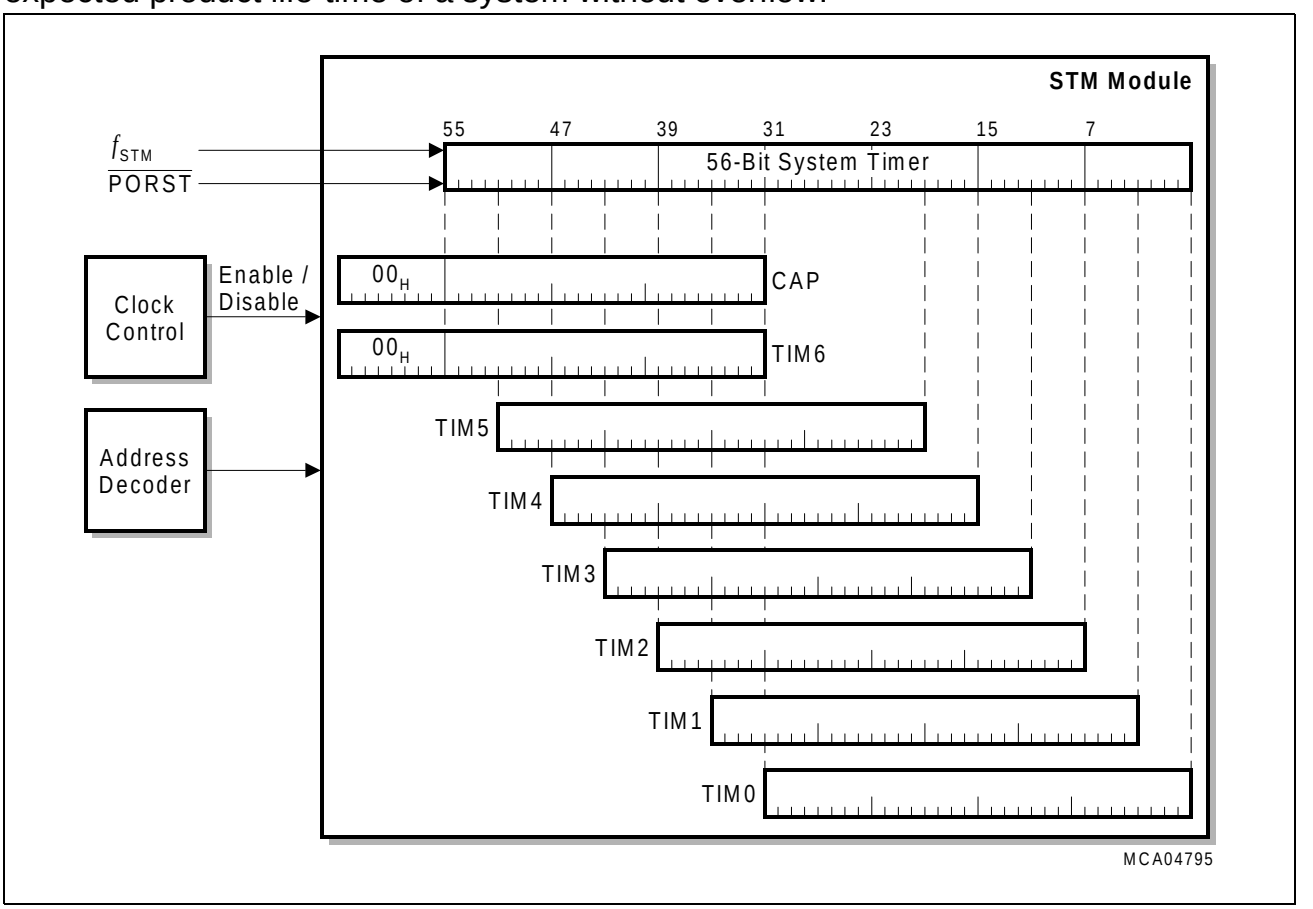


Figure 14 Block Diagram of the STM Module

Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC11IB in a user-specified time period. When enabled, the WDT will cause the TC11IB system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC11IB system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard “Watchdog” function, the WDT incorporates the EndInit feature and monitors its modifications. A system-wide line is connected to the ENDINIT bit implemented in a WDT control register, serving as an additional write-protection for critical registers (besides Supervisor Mode protection).

A further enhancement in the TC11IB’s Watchdog Timer is its reset prewarning operation. Instead of immediately resetting the device on the detection of an error, as known from standard Watchdogs, the WDT first issues an Non-maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, an important aid in debugging.

Features

- 16-bit Watchdog counter
- Selectable input frequency: $f_{SYS}/256$ or $f_{SYS}/16384$ (f_{SYS} = 48MHz)
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated password access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT and limited.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation.
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation.
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled.
- Double Reset Detection: If a Watchdog induced reset occurs twice without a proper access to its control register in between, a severe system malfunction is assumed and the TC11IB is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed.

- Important debugging support is provided through the reset prewarning operation by first issuing an NMI to the CPU before finally resetting the device after a certain period of time.

System Control Unit

The System Control Unit (SCU) of the TC11IB handles the system control tasks. All these system functions are tightly coupled, thus, they are conveniently handled by one unit, the SCU. The system tasks of the SCU are:

- PLL Control
  - PLL_CLC Clock Control Register
  - f_{SYS} = 96MHz clock generation.
  - f_{SYS} = 48MHz clock generation.
- Reset Control
  - Generation of all internal reset signals
  - Generation of external $\overline{\text{HDRST}}$ reset signal
  - Generation of LMU eDRAM reset signals
- Boot Scheme
  - Hardware Booting Scheme
  - Software Booting Scheme
- Power Management Control
  - Enabling of several power-down modes
  - Control of the PLL in power-down modes
- Watchdog Timer
- OCDS2 Trace Port Control
- Selection between PCI and Cardbus (PCMCIA) Standard Compliance
- FFI Bridge Control
- Device Identification Registers

Interrupt System

An interrupt request can be serviced either by the CPU or by the Peripheral Control Processor (PCP). These units are called “Service Providers”. Interrupt requests are called “Service Requests” rather than “Interrupt Requests” in this document because they can be serviced by either of the Service Providers.

Each peripheral in the TC11IB can generate service requests. Additionally, the Bus Control Unit, the Debug Unit, the PCP, and even the CPU itself can generate service requests to either of the two Service Providers. As shown in **Figure 15**, each TC11IB unit that can generate service requests is connected to one or multiple Service Request Nodes (SRN). Each SRN contains a Service Request Control Register mod_SRCx, where “mod” is the identifier of the service requesting unit and “x” an optional index. Two buses connect the SRNs with two Interrupt Control Units, which handle interrupt arbitration among competing interrupt service requests, as follows:

- The Interrupt Control Unit (ICU) arbitrates service requests for the CPU and administers the CPU Interrupt Arbitration Bus.
- The Peripheral Interrupt Control Unit (PICU) arbitrates service requests for the PCP and administers the PCP Interrupt Arbitration Bus.

Units which can generate service requests are:

- General Purpose Timer Units (GPTU 0 and GPTU 1) with 8 SRNs each
- High-Speed Synchronous Serial Interfaces (SSC) with 3 SRNs
- Asynchronous/Synchronous Serial Interfaces (ASC) with 4 SRNs
- Asynchronous Serial Interface (16X50) with 1 SRN
- PCI with 33 SRNs
- Ethernet Controller with 9 SRNs
- MultiMediaCard (MMCI) with 1 SRN
- External Interrupts with 24 SRNs
- Bus Control Units (BCU0 and BCU1) with 1 SRN each
- Peripheral Control Processor (PCP) with 12 SRNs
- Central Processing Unit (CPU) with 4 SRNs
- Debug Unit (OCDS) with 1 SRN

The PCP can make service requests directly to itself (via the PICU), or it can make service requests to the CPU. The Debug Unit can generate service requests to the PCP or the CPU. The CPU can make service requests directly to itself (via the ICU), or it can make service requests to the PCP. The CPU Service Request Nodes are activated through software.

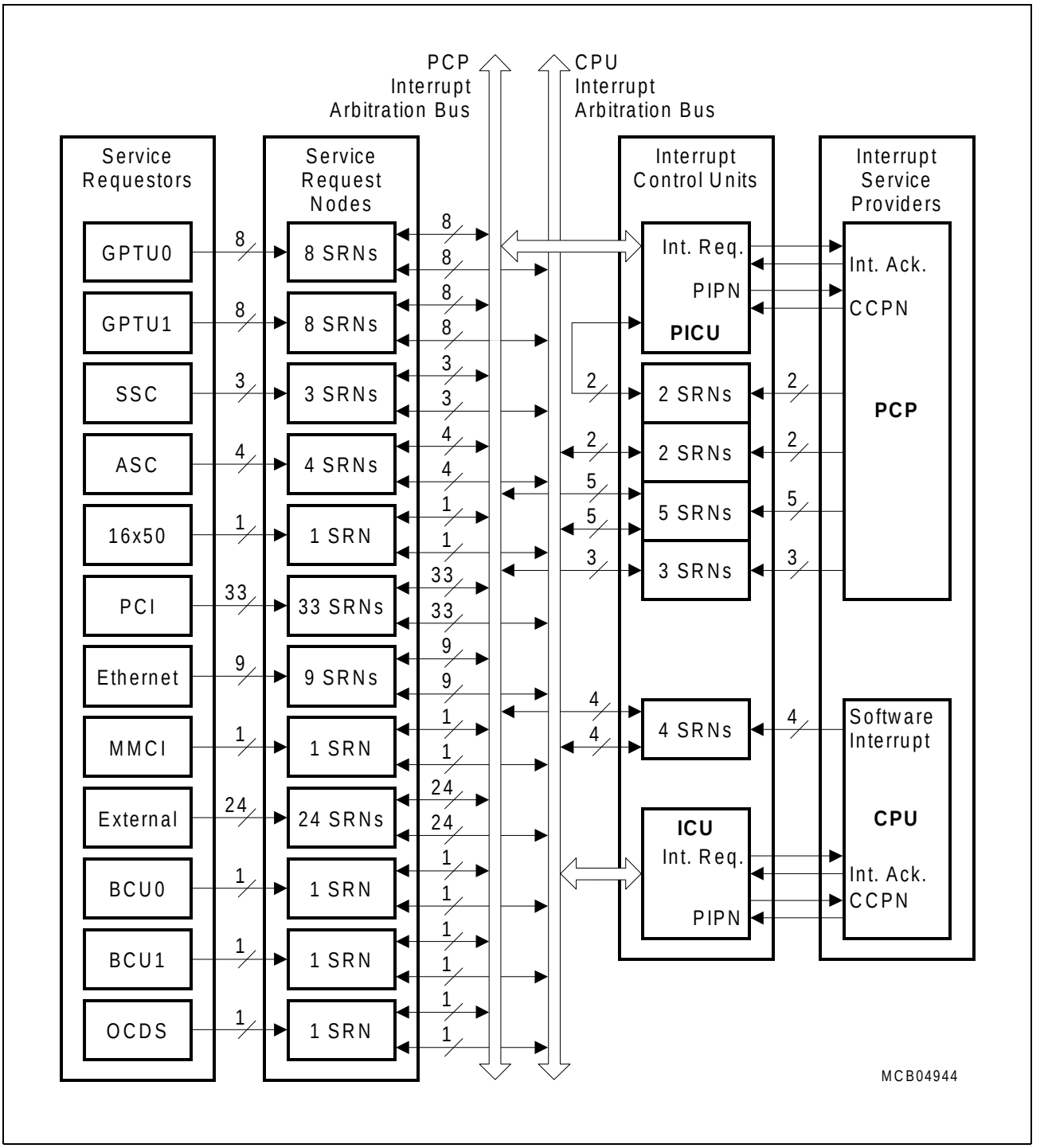


Figure 15 Block Diagram of the TC11IB Interrupt System

Boot Options

The TC11IB booting schemes provides a number of different boot options for the start of code execution. **Table 5** shows the boot options available in the TC11IB.

Table 5 Boot Selections

$\overline{\text{OCDSE}}$	$\overline{\text{BRKIN}}$	CFG [3]	CFG [2:0]	Type of Boot	Boot Source	Initial PC Value
1	1	X	000_B	Start directly in core scratchpad memory	SRAM (Only via SW Reset)	D400 0000_H
			Not (000 or 100)	Start from Boot ROM	Boot ROM, SSC BSL mode[1] (BootStrap Loader) or ASC BSL mode[1]	DFFF $FFFC_H$
		0	100_B	External memory as slave directly via EBU	External Memory (non-cached, CS0)	A000 0000_H
		1	100_B	External memory as master directly via EBU		
1	0	don't care		Tri-state chip (deep sleep)	–	–
0	1	0	100_B	Go to halt with EBU enabled as slave	–	–
		1		Go to halt with EBU enabled as master		
		all other combina-tions		Go to halt with EBU disabled		
0	0	don't care		Go to external emulator space	–	DE00 0000_H

1) SSC/ASC BootStrap Loader is built in BOOT ROM which provides a mechanism to load the startup program, which is executed after reset, via the SSC/ASC interface. After successfully loaded, the startup program will be executed from the address at 0xC000 0004_H.

Power Management System

The TC11IB power management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application.

There are four power management modes:

- Run Mode
- Idle Mode
- Sleep Mode
- Deep Sleep Mode

Table 6 describes these features of the power management modes.

Table 6 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the $\overline{\text{NMI}}$ pin, or any enabled interrupt event will return the system to Run Mode.
Sleep	The system clock continues to be distributed only to those peripherals programmed to operate in Sleep Mode. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the $\overline{\text{NMI}}$ pin, or a reset event will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.
Deep Sleep	The system clock is shut off; only an external signal will restart the system. Entering this state requires an orderly shut-down controlled by the Power Management State Machine (PMSM).

Besides these explicit software-controlled power-saving modes, TC11IB supports automatic power-saving in that operating units, which are currently not required or idle, are shut off automatically until their operation is required again.

On-Chip Debug Support

The On-Chip Debug Support of the TC11IB consists of four building blocks:

- OCDS module in the TriCore CPU
  - On-chip breakpoint hardware
  - Support of an external break signal
- OCDS module in the PCP
  - Special DEBUG instruction for program execution tracing
- Trace module of the TriCore
  - Outputs 16 bits per cycle with pipeline status information, PC bus information, and breakpoint qualification information
- Debugger Interface (Cerberus)
  - Provided for debug purposes of emulation tool vendors
  - Accessible through a JTAG standard interface with dedicated JTAG port pins

Figure 16 shows a basic block diagram of the building blocks.

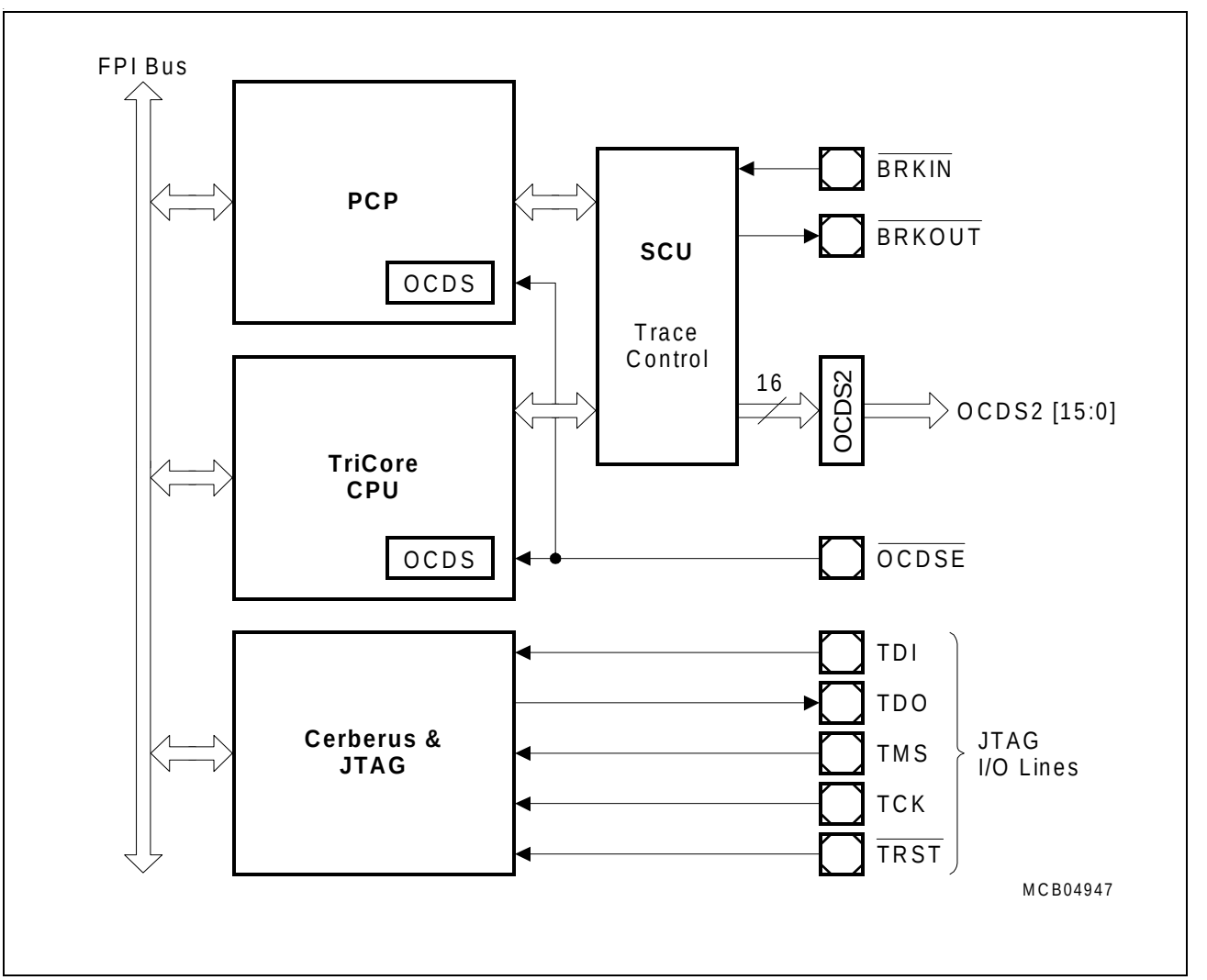


Figure 16 OCDS Support Basic Block Diagram

Clock Generation Unit

The Clock Generation Unit in the TC11IB, shown in **Figure 17**, consists of an oscillator circuit and one Phase-Locked Loop (PLL). The PLL can convert a low-frequency external clock signal to a high-speed internal clock for maximum performance. The PLL also has fail-safe logic that detects degenerate external clock behavior such as abnormal frequency deviations or a total loss of the external clock. It can execute emergency actions if it losses the lock on the external clock. PLL can provide the 96MHz and 48MHz clocks.

In general, the Clock Generation Unit (CGU) is controlled through the System Control Unit (SCU) module of the TC11IB.

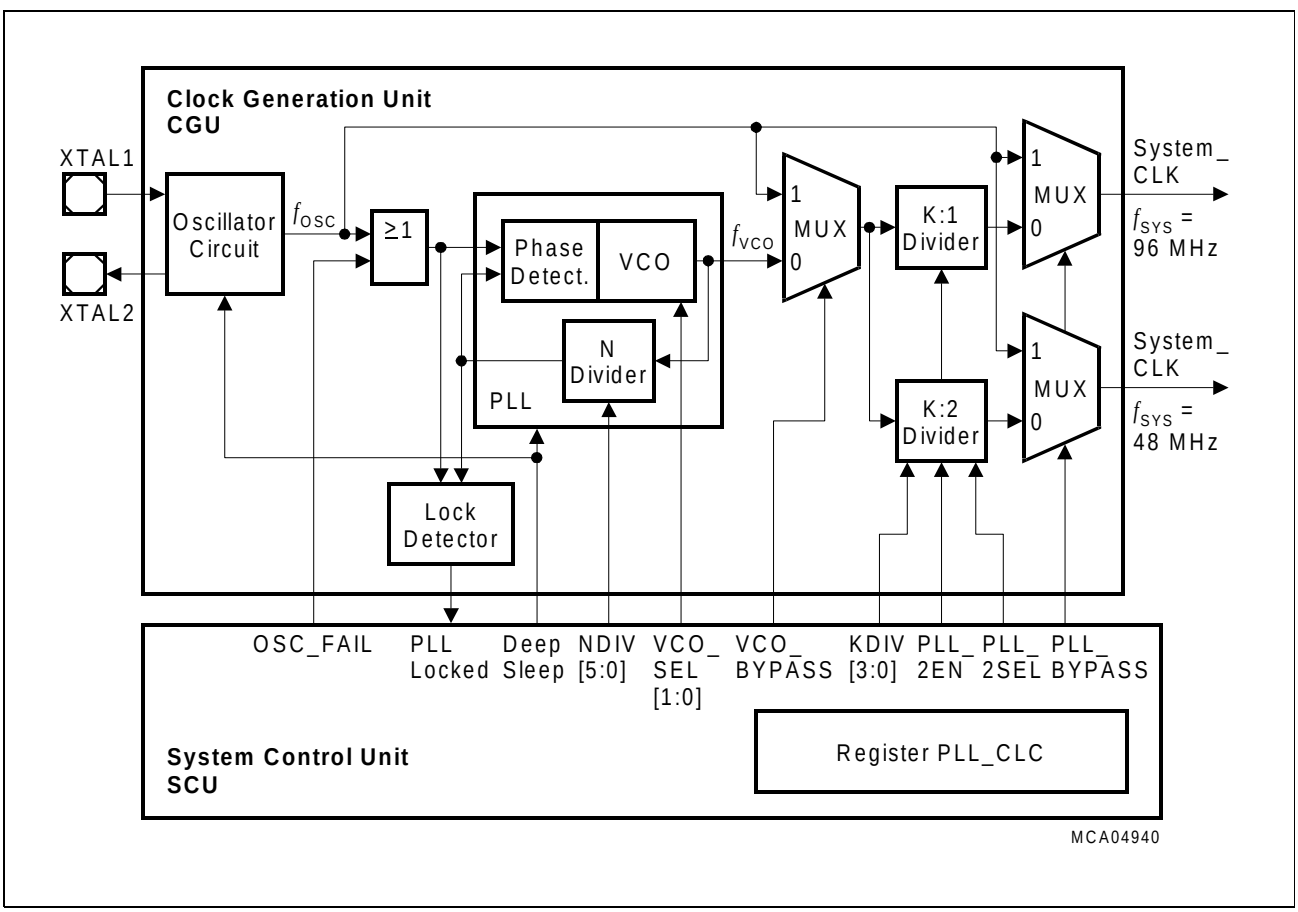


Figure 17 Clock Generation Unit Block Diagram

Recommended Oscillator Circuits

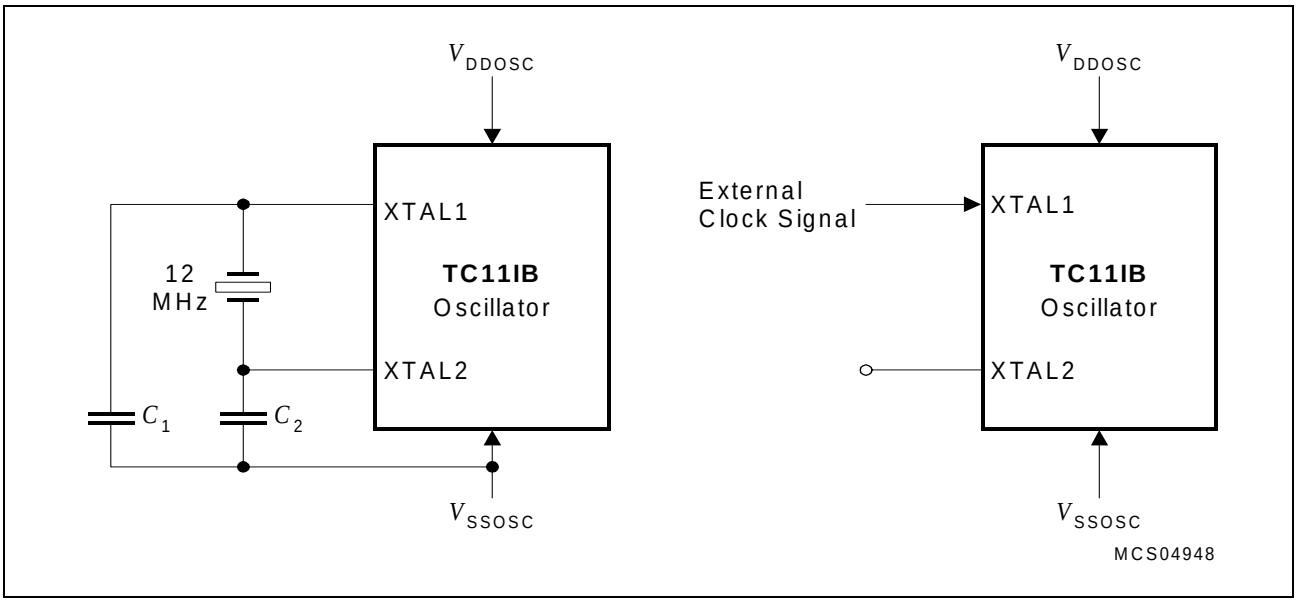


Figure 18 Oscillator Circuitries

For the main oscillator of the TC11IB the following external passive components are recommended:

- Crystal: 12 MHz
- C1, C2: 10 pF

A block capacitor between V_{DDOSC} and V_{SSOSC} is recommended, too.

Power Supply

The TC11IB provides an ingenious power supply concept in order to improve the EMI behavior as well as to minimize the crosstalk within on-chip modules.

Figure 19 shows the TC11IB's power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling.

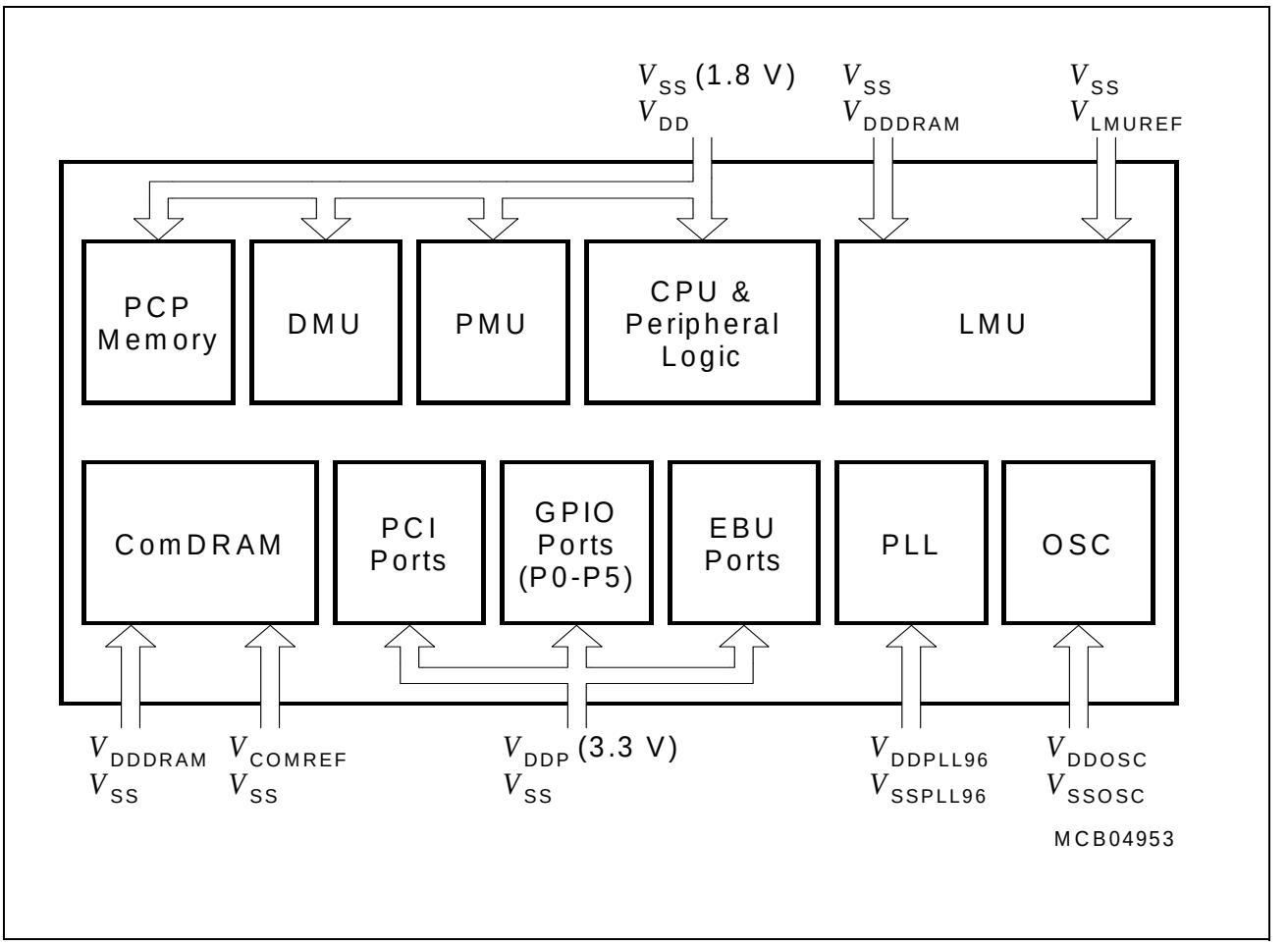


Figure 19 TC11IB Power Supply Concept

Identification Register Values

Table 7 TC11IB Identification Registers

Short Name	Address	Value
SCU_ID	F000 0008$_H$	0013 C002$_H$
MANID	F000 0070$_H$	0000 1820$_H$
CHIPID	F000 0074$_H$	0000 8502$_H$
RTID	F000 0078$_H$	0000 0000$_H$
BCU1_ID	F000 0208$_H$	0000 6A06$_H$
STM_ID	F000 0308$_H$	0000 C002$_H$
JPD_ID	F000 0408$_H$	0000 6302$_H$
GPTU0_ID	F000 0608$_H$	0001 C002$_H$
GPTU1_ID	F000 0708$_H$	0001 C002$_H$
ASC_ID	F000 0808$_H$	0000 4461$_H$
16X50_ID	F000 0908$_H$	0012 C001$_H$
SSC_ID	F000 0A08$_H$	0000 4503$_H$
MMCI_ID	F000 0B08$_H$	0000 5B01$_H$
PCP_ID	F000 3F08$_H$	0020 C002$_H$
PCI_ID	F040 0034$_H$	0001 15D1$_H$
PCI_SUBID	F040 0038$_H$	0000 15D1$_H$
PCI_CS1_ID	F100 0000$_H$	0001 15D1$_H$
PCI_CS1_SUBID	F100 002C$_H$	0001 15D1$_H$
PCI_CS2_ID	F100 0100$_H$	0001 15D1$_H$
PCI_CS2_SUBID	F100 012C$_H$	0002 15D1$_H$
BCU0_ID	F200 0008$_H$	0000 6A06$_H$
CPU_ID	F7E0 FF18$_H$	0015 C004$_H$
MMU_ID	F7E1 8008$_H$	0009 C002$_H$
EBU_ID	F800 0008$_H$	0014 C003$_H$
LMU_ID	F800 0410$_H$	0016 C001$_H$
DMU_ID	F87F FC08$_H$	0008 C002$_H$
PMU_ID	F87F FD08$_H$	000B C002$_H$
LCU_ID	F87F FE08$_H$	000F C003$_H$
LFI_ID	F87F FF08$_H$	000C C003$_H$

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	–25	85	°C	under bias
Storage temperature	T_{ST}	–65	150	°C	
Junction temperature	T_J	–	110	°C	under bias
Voltage on I/O Supply pins with respect to ground (V_{SS})	V_{DDP}	–0.5	4.5	V	
Voltage on Core Supply pins with respect to ground (V_{SS})	V_{DD}	–0.3	2.4	V	
Voltage on PLL Supply pins with respect to ground (V_{SS})	V_{DDPLL}	–0.3	2.4	V	
Voltage on Oscillator Supply pins with respect to ground (V_{SS})	V_{DDOSC}	–0.3	2.4	V	
Voltage on eDRAM Supply pins with respect to ground (V_{SS})	V_{DDDRAM}	–0.3	2.4	V	
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	–0.5	4.5	V	
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	ΣI_{IN}	–	|100|	mA	
Power dissipation	P_{DISS}	–	1.6	W	

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN}>V_{DD}$ or $V_{IN}<V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC11IB. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DDP}	3.0	3.6	V	I/O supply
	V_{DD}	1.71	1.89	V	Core supply
	V_{DDPLL}	1.71	1.89	V	PLL supply
	V_{DDOSC}	1.71	1.89	V	Oscillator supply
	V_{DDDRAM}	1.71	1.89	V	eDRAM supply
Ground voltage	V_{SS}	0		V	
Ambient temperature under bias	T_A	–25	85	°C	
CPU clock	f_{CPU}	–	96	MHz	
External Load Capacitance	C_L	–	50	pF	

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the TC11IB and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the TC11IB will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective characteristics to the TC11IB.

DC Characteristics

DC-Characteristics

V_{SS} = 0 V; T_A = -25 °C to +85 °C

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
GPIO pins, Dedicated pins and EBU pins						
Input low voltage	V_{IL}	SR	–	0.8	V	
Input high voltage	V_{IH}	SR	2.0	–	V	
Output low voltage	V_{OL}	CC	–	0.4	V	
Output high voltage	V_{OH}	CC	2.4	–	V	
Pull-up current [1]	I_{PUB}	CC	–37	–12	µA	V_{IN} = 0V
	I_{PUC}	CC	–12	–2	µA	V_{IN} = 0V
Pull-down current [2]	I_{PDA}	CC	55	220	µA	V_{IN} = V_{DDP}
	I_{PDC}	CC	2	14	µA	V_{IN} = V_{DDP}
Input leakage current [3]	I_{OZ2}	CC	–	±1	µA	0 < V_{IN} < V_{DDP}
Pin Capacitance [4]	C_{IO}	CC	–	10	pF	
PCI pins						
Input low voltage	V_{ILP}	SR	–0.5	0.3V_{DDP}	V	
Input high voltage	V_{IHP}	SR	0.5V_{DDP}	V_{DDP} + 0.5	V	
Output low voltage	V_{OLP}	CC	–	0.1V_{DDP}	V	I_{OLP} = 1500µA
Output high voltage	V_{OHP}	CC	0.9V_{DDP}	–	V	I_{OHP} = –500µA
Input Pull-up voltage [5]	V_{IPU}	CC	0.7V_{DDP}	–		
Input leakage current [6]	I_{IL}	CC	–	±10	µA	0 < V_{IN} < V_{DDP}
$\overline{\text{PME}}$ input leakage [7]	I_{OFF}	CC	–	1	µA	V_{IN} ≤ 3.6V V_{DD} off or floating
Input pin capacitance [8]	C_{IN}	CC	–	10	pF	
CLK pin capacitance	C_{CLK}	CC	5	12	pF	

DC-Characteristics(cont'd)

V_{SS} = 0 V; T_A = -25 °C to +85 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
IDSEL pin capacitance [9]	C_{IDSEL} CC	–	8	pF	
Pin inductance	L_{PIN} CC	–	20	nH	

Oscillator Pins

Input low voltage at XTAL1	V_{ILX} SR	-0.3	0.3 × V_{DDOSC}	V	
Input high voltage at XTAL1	V_{IHX} SR	0.7 × V_{DDOSC}	2.4	V	

Notes:

1) The current is applicable to the pins, for which a pull up has been specified. Refer to **Table 1**. I_{PUx} refers to the pull up current for type *x*.

2) The current is applicable to the pins, for which a pull down has been specified. Refer to **Table 1**. I_{PDx} refers to the pull down current for type *x*.

3) Pins with internal pull up or pull down are not included.

4) Not 100% tested, guaranteed by design characterization.

5) This specification is guaranteed by design. It is the minimum voltage to which pull up resistors are calculated to pull a floated network. Applications sensitive to static power utilization must assure that the input buffer is conducting minimum current at this input voltage.

6) Input leakage currents include high impedance output leakage for all bi-directional buffers with tristate outputs.

7) This input leakage is the maximum allowable leakage into the $\overline{\text{PME}}$ open drain driver when power is removed from VDD of the component. This assumes that no event has occurred to cause the device to attempt to assert $\overline{\text{PME}}$.

8) Absolute maximum pin capacitance for a PCI input is 10pF (except for CLK). Exceptions are granted to motherboard-only devices up to 16pF.

9) Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

Power Supply Current

Parameter	Symbol	Limit values		Unit	Test Conditions
		typ. [1]	max.		
Active mode supply current	I_{DD}	477.8	629	mA	Sum of I_{DDS} [2][3]
		414.4	519	mA	I_{DD} at V_{DD} [4]
		39.0	60	mA	I_{DD} at V_{DDP}
		24.4	50	mA	I_{DD} at V_{DDDRAM} [2]
Idle mode supply current	I_{ID}	214.4	308	mA	Sum of I_{DDS} [2][3][5]
		191.7	259	mA	I_{DD} at V_{DD} [4][5]
		12.7	20	mA	I_{DD} at V_{DDP} [5]
		10.0	29	mA	I_{DD} at V_{DDDRAM} [2][5]
Sleep mode supply current	I_{SL}	196.7	288	mA	Sum of I_{DDS} [2][3][6]
		174.0	239	mA	I_{DD} at V_{DD} [4][6]
		12.7	20	mA	I_{DD} at V_{DDP} [6]
		10.0	29	mA	I_{DD} at V_{DDDRAM} [2][6]
Deep sleep mode supply current	I_{DS}	12.5	69	mA	Sum of I_{DDS} [2][3][7]
		3.3	41	mA	I_{DD} at V_{DD} [4][7]
		5.7	10	mA	I_{DD} at V_{DDP} [7]
		3.5	18	mA	I_{DD} at V_{DDDRAM} [2][7]

1) Typical values are measured at 25°C, CPU clock at 96MHz and nominal supply voltage, i.e. 3.3V for V_{DDP} and 1.8V for V_{DD}, V_{DDPLL}, V_{DDOSC} and V_{DDDRAM}. These currents are measured using a typical application pattern. The power consumption of modules can increase or decrease using other application programs. The PLL is bypassed while PCI and MMCI modules are inactive.

2) The current is measured by following this sequence: during the power on reset ($\overline{PORST}$ = V_{IL}) active, the configuration pins are set as follow:
TESTMODE = 1; CFG0 = 1; CFG1 = 1; CFG2 = 0; CFG3 = 0
Thereafter, these inputs are set to the levels based on the desired operational mode, which are switched before the power on reset pin $\overline{PORST}$ goes inactive. This sequence achieves low eDRAM current. Otherwise, there may be a current offset around 150 mA.

3) These power supply currents are defined as the sum of all currents at the V_{DD} power supply lines:
V_{DD} + V_{DDP} + V_{DDDRAM} + V_{DDPLL} + V_{DDOSC}

4) This measurement includes the TriCore and Logic power supply lines.

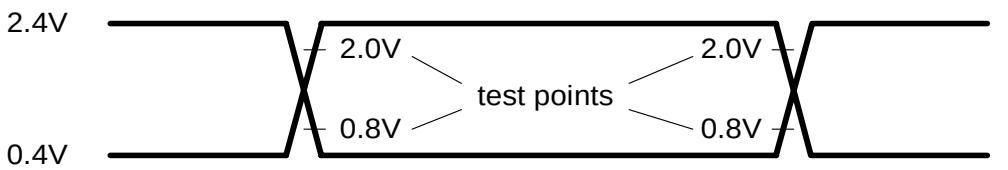
5) CPU is in idle state, input clock to all peripherals are enabled,

6) Input clock to all peripherals are disabled.

7) Clock generation is disabled at the source.

AC Characteristics

(Operating Conditions apply)



AC inputs during testing are driven at 2.4V for a logic “1” and 0.4V for a logic “0”. Timing measurements are made at V_{IHmin} for a logic “1” and V_{ILmax} for a logic “0”.

Figure 20 Input/Output Waveforms for AC Tests - for GPIO, Dedicated and EBU pins

Input Clock Timing
(Operating Conditions apply)

Parameter		Symbol	Limits		Unit
			min	max	
Oscillator clock frequency	with PLL	f_{OSC} SR	12		MHz
Input clock frequency driving at XTAL1	with PLL	f_{OSCDD} SR	12		MHz
Input Clock high time		t_1 SR	37.5	–	ns
Input Clock low time		t_2 SR	37.5	–	ns
Input Clock rise time		t_3 SR	–	4.1	ns
Input Clock fall time		t_4 SR	–	4.1	ns

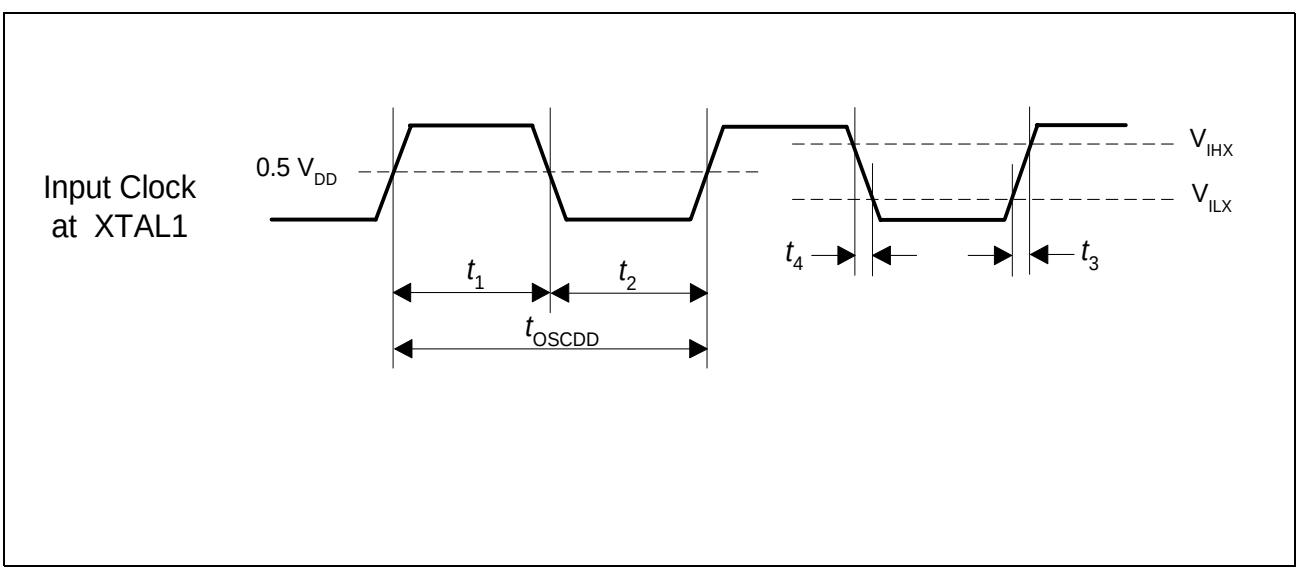


Figure 21 Input Clock Timing

CPU Clock Timing
(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limits		Unit
		min	max	
CPUCLK period	t_{CPUCLK} CC	10.4	–	ns
CPUCLK high time	t_1 CC	3	–	ns
CPUCLK low time	t_2 CC	4.5	–	ns
CPUCLK rise time	t_3 CC	–	2.8	ns
CPUCLK fall time	t_4 CC	–	2.2	ns

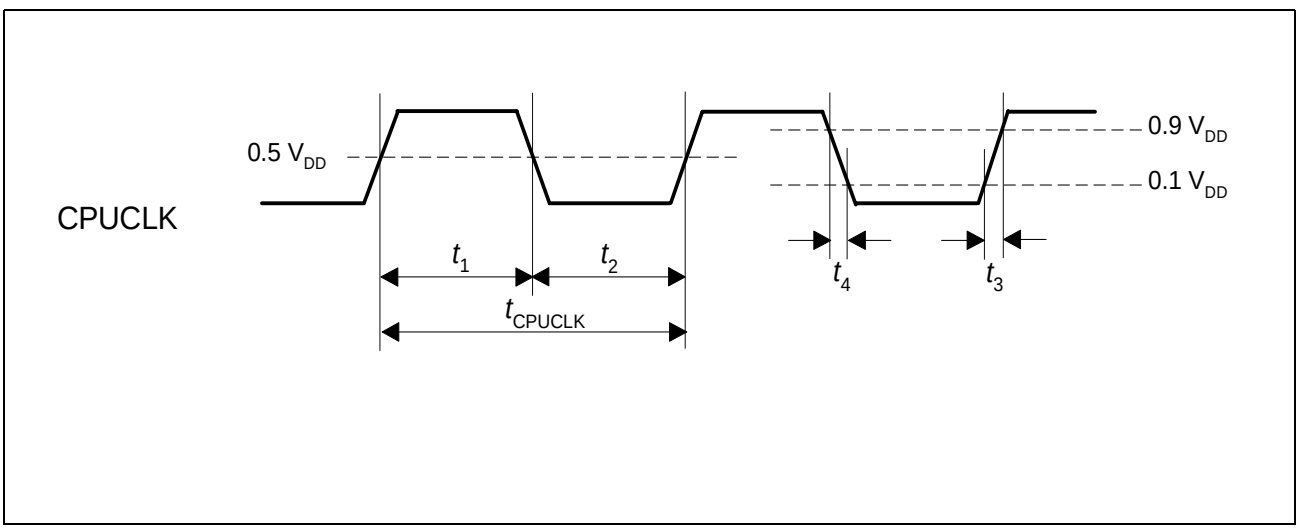


Figure 22 CPUCLK Timing

Timing for eDRAM Refresh Cycle

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limits		Unit
		min	max	
eDRAM retention time	t_{TRET} CC	–	16	ms
LMU eDRAM refresh cycle time	t_{REF} CC	–	1.6	µs
ComDRAM eDRAM refresh cycle time	t_{REF} CC	–	0.8	µs

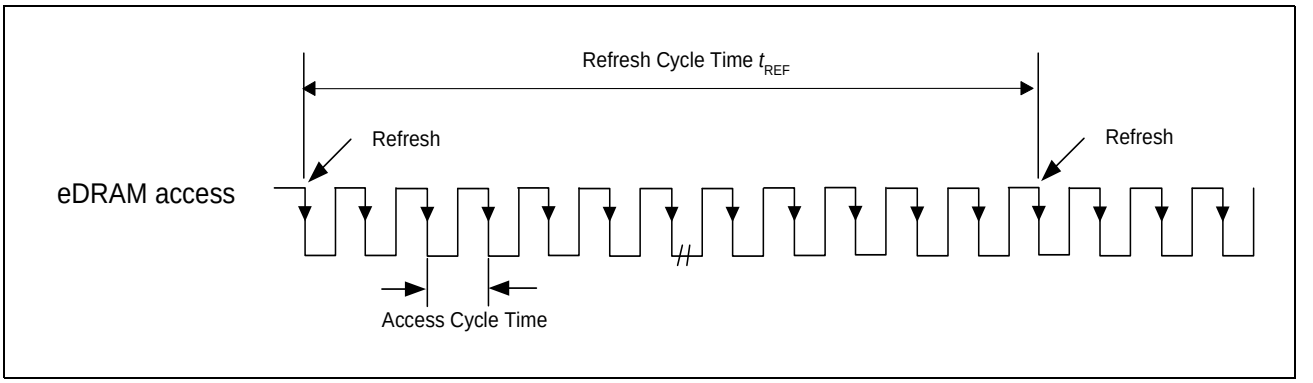


Figure 23 eDRAM Refresh Cycle Timing

Timing for EBU_LMB Clock Outputs
(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
EBUCLK period	t_1	CC	10.4	–	ns
EBUCLK high time	t_2	CC	4.5	–	ns
EBUCLK low time	t_3	CC	3	–	ns
EBUCLK rise time	t_4	CC	–	2.5	ns
EBUCLK fall time	t_5	CC	–	2.5	ns
ACLK period	t_6	CC	20	–	ns
ACLK high time	t_7	CC	9	–	ns
ACLK low time	t_8	CC	9	–	ns
ACLK rise time	t_9	CC	–	3.5	ns
ACLK fall time	t_{10}	CC	–	2.5	ns

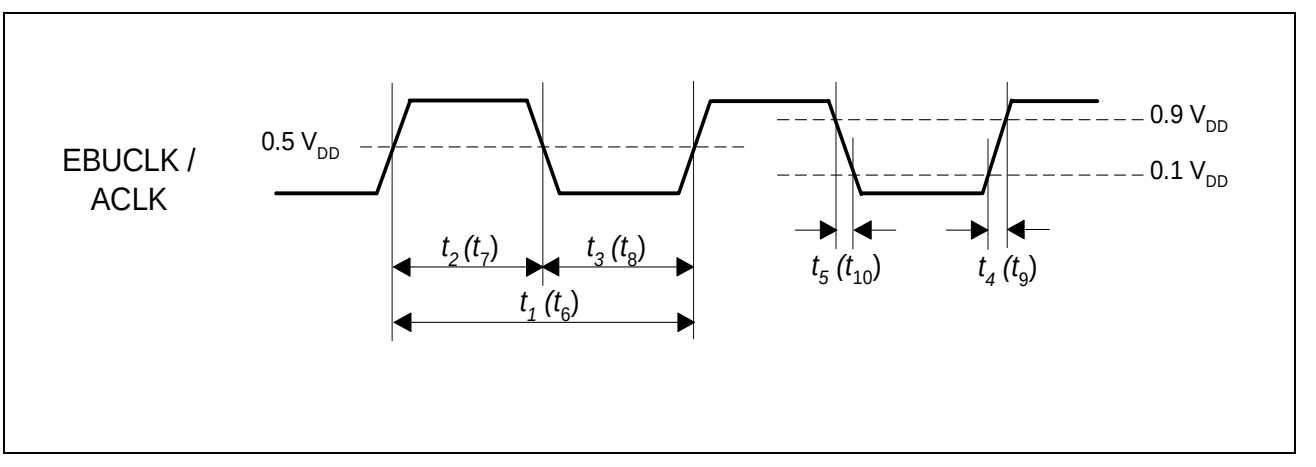


Figure 24 EBU_LMB Clock Output Timing

Timing for SDRAM Access Signals
(Operating Conditions apply; C_L = 30 pF)

Parameter	Symbol		Limits		Unit
			min	max	
CKE high from EBUCLK ↑	t_1	CC	–	7.0	ns
CKE low from EBUCLK ↑	t_2	CC	–	7.0	ns
A(23:0) output valid from EBUCLK ↑	t_3	CC	–	8.0	ns
A(23:0) output hold from EBUCLK ↑	t_4	CC	2.0	–	ns
$\overline{\text{CS}}$(6:0) low from EBUCLK ↑	t_5	CC	–	7.0	ns
$\overline{\text{CS}}$(6:0) high from EBUCLK ↑	t_6	CC	–	7.0	ns
$\overline{\text{RAS}}$ low from EBUCLK ↑	t_7	CC	–	7.0	ns
$\overline{\text{RAS}}$ high from EBUCLK ↑	t_8	CC	–	8.0	ns
$\overline{\text{CAS}}$ low from EBUCLK ↑	t_9	CC	–	7.0	ns
$\overline{\text{CAS}}$ high from EBUCLK ↑	t_{10}	CC	–	8.0	ns
RD/$\overline{\text{WR}}$ low from EBUCLK ↑	t_{11}	CC	–	7.5	ns
RD/$\overline{\text{WR}}$ high from EBUCLK ↑	t_{12}	CC	–	7.5	ns
$\overline{\text{BC}}$(3:0) low from EBUCLK ↑	t_{13}	CC	–	7.0	ns
$\overline{\text{BC}}$(3:0) high from EBUCLK ↑	t_{14}	CC	–	7.0	ns
AD(31:0) output valid from EBUCLK ↑	t_{15}	CC	–	7.7	ns
AD(31:0) output hold from EBUCLK ↑	t_{16}	CC	2.0	–	ns
AD(31:0) input setup to EBUCLK ↑	t_{17}	SR	-0.8	–	ns
AD(31:0) input hold from EBUCLK ↑	t_{18}	SR	3.8	–	ns

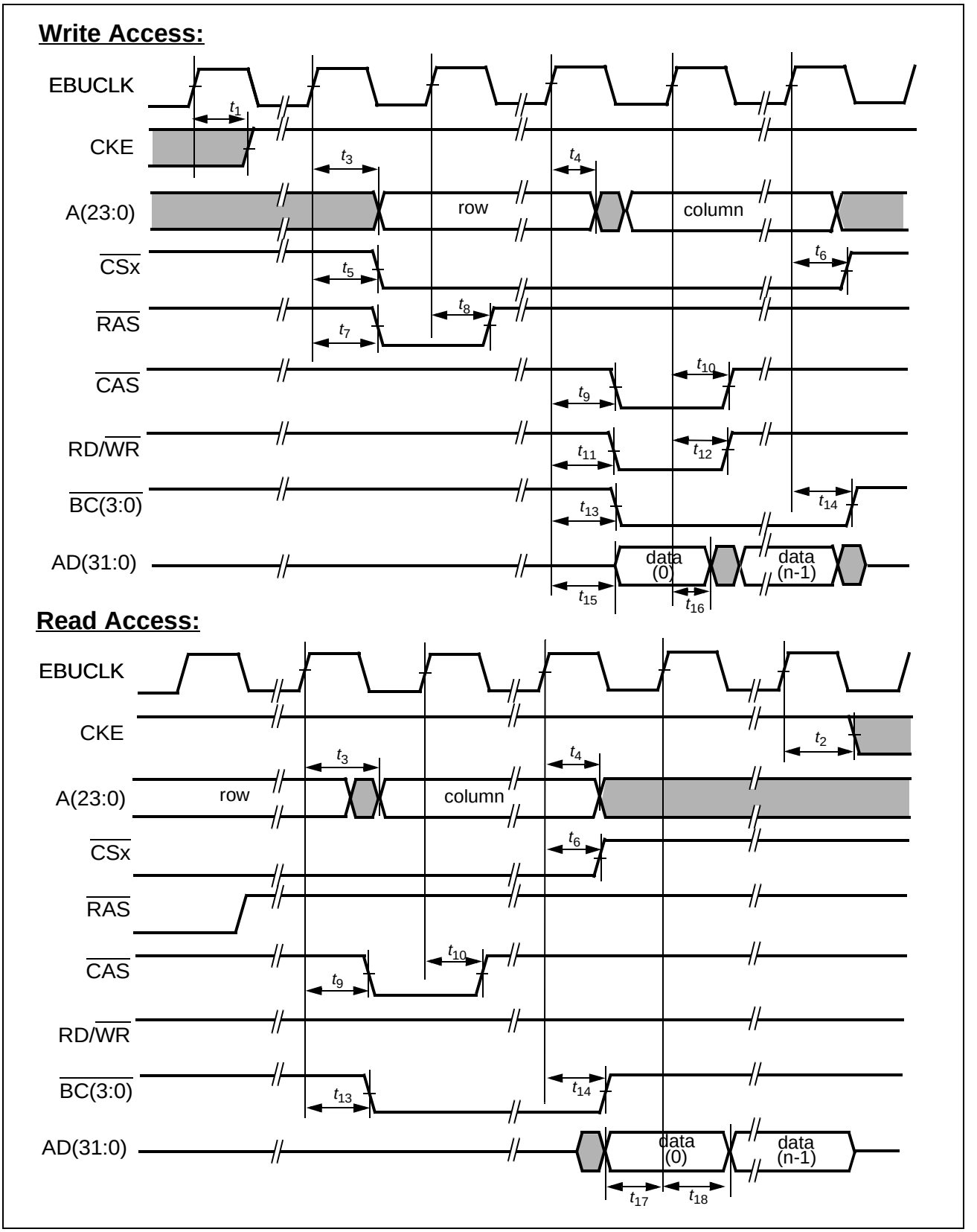


Figure 25 SDRAM Access Timing

Timing for Burst Flash Access Signals

Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
A(23:0) output valid from ACLK ↓	t_1	CC	–	12.0	ns
A(23:0) output hold from ACLK ↓	t_2	CC	2.0	–	ns
$\overline{\text{CS}}$(6:0) low from ACLK ↓	t_3	CC	–	12.0	ns
$\overline{\text{CS}}$(6:0) high from ACLK ↓	t_4	CC	–	12.0	ns
$\overline{\text{ADV}}$ low from ACLK ↓	t_5	CC	–	19.0	ns
$\overline{\text{ADV}}$ high from ACLK ↓	t_6	CC	–	19.0	ns
$\overline{\text{BAA}}$ low from ACLK ↓	t_7	CC	–	20.0	ns
$\overline{\text{BAA}}$ high from ACLK ↓	t_8	CC	–	20.0	ns
$\overline{\text{RD}}$ low from ACLK ↓	t_9	CC	–	12.0	ns
$\overline{\text{RD}}$ high from ACLK ↓	t_{10}	CC	–	12.0	ns
AD(31:0) input setup to ACLK ↓	t_{11}	SR	8.0	–	ns
AD(31:0) input hold from ACLK ↓	t_{12}	SR	1.0	–	ns

Note:$\overline{\text{WAIT}}$ signal is not characterized here because the TC11IB does not cover such cases.

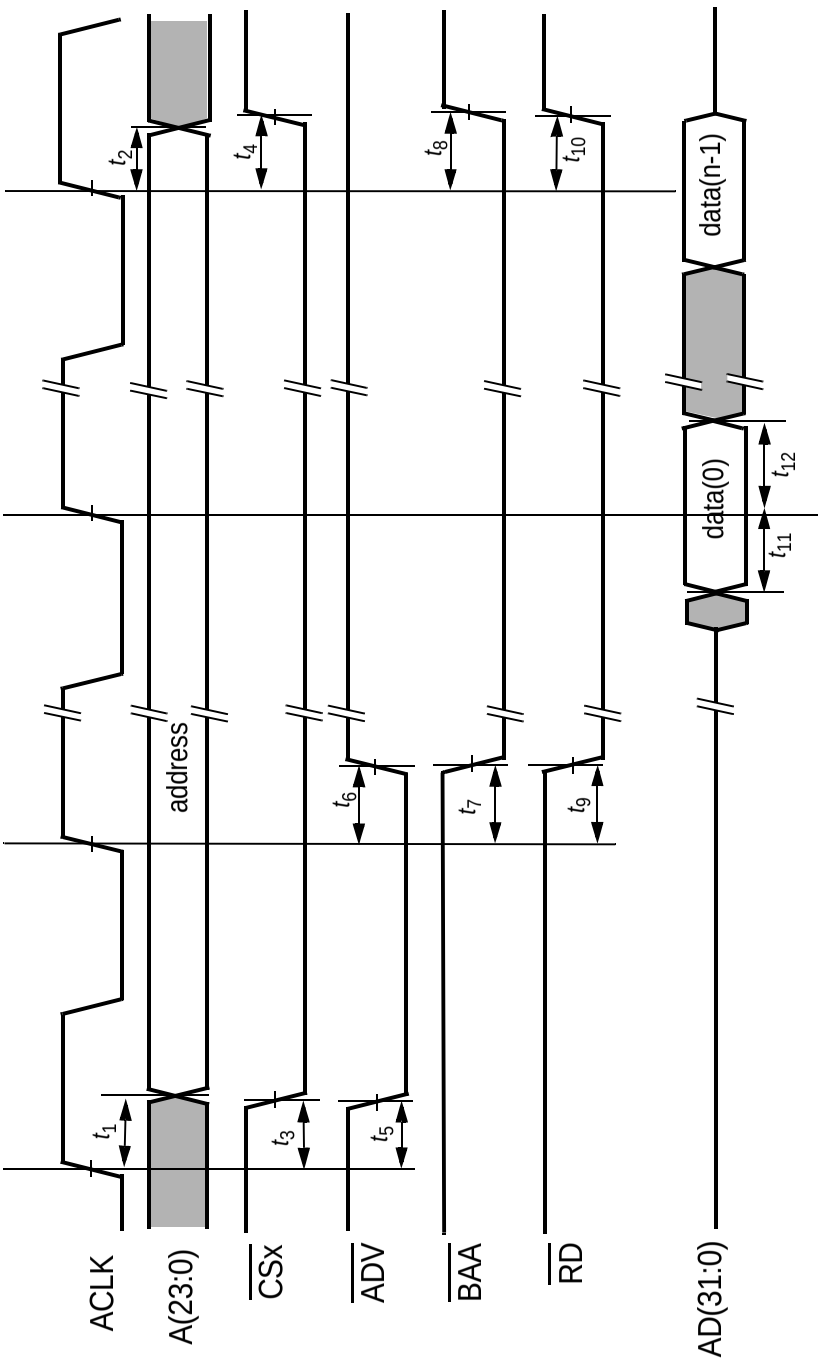


Figure 26 Burst Flash Access Timing

Timing for Demultiplexed Access Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
ALE low from EBUCLK ↓	t_1	CC	–	8.0	ns
ALE high from EBUCLK ↓	t_2	CC	–	8.0	ns
A(23:0) output valid from EBUCLK ↓	t_3	CC	–	8.0	ns
A(23:0) output hold from EBUCLK ↓	t_4	CC	2.0	–	ns
$\overline{\text{CS}}$(6:0) low from EBUCLK ↓	t_5	CC	–	8.0	ns
$\overline{\text{CS}}$(6:0) high from EBUCLK ↓	t_6	CC	–	8.0	ns
MR/$\overline{\text{W}}$ low from EBUCLK ↓	t_7	CC	–	8.0	ns
MR/$\overline{\text{W}}$ high from EBUCLK ↓	t_8	CC	–	8.0	ns
$\overline{\text{RMW}}$ low from EBUCLK ↓	t_9	CC	–	16.5	ns
$\overline{\text{RMW}}$ high from EBUCLK ↓	t_{10}	CC	–	16.5	ns
$\overline{\text{RD}}$ low from EBUCLK ↓	t_{11}	CC	–	8.0	ns
$\overline{\text{RD}}$ high from EBUCLK ↓	t_{12}	CC	–	8.0	ns
RD/$\overline{\text{WR}}$ low from EBUCLK ↓	t_{13}	CC	–	8.0	ns
RD/$\overline{\text{WR}}$ high from EBUCLK ↓	t_{14}	CC	–	8.0	ns
$\overline{\text{CMDELAY}}$ input setup to EBUCLK ↓	t_{15}	SR	7.0	–	ns
$\overline{\text{CMDELAY}}$ hold from EBUCLK ↓	t_{16}	SR	5.5	–	ns
$\overline{\text{WAIT}}$ input setup to EBUCLK ↓	t_{17}	SR	8.0	–	ns
$\overline{\text{WAIT}}$ hold from EBUCLK ↓	t_{18}	SR	5.5	–	ns
$\overline{\text{BC}}$(3:0) low from EBUCLK ↓	t_{19}	CC	–	8.0	ns
$\overline{\text{BC}}$(3:0) high from EBUCLK ↓	t_{20}	CC	–	8.0	ns
AD(31:0) output valid from EBUCLK ↓	t_{21}	CC	–	8.0	ns
AD(31:0) output hold from EBUCLK ↓	t_{22}	CC	2.0	–	ns
AD(31:0) input setup to EBUCLK ↓	t_{23}	SR	7.0	–	ns
AD(31:0) input hold from EBUCLK ↓	t_{24}	SR	3.5	–	ns

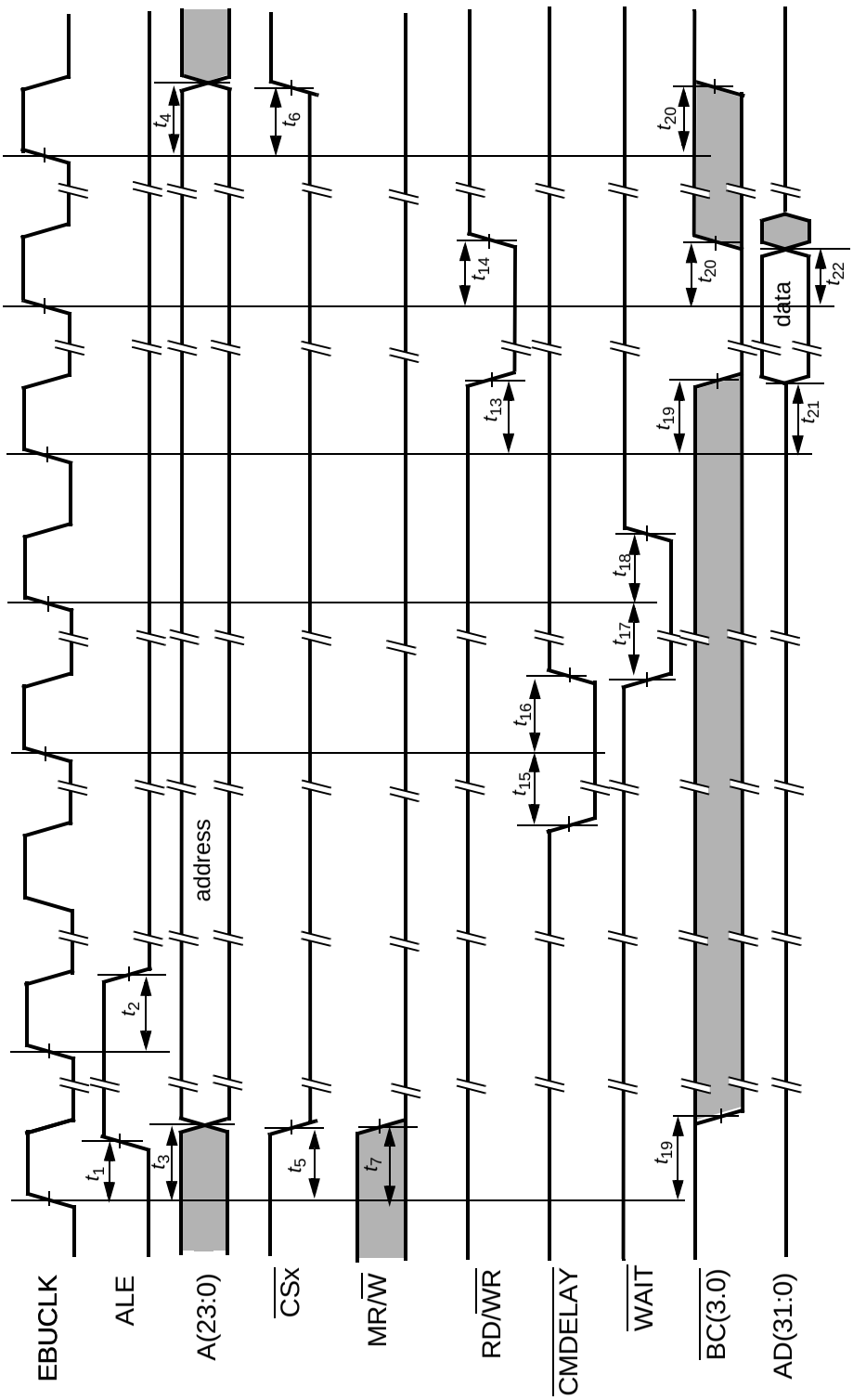


Figure 27 Write Access in Demultiplexed Access

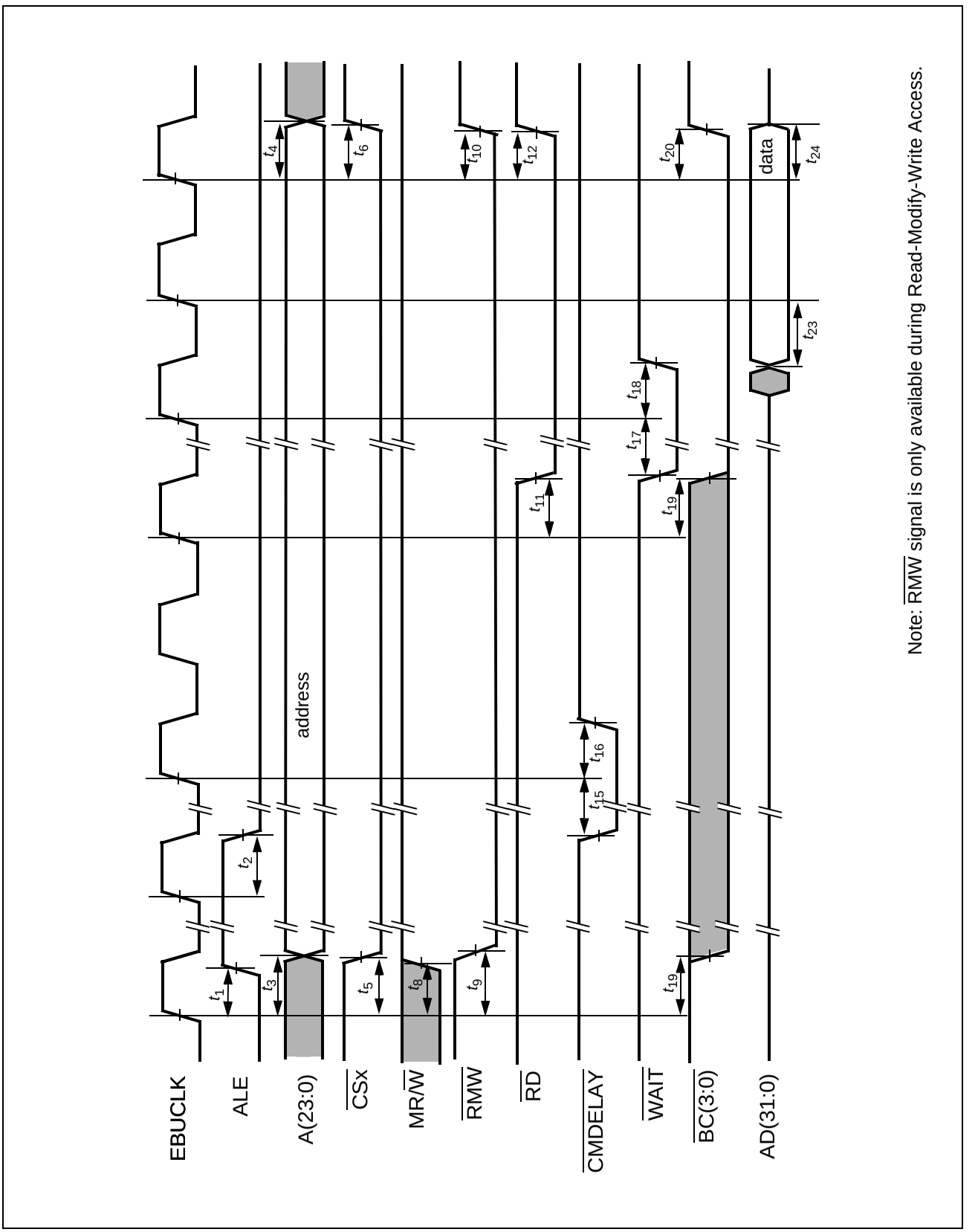


Figure 28 Read Access in Demultiplexed Access

Timing for Multiplexed Access Signals
(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
ALE high from EBUCLK ↑	t_1	CC	–	8.0	ns
ALE low from EBUCLK ↑	t_2	CC	–	8.0	ns
AD(31:0) output valid from EBUCLK ↑	t_3	CC	–	8.0	ns
AD(31:0) output hold from EBUCLK ↑	t_4	CC	2.0	–	ns
AD(31:0) input setup to EBUCLK ↑	t_5	SR	7.0	–	ns
AD(31:0) input hold from EBUCLK ↑	t_6	SR	3.5	–	ns
$\overline{\text{CS}}$(6:0) low from EBUCLK ↑	t_7	CC	–	8.0	ns
$\overline{\text{CS}}$(6:0) high from EBUCLK ↑	t_8	CC	–	8.0	ns
MR/$\overline{\text{W}}$ low from EBUCLK ↑	t_9	CC	–	8.0	ns
MR/$\overline{\text{W}}$ high from EBUCLK ↑	t_{10}	CC	–	8.0	ns
$\overline{\text{RMW}}$ low from EBUCLK ↑	t_{11}	CC	–	16.5	ns
$\overline{\text{RMW}}$ high from EBUCLK ↑	t_{12}	CC	–	16.5	ns
RD/$\overline{\text{WR}}$ low from EBUCLK ↑	t_{13}	CC	–	8.0	ns
RD/$\overline{\text{WR}}$ high from EBUCLK ↑	t_{14}	CC	–	8.0	ns
$\overline{\text{RD}}$ low from EBUCLK ↑	t_{15}	CC	–	8.0	ns
$\overline{\text{RD}}$ high from EBUCLK ↑	t_{16}	CC	–	8.0	ns
$\overline{\text{CMDELAY}}$ input setup to EBUCLK ↑	t_{17}	SR	7.0	–	ns
$\overline{\text{CMDELAY}}$ hold from EBUCLK ↑	t_{18}	SR	5.5	–	ns
$\overline{\text{WAIT}}$ input setup to EBUCLK ↑	t_{19}	SR	6.0	–	ns
$\overline{\text{WAIT}}$ hold from EBUCLK ↑	t_{20}	SR	5.5	–	ns
$\overline{\text{BC}}$(3:0) low from EBUCLK ↑	t_{21}	CC	–	8.0	ns
$\overline{\text{BC}}$(3:0) high from EBUCLK ↑	t_{22}	CC	–	8.0	ns

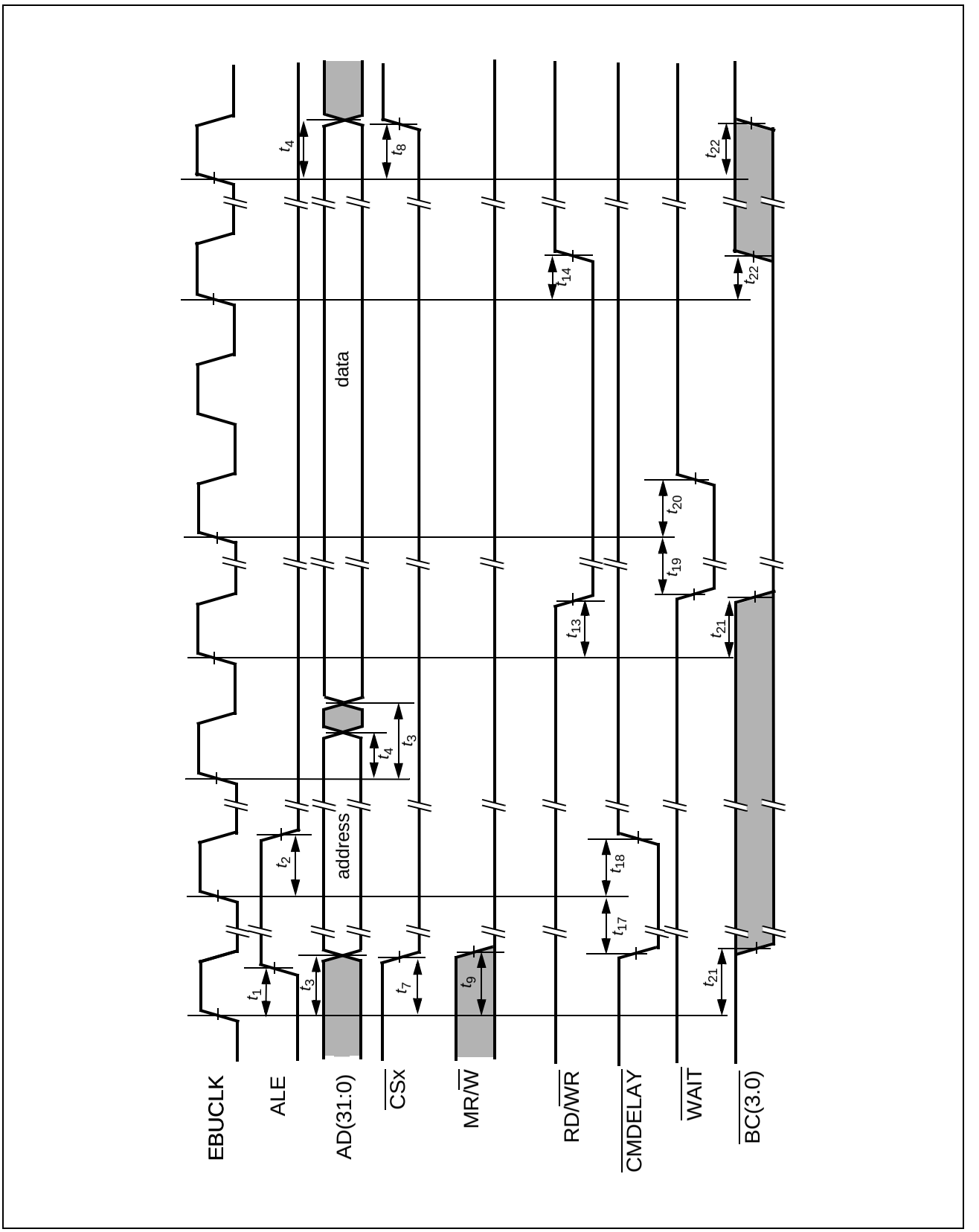


Figure 29 Write Access in Multiplexed Access

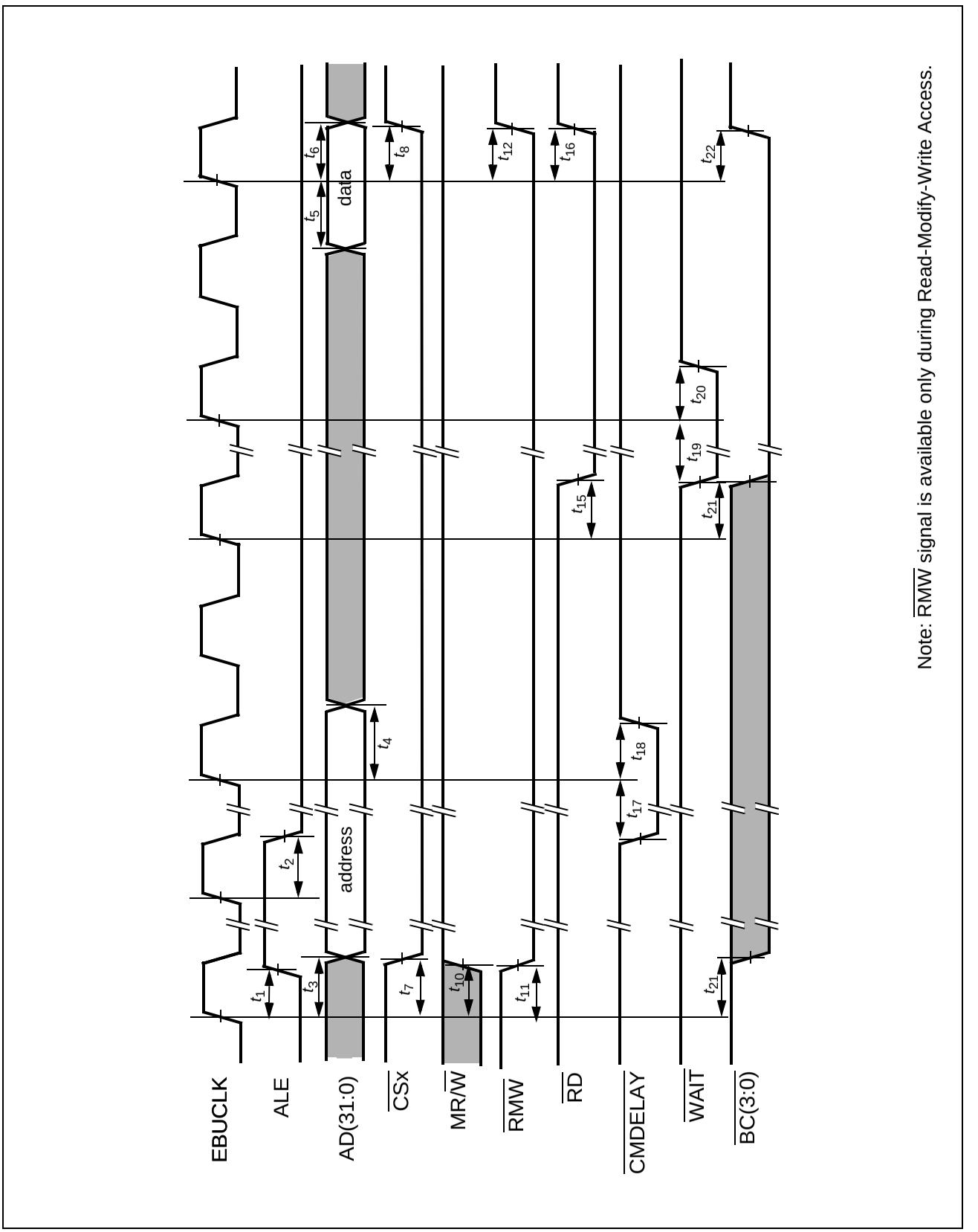


Figure 30 Read Access in Multiplexed Access

Timing for External Bus Arbitration Signals
(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
$\overline{\text{HOLD}}$ input setup to EBUCLK ↑	t_1	SR	6.0	–	ns
$\overline{\text{HOLD}}$ input hold from EBUCLK ↑	t_2	SR	5.5	–	ns
$\overline{\text{HLDA}}$ low from EBUCLK ↑	t_3	CC	–	11.0	ns
$\overline{\text{HLDA}}$ high from EBUCLK ↑	t_4	CC	–	11.0	ns
$\overline{\text{HLDA}}$ input setup to EBUCLK ↑	t_5	SR	6.4	–	ns
$\overline{\text{HLDA}}$ input hold from EBUCLK ↑	t_6	SR	5.5	–	ns
$\overline{\text{BREQ}}$ low from EBUCLK ↑	t_7	CC	–	9.5	ns
$\overline{\text{BREQ}}$ high from EBUCLK ↑	t_8	CC	–	9.5	ns
$\overline{\text{CS}}$(6:0) drive from EBUCLK ↑	t_9	CC	–	8.0	ns
$\overline{\text{CS}}$(6:0) high-impedance from EBUCLK ↑	t_{10}	CC	–	8.0	ns
Other signals high-impedance from EBUCLK ↑	t_{11}	CC	–	8.0	ns
Other signals drive from EBUCLK ↑	t_{12}	CC	–	8.0	ns

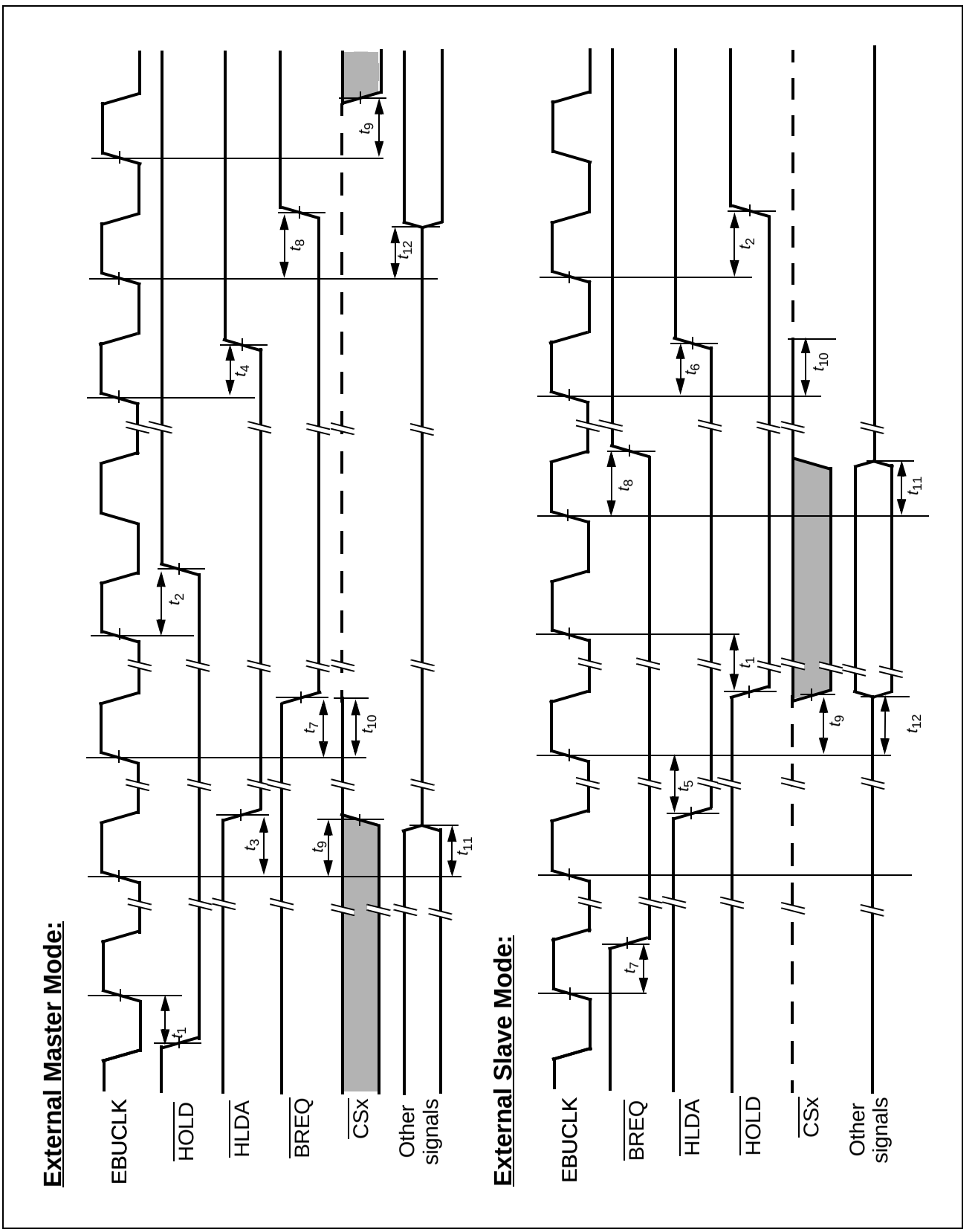


Figure 31 External Bus Arbitration Timing

Port Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limits		Unit
		min	max	
Port data valid from CPUCLK ↓ [1]	t_1 CC	–	14.0	ns

[1] Port data is output with respect to the slow FPI clock at 48MHz. The CPUCLK is used as a reference here since the slow FPI clock is not available as an external pin. Port lines maintain its state for at least 2 CPU clocks.

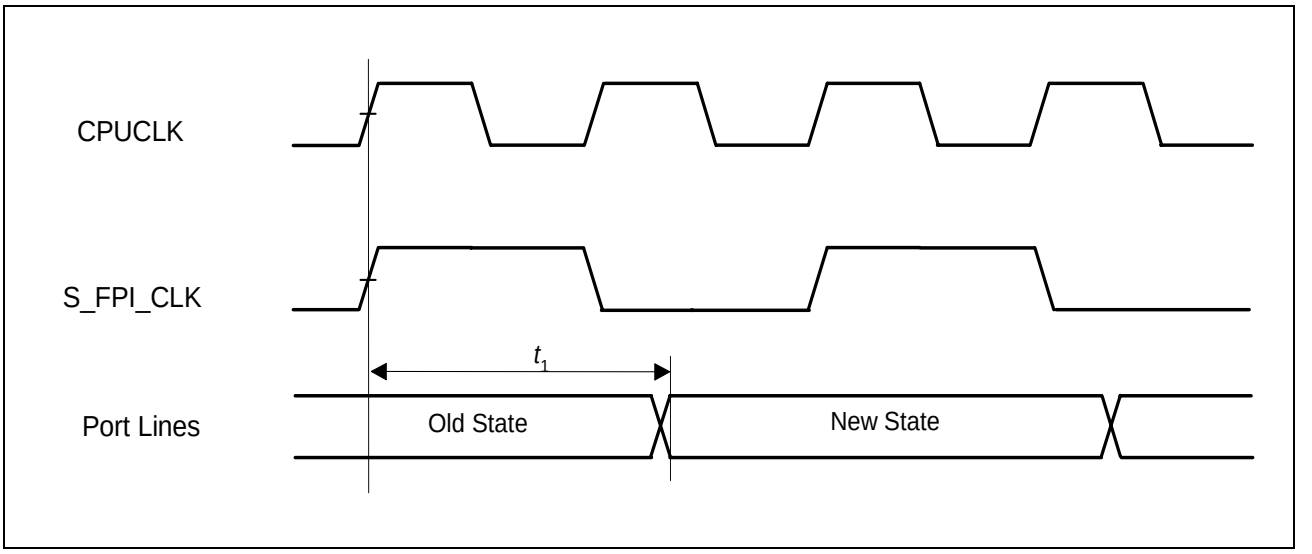


Figure 32 Port Timing

Timing for Ethernet Signals
(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
ETXCLK period (10 Mbps Ethernet)	t_1	SR	400.0	–	ns
ETXCLK high time (10 Mbps Ethernet)	t_2	SR	140.0	260.0	ns
ETXCLK low time (10 Mbps Ethernet)	t_3	SR	140.0	260.0	ns
ETXCLK period (100 Mbps Ethernet)	t_1	SR	40.0	–	ns
ETXCLK high time (100 Mbps Ethernet)	t_2	SR	14.0	26.0	ns
ETXCLK low time (100 Mbps Ethernet)	t_3	SR	14.0	26.0	ns
ERXCLK period (10 Mbps Ethernet)	t_1	SR	400.0	–	ns
ERXCLK high time (10 Mbps Ethernet)	t_2	SR	140.0	260.0	ns
ERXCLK low time (10 Mbps Ethernet)	t_3	SR	140.0	260.0	ns
ERXCLK period (100 Mbps Ethernet)	t_1	SR	40.0	–	ns
ERXCLK high time (100 Mbps Ethernet)	t_2	SR	14.0	26.0	ns
ERXCLK low time (100 Mbps Ethernet)	t_3	SR	14.0	26.0	ns
ERXD(3:0) input setup to ERXCLK	t_4	SR	10.0	–	ns
ERXD(3:0) input hold from ERXCLK	t_5	SR	–	10.0	ns
ERXDV input setup to ERXCLK	t_4	SR	10.0	–	ns
ERXDV input hold from ERXCLK	t_5	SR	–	10.0	ns
ERXER input setup to ERXCLK	t_4	SR	10.0	–	ns
ERXER input hold from ERXCLK	t_5	SR	–	10.0	ns
ETXD(3:0) output valid from ETXCLK	t_6	CC	–	25.0	ns
ETXEN output valid from ETXCLK	t_6	CC	–	25.0	ns
ETXER output valid from ETXCLK	t_6	CC	–	25.0	ns
EMDC clock period	t_7	CC	150.0	–	ns
EMDIO input setup to EMDC (sourced by STA)	t_8	SR	10.0	–	ns
EMDIO input hold from EMDC (sourced by STA)	t_9	SR	–	10.0	ns
EMDIO output valid from EMDC (sourced by PHY)	t_{10}	CC	–	15.0	ns

Note: Any other parameters which are not stated here, please refer to ANSI/IEEE Std 802.3, Section 22.3.

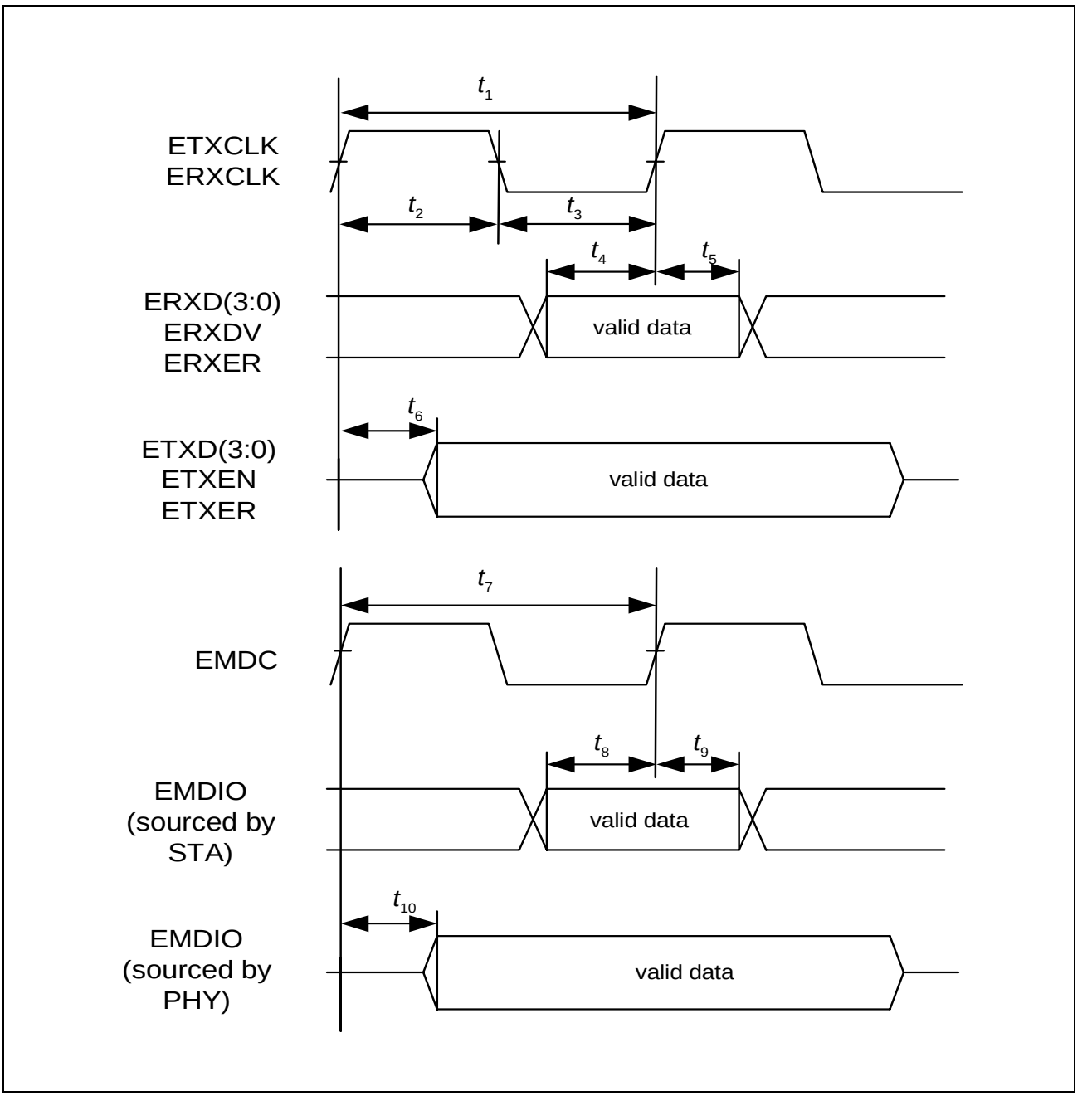


Figure 33 Ethernet Timing

Timing for MultiMediaCard Interface Signals
(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
MMCI.CLK period	t_1	CC	62.5	–	ns
MMCI.CLK high time	t_2	CC	28	–	ns
MMCI.CLK low time	t_3	CC	28	–	ns
MMCI.CMD_RW output valid from MMCI.CLK ↓	t_4	CC	–	4.0	ns
MMCI.DAT_RW output valid from MMCI.CLK ↓	t_4	CC	–	3.0	ns
MMCI.ROD output valid from MMCI.CLK ↓	t_4	CC	–	4.0	ns
MMCI.VDDEN output valid from MMCI.CLK ↓	t_4	CC	–	2.0	ns
MMCI.CMD output valid from MMCI.CLK ↓	t_4	CC	–	33	ns
MMCI.DAT output valid from MMCI.CLK ↓	t_4	CC	–	33	ns
MMCI.CMD input setup to MMCI.CLK ↓	t_5	SR	12	–	ns
MMCI.DAT input setup to MMCI.CLK ↓	t_5	SR	10	–	ns
MMCI.CMD input hold from MMCI.CLK ↓	t_6	SR	–	2.0	ns
MMCI.DAT input hold from MMCI.CLK ↓	t_6	SR	–	2.0	ns

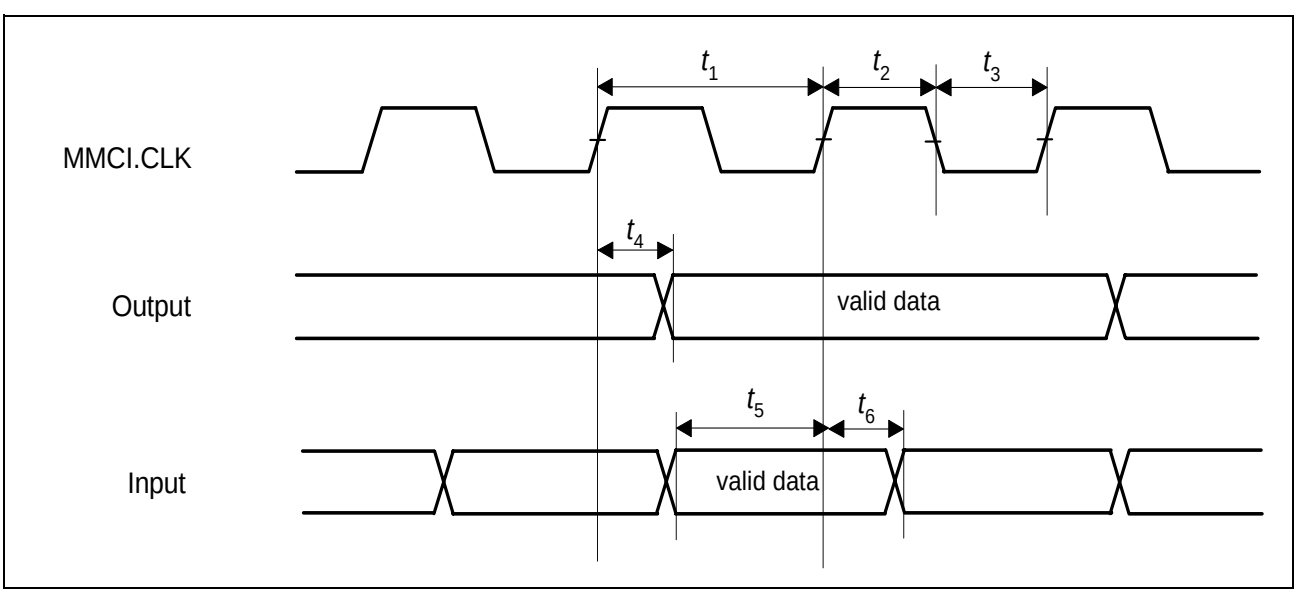


Figure 34 MultiMediaCard Interface Timing

SSC Master Mode Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK clock frequency	$1 / t_{SCLK}$	CC	-	24	MHz
SCLK clock high time	t_1	CC	18	-	ns
SCLK clock low time	t_2	CC	18	-	ns
SCLK clock rise time	t_3	CC	-	11	ns
SCLK clock fall time	t_4	CC	-	11	ns
MTSR low/high from SCLK edge	t_5	CC	-	2.0	ns
MRST setup to SCLK edge	t_6	SR	13	-	ns
MRST hold from SCLK edge	t_7	SR	7.5	-	ns

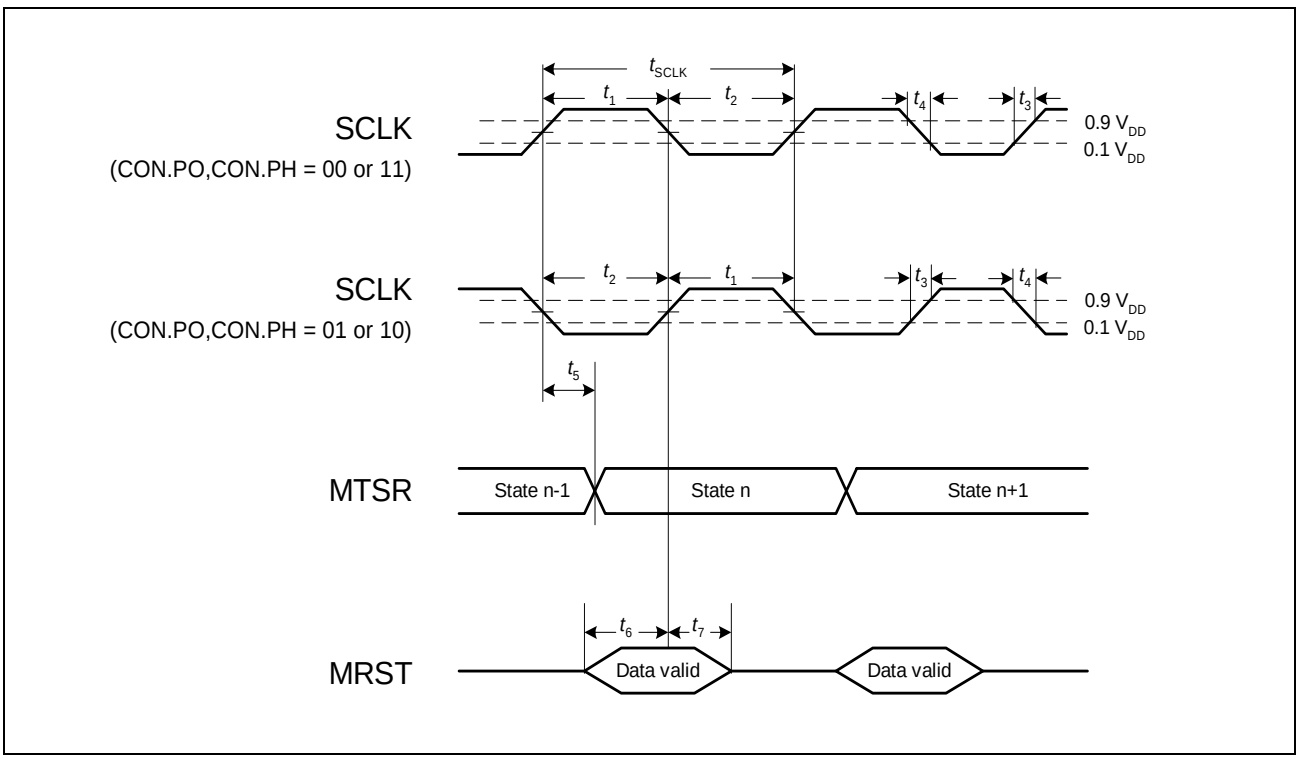


Figure 35 SSC Master Mode Timing

Timing for JTAG Signals
(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TCK clock period	t_{TCK}	CC	50	–	ns
TCK high time	t_1	CC	10	–	ns
TCK low time	t_2	CC	29	–	ns
TCK clock rise time	t_3	CC	–	0.4	ns
TCK clock fall time	t_4	CC	–	0.4	ns

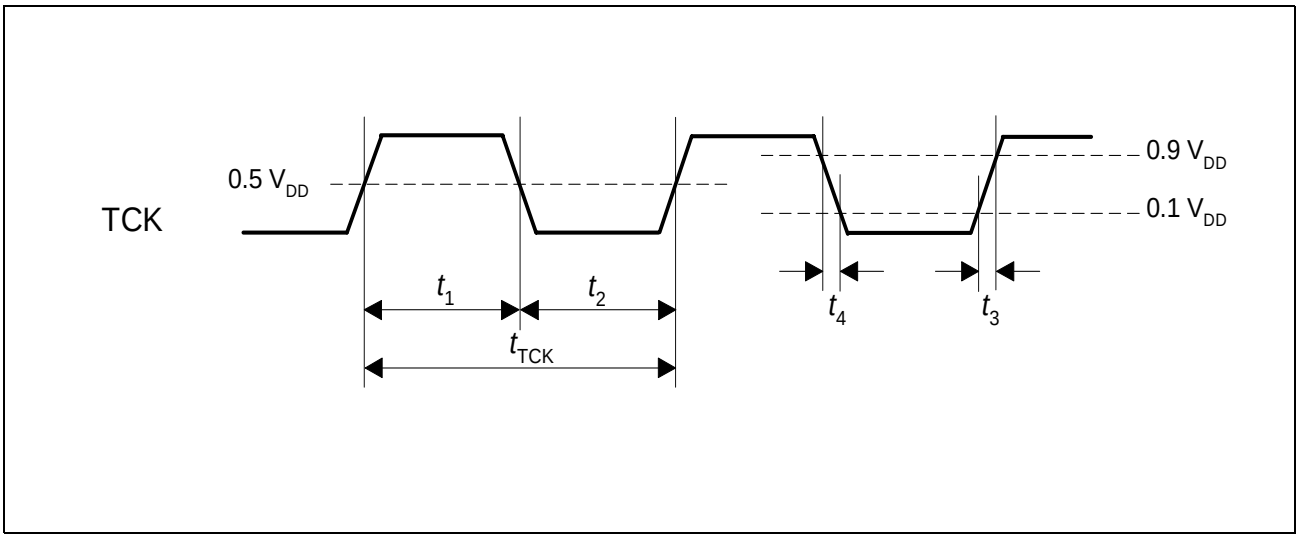


Figure 36 TCK Clock Timing

Parameter	Symbol		Limits		Unit
			min	max	
TMS setup to TCK ↑	t_1	CC	7.85	–	ns
TMS hold to TCK ↑	t_2	CC	–	1.0	ns
TDI setup to TCK ↑	t_1	CC	10.9	–	ns
TDI hold to TCK ↑	t_2	CC	–	1.0	ns
TDO valid output from TCK ↓	t_3	CC	–	29.0	ns
TDO high impedance to valid output from TCK ↓	t_4	CC	–	23.0	ns
TDO valid output to high impedance from TCK ↓	t_5	CC	–	26.0	ns

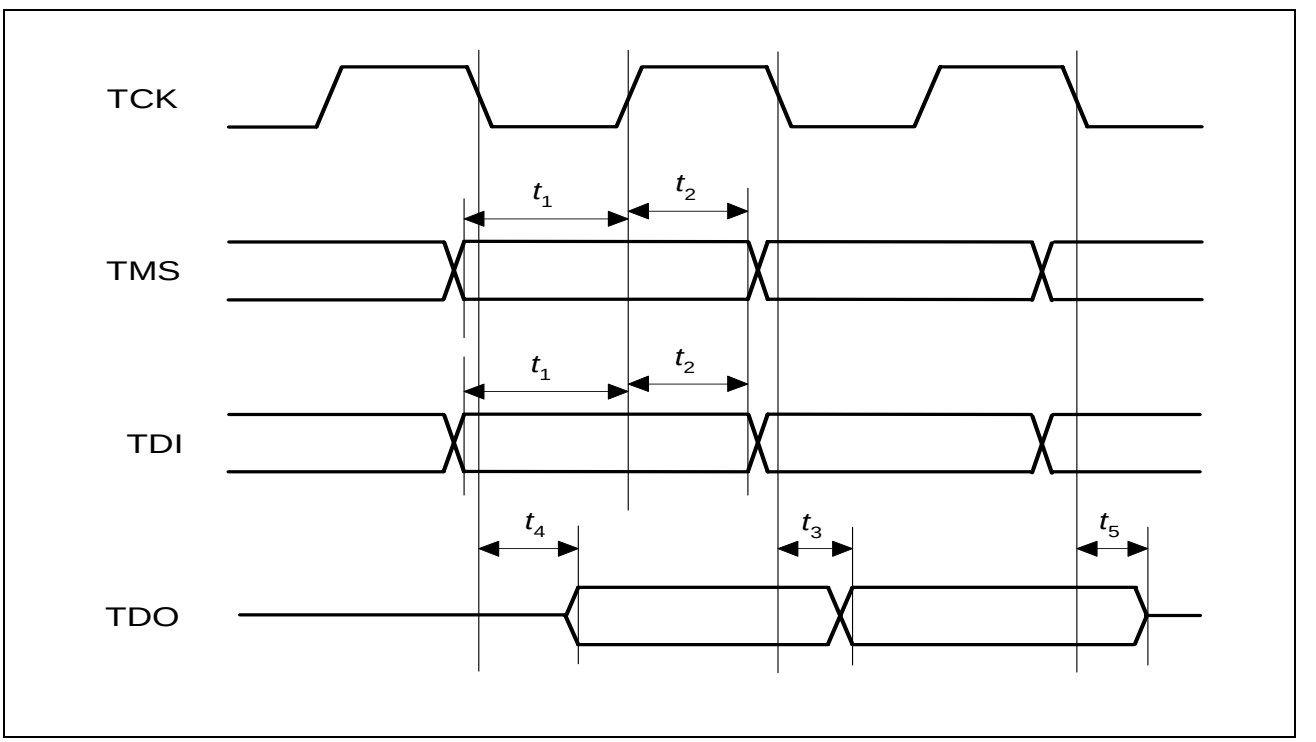


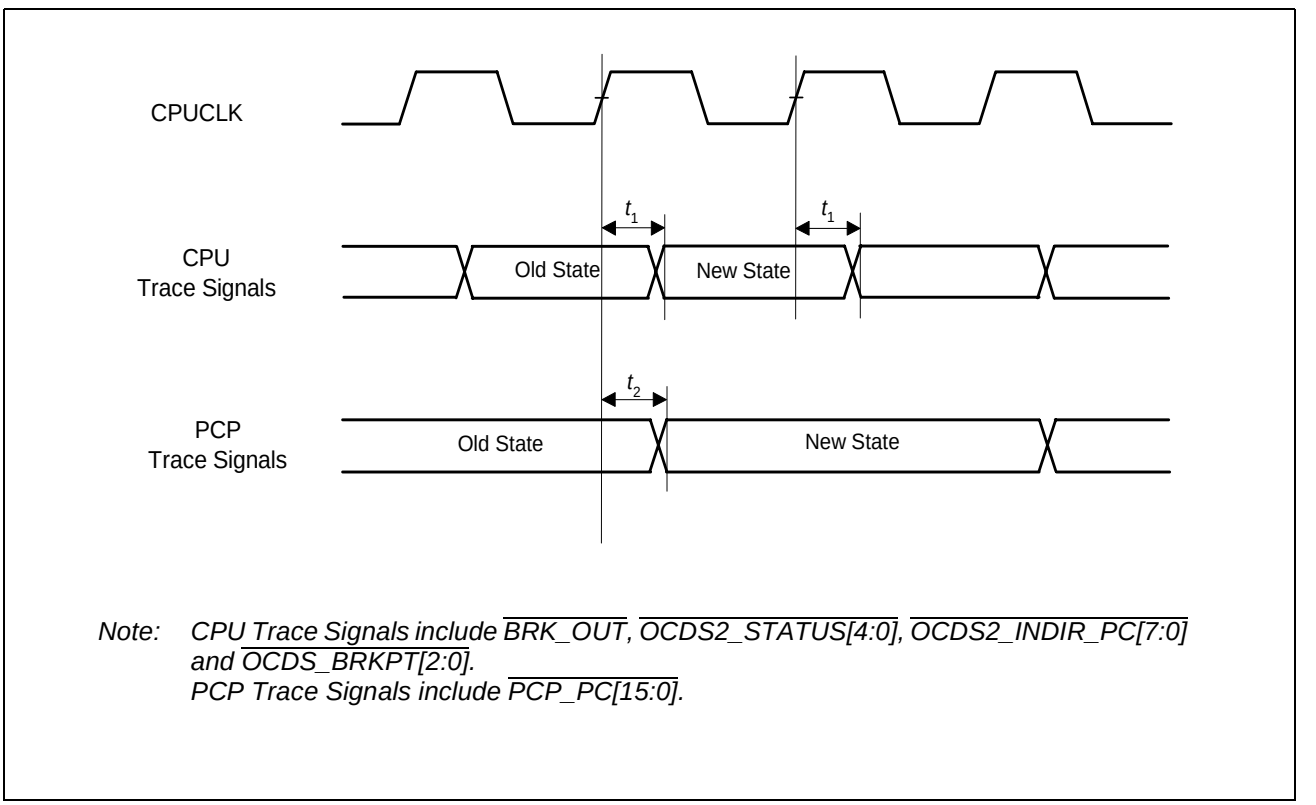
Figure 37 JTAG Timing

Timing for OCDS Trace and Breakpoint Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
$\overline{\text{BRK\_OUT}}$ valid from CPUCLK ↓	t_1	CC	–	17.0	ns
$\overline{\text{OCDS2\_STATUS[4:0]}}$ valid from CPUCLK ↓	t_1	CC	–	7.0	ns
$\overline{\text{OCDS2\_INDIR\_PC[7:0]}}$ valid from CPUCLK ↓	t_1	CC	–	7.0	ns
$\overline{\text{OCDS2\_BRKPT[2:0]}}$ valid from CPUCLK ↓	t_1	CC	–	7.0	ns
$\overline{\text{PCP\_PC[15:0]}}$ valid from CPUCLK ↓ [1]	t_2	CC	–	7.0	ns

[1] PCP Trace signals are output with respect to the slow FPI clock at 48MHz. The CPUCLK is used as a reference here since the slow FPI clock is not available as an external pin. PCP Trace signals maintain its state for at least 2 CPU clocks.



Note: CPU Trace Signals include $\overline{\text{BRK\_OUT}}$, $\overline{\text{OCDS2\_STATUS[4:0]}}$, $\overline{\text{OCDS2\_INDIR\_PC[7:0]}}$ and $\overline{\text{OCDS\_BRKPT[2:0]}}$.
PCP Trace Signals include $\overline{\text{PCP\_PC[15:0]}}$.

Figure 38 OCDS Trace Signals Timing

PCI 33MHz, 3.3V Signaling

(Operating Conditions apply; C_L = 10 pF)

Parameter	Symbol	Min.	Max.	Units	Test condition
Switching Current High	I_{OH}(AC)	$-12V_{DDP}$		mA	$0 < V_{OUT} \leq 0.3V_{DDP}$ [1]
		$-17.1(V_{DDP} - V_{OUT})$		mA	$0.3V_{DDP} < V_{OUT} < 0.9V_{DDP}$ [1]
			Eqt'n 1 [2]		$0.7V_{DDP} < V_{OUT} < V_{DDP}$ [1] [3]
(Test Point)			$-32V_{DDP}$	mA	$V_{OUT} = 0.7V_{DDP}$ [3]
Switching Current Low	I_{OL}(AC)	$16V_{DDP}$		mA	$V_{DDP} > V_{OUT} \geq 0.6V_{DDP}$ [1]
		$26.7V_{OUT}$		mA	$0.6V_{DDP} > V_{OUT} > 0.1V_{DDP}$ [1]
			Eqt'n 2 [4]		$0.18V_{DDP} > V_{OUT} > 0$ [1] [3]
(Test Point)			$38V_{DDP}$	mA	$V_{OUT} = 0.18V_{DDP}$ [3]
Low Clamp Current	I_{CL}	$-25 + (V_{IN} + 1)/(0.015)$		mA	$-3 < V_{IN} \leq -1$
High Clamp Current	I_{CH}	$25 + (V_{IN} - V_{DDP} - 1)/(0.015)$		mA	$V_{DDP}+4 > V_{IN} \geq V_{DDP}+1$
Output Rise Slew Rate	$slew_r$	1	4	V / ns	$0.2V_{DDP}$ - $0.6V_{DDP}$ load [5]
Output Fall Slew Rate	$slew_f$	1	4	V / ns	$0.6V_{DDP}$ - $0.2V_{DDP}$ load [5]

[1] Refer to the V/I curves in **Figure 39**. Switching current characteristics for **REQ** and **GNT** are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to **CLK** and **RST** which are system outputs. "Switching Current High" specifications are not relevant to **SERR, PME, INTA, INTB** which are open drain outputs.

[2] **Equation 1**: $I_{OH} = (98/V_{DDP}) \cdot (V_{OUT} - V_{DDP}) \cdot (V_{OUT} + 0.4\ V_{DDP})$, where $0.7\ V_{DDP} < V_{OUT} < V_{DDP}$

[3] Maximum current requirements must be met as drivers pull beyond the first step voltage. Equations defining these maximums (1 and 2) are provided with the respective diagrams in **Figure 40**. The equation-defined maximums should be met by design. In order to facilitate testing, a maximum current test point is defined for each side of the output driver.

[4] **Equation 2**: $I_{OL} = (256/V_{DDP}) \cdot (V_{OUT}) \cdot (V_{DDP} - V_{OUT})$, where $0 < V_{OUT} < 0.18\ V_{DDP}$

5) This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition edge. The specified load (see **Figure 41**) is optional; i.e., the designer may choose to meet this parameter with an unloaded output as per revision 2.0 of the PCI Local Bus Specification. However, adherence to both max. and min. parameters is required. Rise slew rates does not apply to open drain outputs.

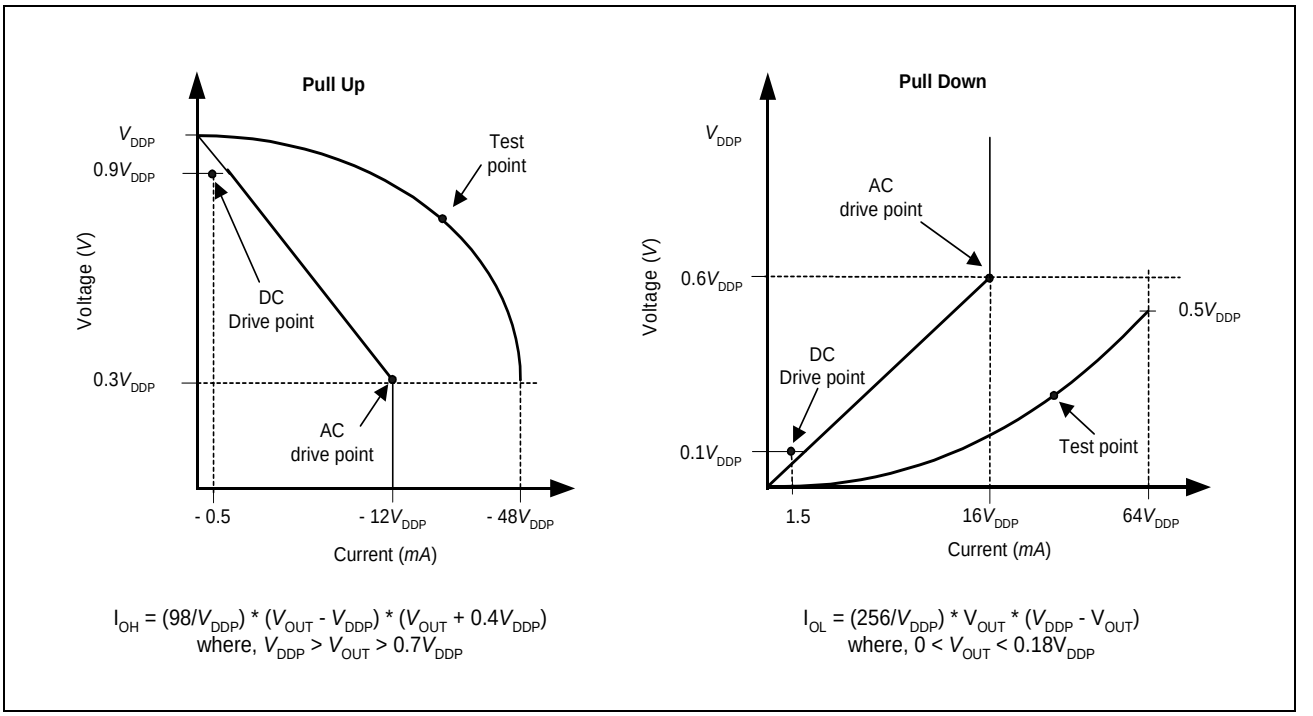


Figure 39 V/I Curves for 3.3V Signaling

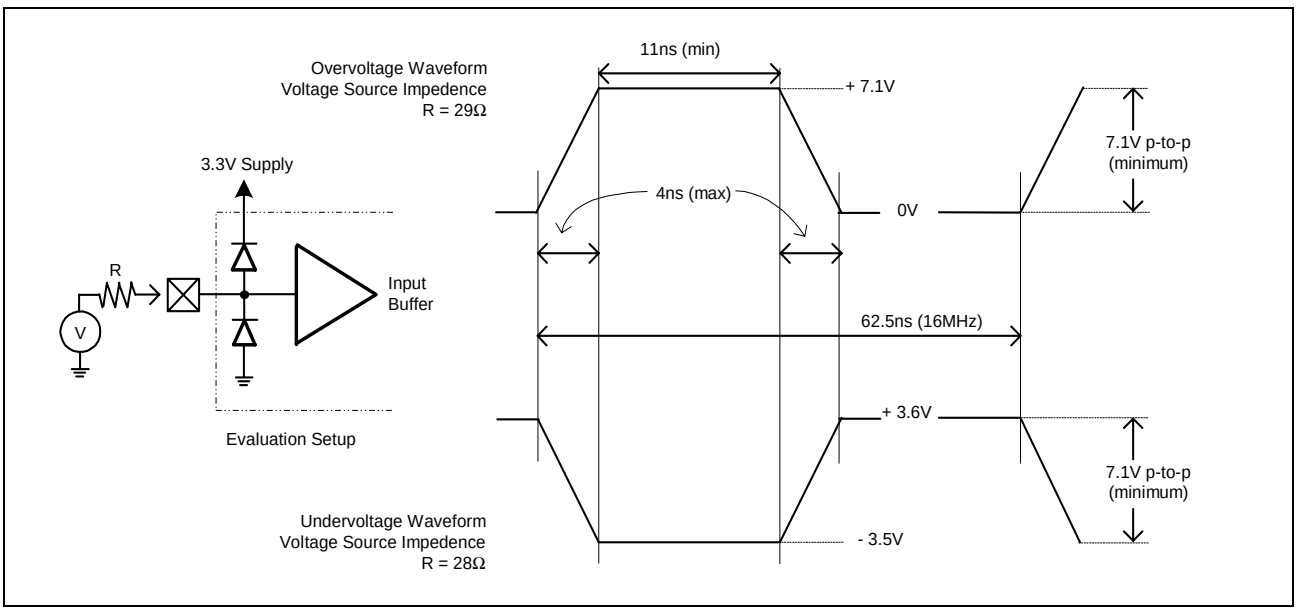


Figure 40 Maximum AC Waveforms for 3.3V Signaling

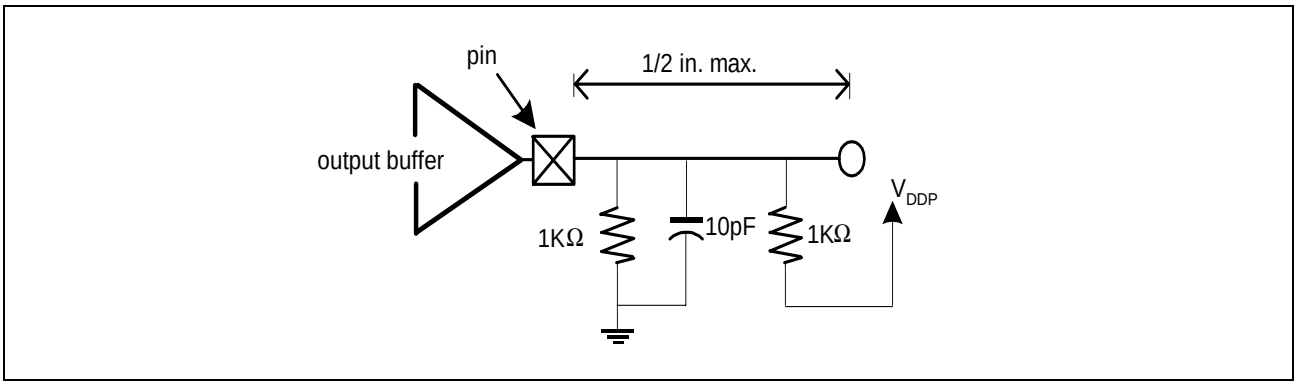


Figure 41 Load Circuit for Slew Rate Measurement

PCI Clock Specification

(Operating Conditions apply; C_L = 10 pF)

Parameter	Symbol	Min.	Max.	Units	Notes
CLK Cycle Time	t_{CYC}	30	-	ns	1)
CLK High Time	t_{HIGH}	11	-	ns	
CLK Low Time	t_{LOW}	11	-	ns	
CLK Slew Rate	-	1	4	V/ns	2)

1) In general, the PCI component must work with any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz may be guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system so long as the clock edges remain “clean” (monotonic) and the minimum cycle, high and low times are not violated. The clock may only be stopped in a low state.

2) Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in **Figure 42**.

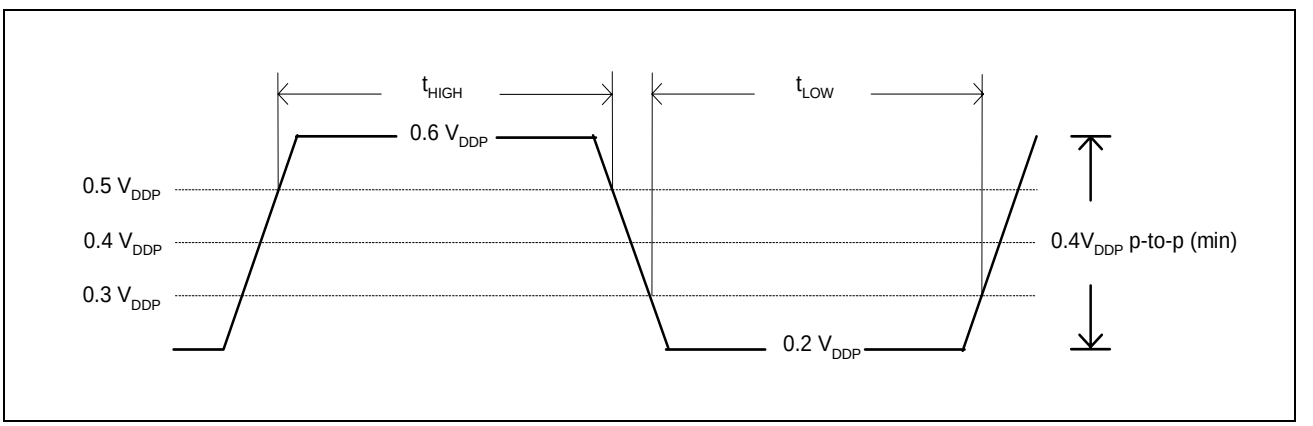


Figure 42 Clock Specification

PCI 3.3V Timing Parameters

(Operating Conditions apply; C_L = 10 pF)

Parameter	Symbol	Min.	Max.	Units	Notes
CLK to signal valid delay - bused signals	t_{VAL}	2	11	ns	1) 2) 3)
CLK to signal valid delay - point to point	$t_{VAL(PTP)}$	2	12	ns	1) 2) 3)
Float to active delay	t_{ON}	2		ns	1) 4)
Active to Float delay	t_{OFF}		28	ns	1) 4)
Input setup time to CLK - bused signals	t_{SU}	7		ns	3) 5) 6)
Input setup time to CLK - point to point	$t_{SU(PTP)}$	10, 12		ns	3) 5)
Input hold time from CLK	t_H	0		ns	5)

1) Refer to **Figure 43**.

2) Minimum times are evaluated with same load used for slew rate measurement (as shown in **Figure 41**). Maximum times are evaluated with the load circuits as illustrated in **Figure 45**.

3) $\overline{REQ}$ and $\overline{GNT}$ are point to point signals and have different output valid delay and input setup times compared to bused signals. $\overline{GNT}$ has a setup of 10 and $\overline{REQ}$ has a setup of 12. All other signals are bused.

4) For purposes of Active/Float timing measurements, the Hi-Z or "OFF" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5) Refer to **Figure 44**.

6) Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

Measurement Conditions

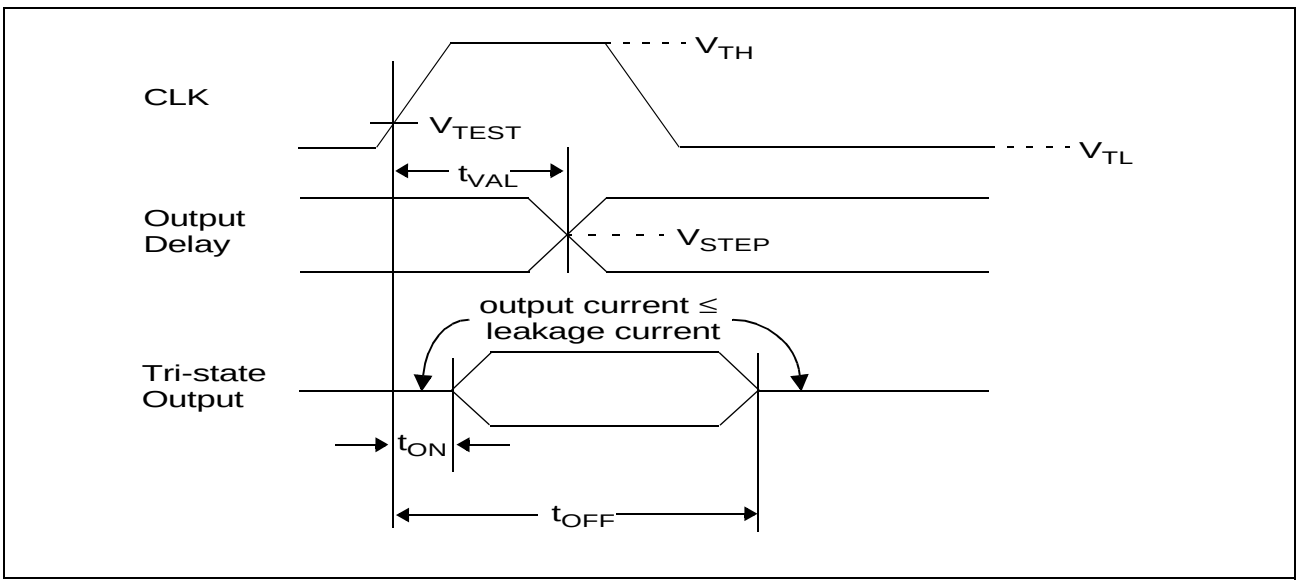


Figure 43 Output timing measurement conditions

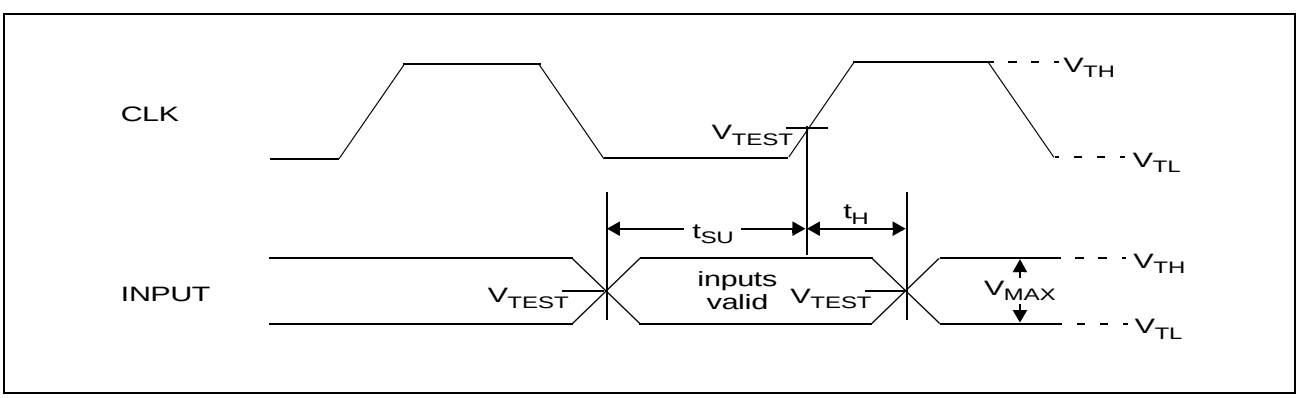


Figure 44 Input timing measurement conditions

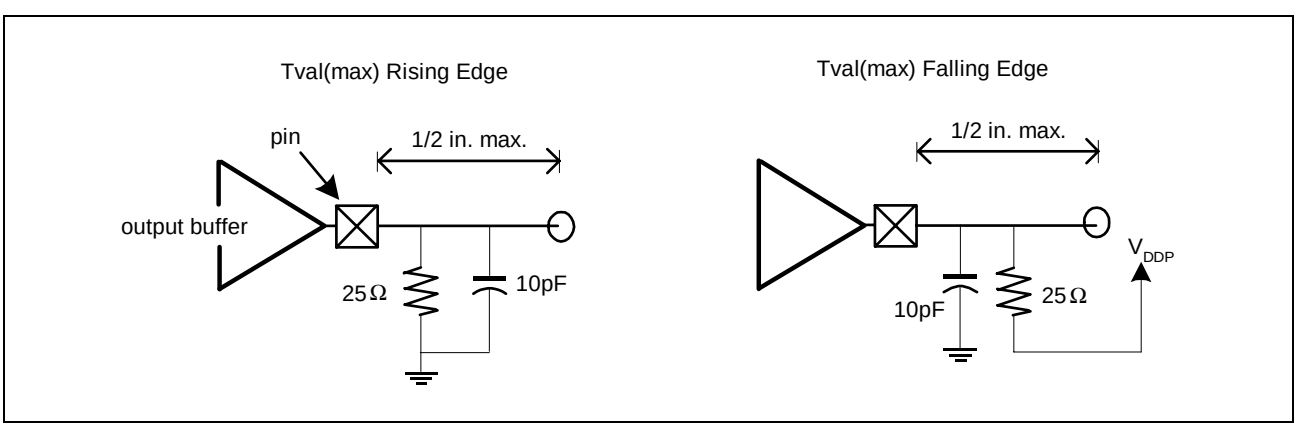


Figure 45 Load circuits for Maximum Clock to Signal Valid Delays

Parameters for Measurement Conditions

Symbol	Value	Units	Notes
V_{TH}	0.6 V_{DDP}	V	1)
V_{TL}	0.2 V_{DDP}	V	1)
V_{TEST}	0.4 V_{DDP}	V	
V_{STEP} (rising edge)	0.285 V_{DDP}	V	
V_{STEP} (falling edge)	0.615 V_{DDP}	V	
V_{MAX}	0.4 V_{DDP}	V	2)
Input signal edge rate	1	V / ns	

1) The input test is done with 0.1 V_{DDP} overdrive. Timing parameters must be met with no more overdrive than this.

2) V_{MAX} specifies the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.

Package Outline

Plastic Package, P-BGA-388-2 (SMD)
(Plastic Ball Grid Array Package)

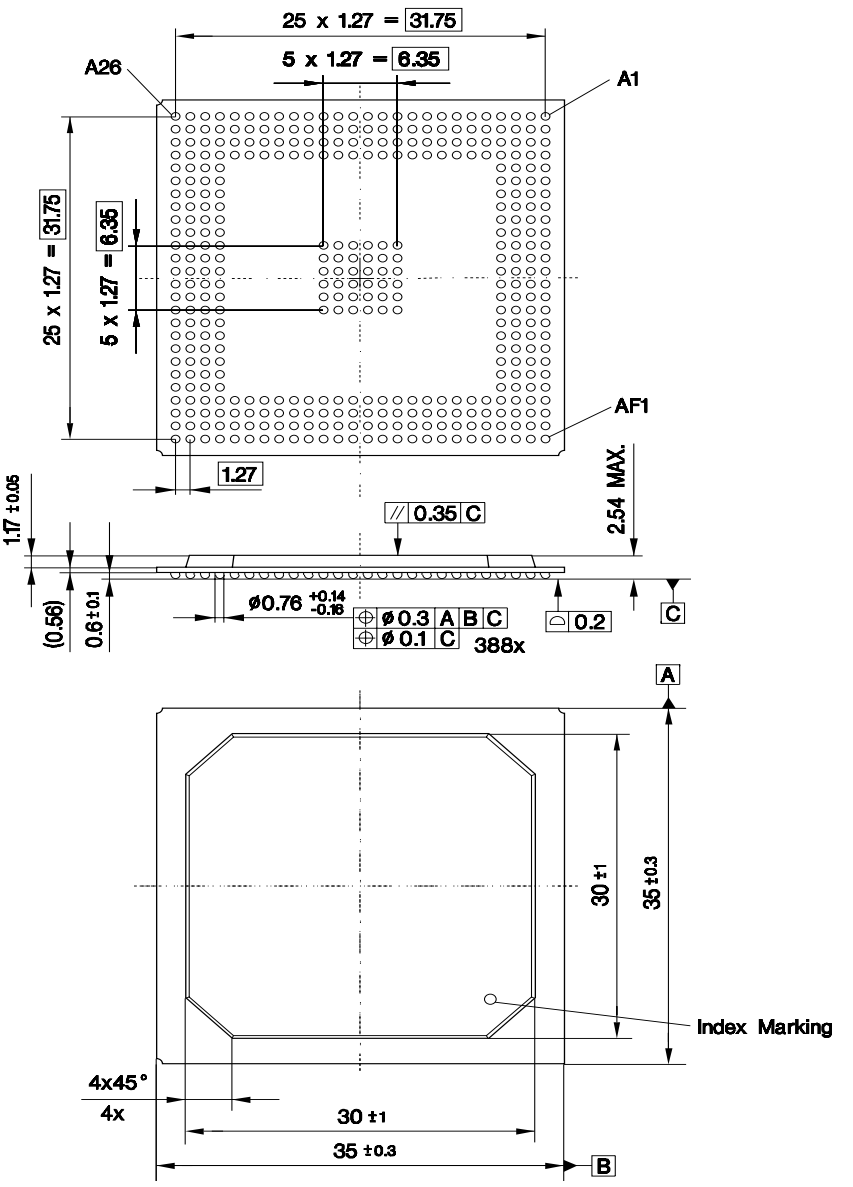


Figure 46 P-BGA-388-2 Package

Sorts of Packing

Package outlines for tubes, trays, etc. are contained in Data Sheet “Package Information”

SMD = Surface Mounted Device

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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Dr. Ulrich Schumacher

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