Data Sheet, V1.2, Dec. 2002

TC1765

32-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

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TC1765 Data Sheet
Preliminary
Revision History: 2002-12 V1.2

Previous Version: V1.1, 2002-10, V1.0, 2002-05

Page	Subjects (major changes since last revision)
Changes from V1.1 to V1.2	
58, **59**	Overshoot conditions (notes [2] and [3]) for digital supply voltages added
60	Class A pins: input low voltage V_{ILmin} (CMOS) improved; pull-up/pull-down current spec corrected and completed;
61	Class A pins: pull-up/pull-down current spec corrected and completed;
62	Note [7] inserted
69	Note [3] added to “Sum of I_{DDS}”
80	t_{30min} corrected
83	Package outlines updated (no more “Preliminary” in drawing)
Changes from V1.0 to V1.1	
All	In general: Data Sheet status changed from “Advance Information” to “Preliminary”
22	The SSC RXFIFO and TXFIFO are 4-stage FIFOs (not 8-stage)
61	Input hysteresis corrected
62	Footnote [10] added
66	Footnote [8]: word “numeric” added
69	Missing power supply currents now specified
74	Last paragraph modified because of **Figure 29** correction
75	**Figure 29** corrected and improved
81	t_{55} added (min. value) and corrected (max. value)
82	t_{61min} and t_{62min} corrected

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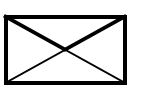

Preliminary

32-Bit Single-Chip Microcontroller TC1765
TriCore Family

- High Performance 32-bit TriCore CPU with 4-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU/System Clock
- Dual Issue super-scalar implementation
  - Instruction triple issue
- Circular Buffer and bit-reverse addressing modes for DSP algorithms
- Flexible multi-master interrupt system
- Very fast interrupt response time
- Hardware controlled context switch for task switch and interrupts
- 48 Kbytes of on-chip SRAM for data and time critical code
- 8-channel DMA Controller for FPI Bus transactions
- Built-in calibration support
- On-chip Flexible Peripheral Interface Bus (FPI Bus) for interconnections of functional units
- External Bus Interface Unit (EBU) with dedicated pins used for
  - Communication with external data memories and peripheral units
  - Instruction fetches from external Burst Flash program memories
- On-Chip Peripheral Units
  - General Purpose Timer Array (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex I/O management
  - Multifunctional General Purpose Timer Unit (GPTU) with three 32-bit timer/counters
  - Two Asynchronous/Synchronous Serial Channels (ASC0, ASC1) with baudrate generator, parity, framing and overrun error detection
  - Two High Speed Synchronous Serial Channels (SSC0, SSC1) with programmable data length and shift direction
  - TwinCAN Module with two interconnected CAN nodes for high efficiency data handling via FIFO buffering and gateway data transfer
  - Two Analog-to-Digital Converter Units (ADC0, ADC1) with 8-bit, 10-bit, or 12-bit resolution and 24 analog inputs
  - Watchdog Timer and System Timer
- 77 digital general purpose I/O lines and one 24-bit analog port
- On-chip Debug Support
- Power Management System
- Clock Generation Unit with PLL
- Two derivatives with upward compatible pin configuration
  - TC1765N
  - TC1765T (with additional 16-bit OCDS Level 2 trace port)
- Ambient temperature under bias: -40 °C to +125 °C
- P-LBGA-260 package

Preliminary

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies: the derivative itself, i.e. its function set, the temperature range, and the package and the type of delivery.

The TC1765 is available with the following ordering code:

Type	Ordering Code	Package	Description
SAK-TC1765N-L40EB	Q67121-C2326	P-LBGA-260	32-Bit Single-Chip Microcontroller 40 MHz, -40 °C to +125 °C
SAK-TC1765T-L40EB	Q67121-C2348	P-LBGA-260	32-Bit Single-Chip Microcontroller 40 MHz, -40 °C to +125 °C (with OCDS2 trace port)

Preliminary

Block Diagram

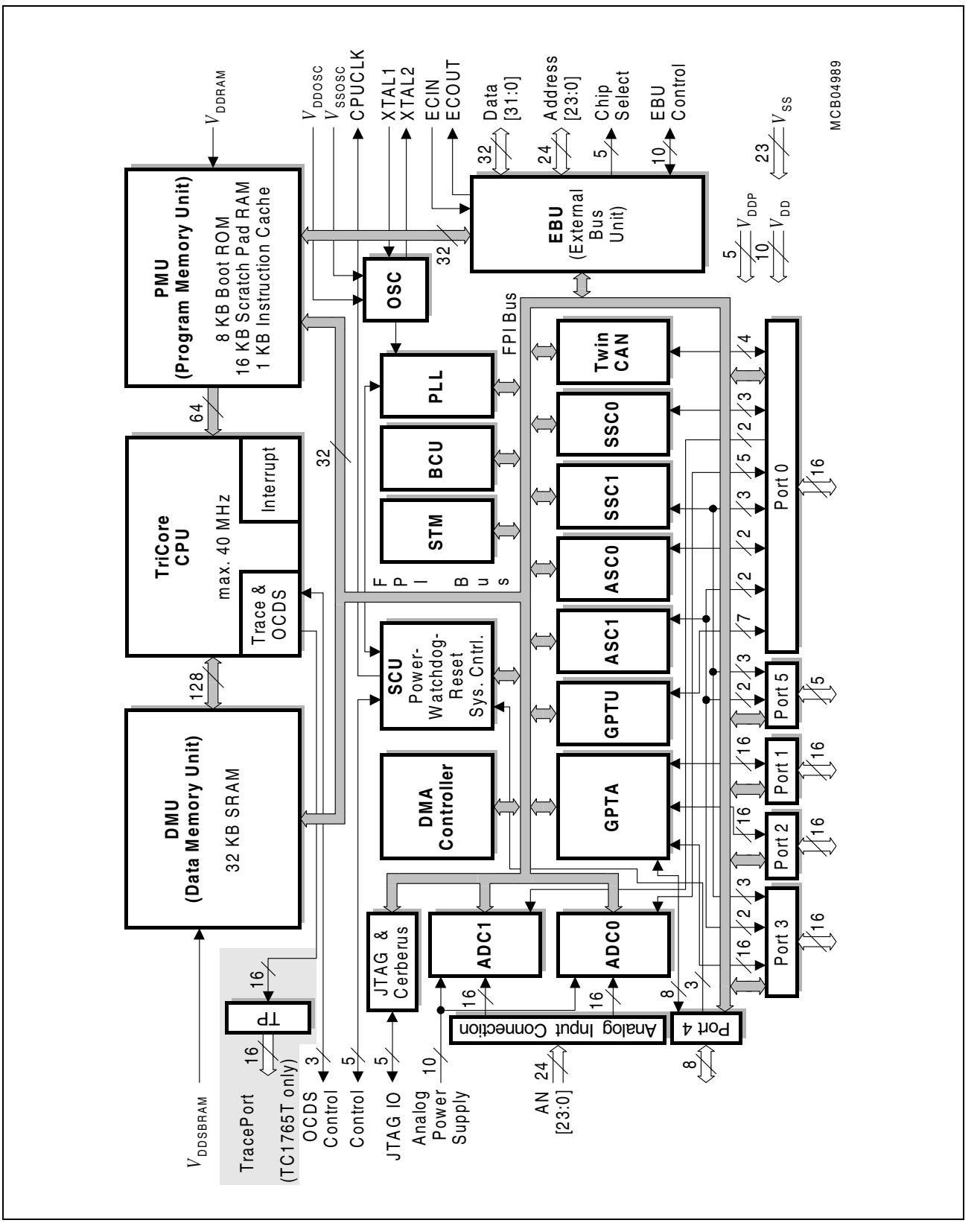

Figure 1 TC1765 Block Diagram

Preliminary

Logic Symbol

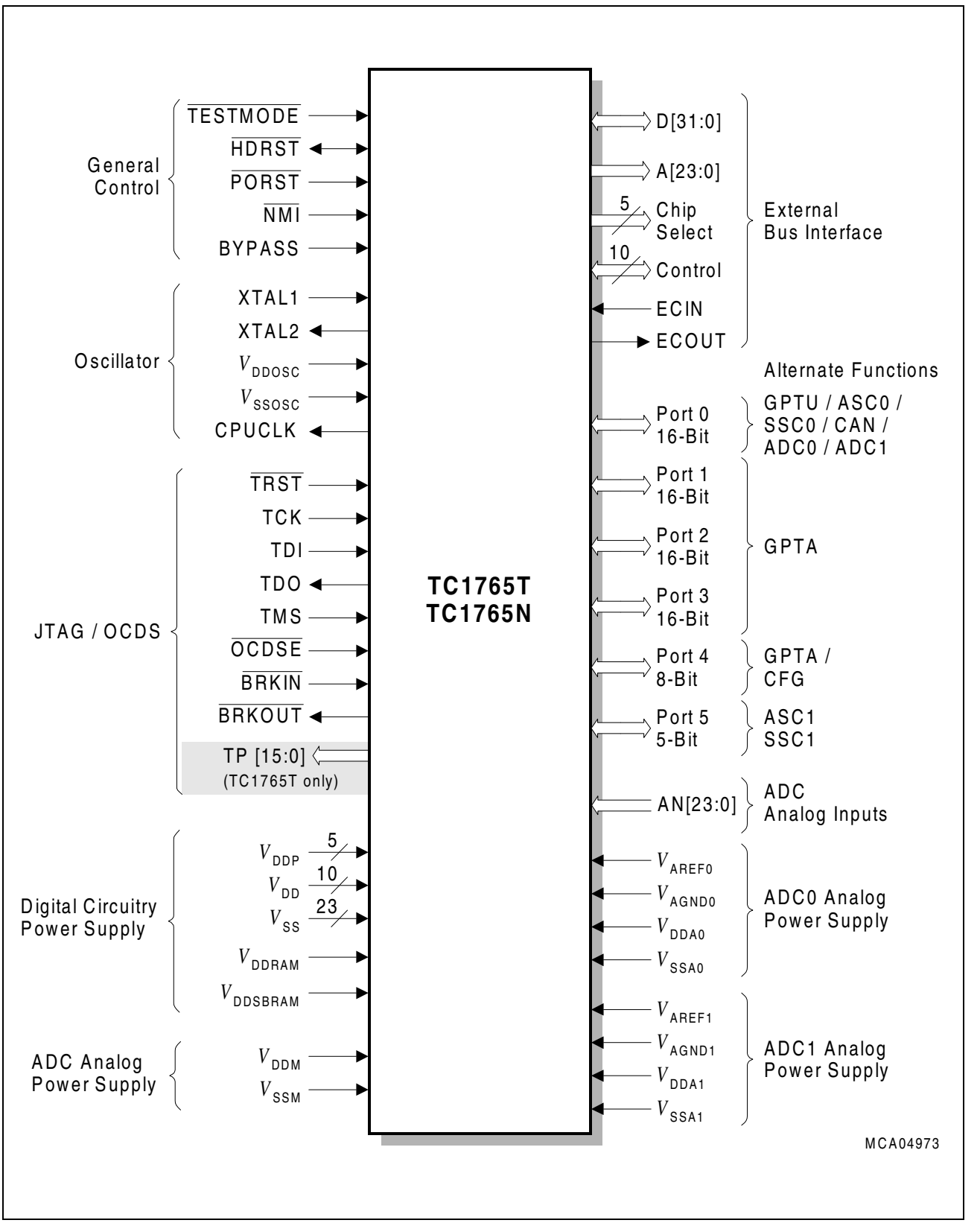

Figure 2 TC1765 Logic Symbol

Preliminary

Pin Configuration

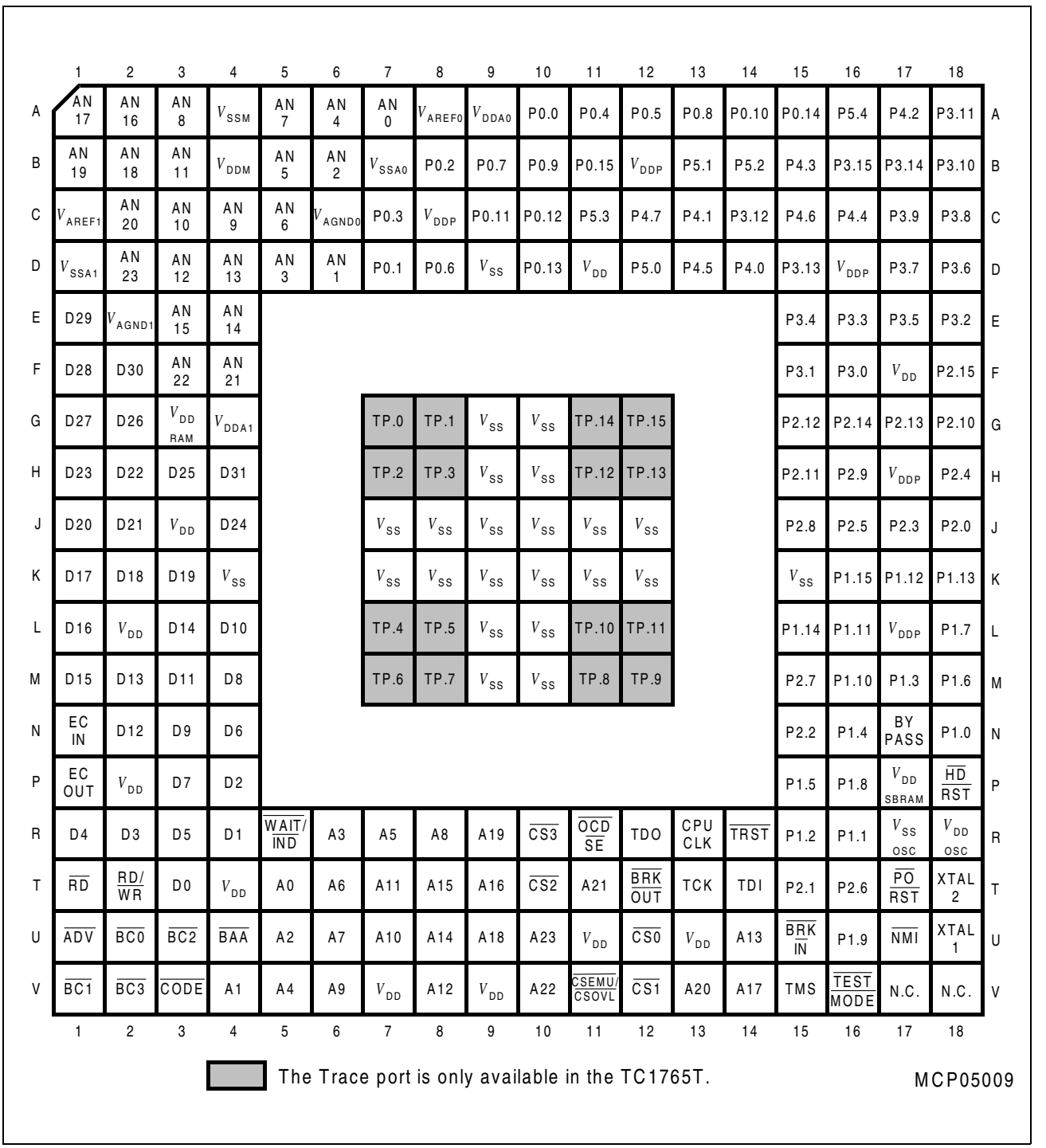

Figure 3 TC1765 Pinning for P-LBGA-260 Package (top view)

Preliminary

Table 1 Pin Definitions and Functions

Symbol	Pin	In Out	Functions
D[31:0]			**EBU Data Bus Lines**[1)2)] The EBU Data Bus Lines D[31:0] serve as external data bus.
D0	T3	I/O	Data bus line 0
D1	R4	I/O	Data bus line 1
D2	P4	I/O	Data bus line 2
D3	R2	I/O	Data bus line 3
D4	R1	I/O	Data bus line 4
D5	R3	I/O	Data bus line 5
D6	N4	I/O	Data bus line 6
D7	P3	I/O	Data bus line 7
D8	M4	I/O	Data bus line 8
D9	N3	I/O	Data bus line 9
D10	L4	I/O	Data bus line 10
D11	M3	I/O	Data bus line 11
D12	N2	I/O	Data bus line 12
D13	M2	I/O	Data bus line 13
D14	L3	I/O	Data bus line 14
D15	M1	I/O	Data bus line 15
D16	L1	I/O	Data bus line 16
D17	K1	I/O	Data bus line 17
D18	K2	I/O	Data bus line 18
D19	K3	I/O	Data bus line 19
D20	J1	I/O	Data bus line 20
D21	J2	I/O	Data bus line 21
D22	H2	I/O	Data bus line 22
D23	H1	I/O	Data bus line 23
D24	J4	I/O	Data bus line 24
D25	H3	I/O	Data bus line 25
D26	G2	I/O	Data bus line 26
D27	G1	I/O	Data bus line 27
D28	F1	I/O	Data bus line 28
D29	E1	I/O	Data bus line 29
D30	F2	I/O	Data bus line 30
D31	H4	I/O	Data bus line 31

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
A[23:0]			**EBU Address Bus Lines**[3)4)] The EBU Address Bus Lines A[23:0] serve as address bus.
A0	T5	O	Address bus line 0
A1	V4	O	Address bus line 1
A2	U5	O	Address bus line 2
A3	R6	O	Address bus line 3
A4	V5	O	Address bus line 4
A5	R7	O	Address bus line 5
A6	T6	O	Address bus line 6
A7	U6	O	Address bus line 7
A8	R8	O	Address bus line 8
A9	V6	O	Address bus line 9
A10	U7	O	Address bus line 10
A11	T7	O	Address bus line 11
A12	V8	O	Address bus line 12
A13	U14	O	Address bus line 13
A14	U8	O	Address bus line 14
A15	T8	O	Address bus line 15
A16	T9	O	Address bus line 16
A17	V14	O	Address bus line 17
A18	U9	O	Address bus line 18
A19	R9	O	Address bus line 19
A20	V13	O	Address bus line 20
A21	T11	O	Address bus line 21
A22	V10	O	Address bus line 22
A23	U10	O	Address bus line 23
			Chip Select Lines[3)5)]
$\overline{\text{CS0}}$	U12	O	Chip select output line 0
$\overline{\text{CS1}}$	V12	O	Chip select output line 1
$\overline{\text{CS2}}$	T10	O	Chip select output line 2
$\overline{\text{CS3}}$	R10	O	Chip select output line 3
$\overline{\text{CSEMU}}$/ $\overline{\text{CSOVL}}$	V11	O	**Chip Select for Emulator Region / Chip Select for Emulator Overlay Memory**[3)5)]

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
			EBU Control Lines[1)5)] The EBU control lines are required for controlling external memory or peripheral devices.
$\overline{BC0}$	U2	O	Byte control line 0
$\overline{BC1}$	V1	O	Byte control line 1
$\overline{BC2}$	U3	O	Byte control line 2
$\overline{BC3}$	V2	O	Byte control line 3
$\overline{RD}$	T1	O	Read control line
RD/$\overline{WR}$	T2	O	Write control line
$\overline{ADV}$	U1	O	Address valid output
$\overline{WAIT}$/$\overline{IND}$	R5	I	Wait input / End of burst input
$\overline{BAA}$	U4	O	Burst address advance output
$\overline{CODE}$	V3	O	Code fetch status output The $\overline{CODE}$ signal has the same timing as the chip select signals.

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
AN[23:0]			**ADC Analog Input Port** The ADC Analog Input Port provides 24 analog input lines for the A/D converters ADC0 and ADC1.
AN0	A7	I	Analog input 0
AN1	D6	I	Analog input 1
AN2	B6	I	Analog input 2
AN3	D5	I	Analog input 3
AN4	A6	I	Analog input 4
AN5	B5	I	Analog input 5
AN6	C5	I	Analog input 6
AN7	A5	I	Analog input 7
AN8	A3	I	Analog input 8
AN9	C4	I	Analog input 9
AN10	C3	I	Analog input 10
AN11	B3	I	Analog input 11
AN12	D3	I	Analog input 12
AN13	D4	I	Analog input 13
AN14	E4	I	Analog input 14
AN15	E3	I	Analog input 15
AN16	A2	I	Analog input 16
AN17	A1	I	Analog input 17
AN18	B2	I	Analog input 18
AN19	B1	I	Analog input 19
AN20	C2	I	Analog input 20
AN21	F4	I	Analog input 21
AN22	F3	I	Analog input 22
AN23	D2	I	Analog input 23

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P0		I/O	**Port 0**[6] Port 0 is a 16-bit bi-directional general purpose I/O port that is also used as input/output for ASC0, SSC0, CAN, GPTU, ADC0, ADC1, and the DMA Controller.	
P0.0	A10	I/O	GPT0	GPTU I/O line 0 /
		I	AD0EXTIN0	ADC0 external trigger input 0
P0.1	D7	I/O	GPT1	GPTU I/O line 1
		I	AD0EXTIN1	ADC0 external trigger input 1
		I	DMREQ0A	DMA request input 0A
P0.2	B8	I/O	GPT2	GPTU I/O line 2
		I	AD1EXTIN0	ADC1 external trigger input 0
		I	DMREQ1A	DMA request input 1A
P0.3	C7	I/O	GPT3	GPTU I/O line 3
		I	AD1EXTIN1	ADC1 external trigger input 1
P0.4	A11	I/O	GPT4	GPTU I/O line 4 /
		O	AD0EMUX0	ADC0 external multiplexer control 0
P0.5	A12	I/O	GPT5	GPTU I/O line 5
		O	AD0EMUX1	ADC0 external multiplexer control 1
P0.6	D8	I/O	GPT6	GPTU I/O line 6
		O	AD0EMUX2	ADC0 external multiplexer control 2
P0.7	B9	I/O	RXD0	ASC0 receiver input/output
P0.8	A13	O	TXD0	ASC0 transmitter output
P0.9	B10	I/O	SCLK0	SSC0 clock input/output
P0.10	A14	I/O	MRST0	SSC0 master receive input / SSC0 slave transmit output
P0.11	C9	I/O	MTSR0	SSC0 master transmit output / SSC0 slave receive input
P0.12	C10	I	RXDCAN0	CAN receiver input 0
P0.13	D10	O	TXDCAN0	CAN transmitter output 0
P0.14	A15	I	RXDCAN1	CAN receiver input 1
P0.15	B11	O	TXDCAN1	CAN transmitter output 1

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P1		I/O	**Port 1**[6)] Port 1 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P1.0	N18	I/O	IN0 / OUT0 line of GPTA
P1.1	R16	I/O	IN1 / OUT1 line of GPTA
P1.2	R15	I/O	IN2 / OUT2 line of GPTA
P1.3	M17	I/O	IN3 / OUT3 line of GPTA
P1.4	N16	I/O	IN4 / OUT4 line of GPTA
P1.5	P15	I/O	IN5 / OUT5 line of GPTA
P1.6	M18	I/O	IN6 / OUT6 line of GPTA
P1.7	L18	I/O	IN7 / OUT7 line of GPTA
P1.8	P16	I/O	IN8 / OUT8 line of GPTA
P1.9	U16	I/O	IN09 / OUT9 line of GPTA
P1.10	M16	I/O	IN10 / OUT10 line of GPTA
P1.11	L16	I/O	IN11 / OUT11 line of GPTA
P1.12	K17	I/O	IN12 / OUT12 line of GPTA
P1.13	K18	I/O	IN13 / OUT13 line of GPTA
P1.14	L15	I/O	IN14 / OUT14 line of GPTA
P1.15	K16	I/O	IN15 / OUT15 line of GPTA
P2		I/O	**Port 2**[6)] Port 2 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P2.0	J18	I/O	IN16 / OUT16 line of GPTA
P2.1	T15	I/O	IN17 / OUT17 line of GPTA
P2.2	N15	I/O	IN18 / OUT18 line of GPTA
P2.3	J17	I/O	IN19 / OUT19 line of GPTA
P2.4	H18	I/O	IN20 / OUT20 line of GPTA
P2.5	J16	I/O	IN21 / OUT21 line of GPTA
P2.6	T16	I/O	IN22 / OUT22 line of GPTA
P2.7	M15	I/O	IN23 / OUT23 line of GPTA
P2.8	J15	I/O	IN24 / OUT24 line of GPTA
P2.9	H16	I/O	IN25 / OUT25 line of GPTA
P2.10	G18	I/O	IN26 / OUT26 line of GPTA
P2.11	H15	I/O	IN27 / OUT27 line of GPTA
P2.12	G15	I/O	IN28 / OUT28 line of GPTA
P2.13	G17	I/O	IN29 / OUT29 line of GPTA
P2.14	G16	I/O	IN30 / OUT30 line of GPTA
P2.15	F18	I/O	IN31 / OUT31 line of GPTA

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P3		I/O	**Port 3**[6] Port 3 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P3.0	F16	I/O	IN32 / OUT32 line of GPTA
P3.1	F15	I/O	IN33 / OUT33 line of GPTA
P3.2	E18	I/O	IN34 / OUT34 line of GPTA
P3.3	E16	I/O	IN35 / OUT35 line of GPTA
P3.4	E15	I/O	IN36 / OUT36 line of GPTA
P3.5	E17	I/O	IN37 / OUT37 line of GPTA
P3.6	D18	I/O	IN38 / OUT38 line of GPTA
P3.7	D17	I/O	IN39 / OUT39 line of GPTA
P3.8	C18	I/O	IN40 / OUT40 line of GPTA
P3.9	C17	I/O	IN41 / OUT41 line of GPTA
P3.10	B18	I/O	IN42 / OUT42 line of GPTA
P3.11	A18	I/O	IN43 / OUT43 line of GPTA
P3.12	C14	I/O	IN44 / OUT44 line of GPTA
P3.13	D15	I/O	IN45 / OUT45 line of GPTA
P3.14	B17	I/O	IN46 / OUT46 line of GPTA
P3.15	B16	I/O	IN47 / OUT47 line of GPTA
P4		I/O	**Port 4**[6] Port 4 is an 8-bit bidirectional general purpose I/O port which also serves as input/output for the GPTA or external request input for the DMA controller. During hardware reset the port 4 lines are also used as start-up configuration selection inputs and PLL clock selection inputs.
P4.0	D14	I/O	IN48 / OUT48 line of GPTA
P4.1	C13	I/O I	IN49 / OUT49 line of GPTA / DMREQ0B DMA request input 0B
P4.2	A17	I/O I	IN50 / OUT50 line of GPTA / DMREQ1B DMA request input 1B
P4.3	B15	I/O	IN51 / OUT51 line of GPTA
P4.4	C16	I/O	IN52 / OUT52 line of GPTA / CFG[0]
P4.5	D13	I/O	IN53 / OUT53 line of GPTA / CFG[1]
P4.6	C15	I/O	IN54 / OUT54 line of GPTA / CFG[2]
P4.7	C12	I/O	IN55 / OUT55 line of GPTA / GPTA emergency shut down **CFG[2:0]: Start-up Configuration Selection Inputs** These pins are sampled during power-on reset ($\overline{\text{PORST}}$ = 0). The configuration inputs define the boot options of the TC1765 after a hardware reset operation.

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P5		I/O	**Port 5**[6] Port 5 is a 5-bit bidirectional general purpose I/O port which also serves as input or output for ASC1 and SSC1.	
P5.0	D12	I/O	RXD1	ASC1 receiver input/output
		I	DMREQ0C	DMA request input 0C
P5.1	B13	O	TXD1	ASC1 transmitter output
		I	DMREQ1C	DMA request input 1C
P5.2	B14	I/O	SCLK1	SSC1 clock input/output
P5.3	C11	I/O	MRST1	SSC1 master receive input / SSC1 slave transmit output
P5.4	A16	I/O	MTSR1	SSC1 master transmit output / SSC1 slave receive input
TP		O	**OCDS-2 Trace Port**[3] TP is the OCDS Level 2 Trace Port. The Trace port is only available in the TC1765T. The TP outputs are tristated during reset and deep sleep mode.	
TP.0	G7	O	Trace output 0	
TP.1	G8	O	Trace output 1	
TP.2	H7	O	Trace output 2	
TP.3	H8	O	Trace output 3	
TP.4	L7	O	Trace output 4	
TP.5	L8	O	Trace output 5	
TP.6	M7	O	Trace output 6	
TP.7	M8	O	Trace output 7	
TP.8	M11	O	Trace output 8	
TP.9	M12	O	Trace output 9	
TP.10	L11	O	Trace output 10	
TP.11	L12	O	Trace output 11	
TP.12	H11	O	Trace output 12	
TP.13	H12	O	Trace output 13	
TP.14	G11	O	Trace output 14	
TP.15	G12	O	Trace output 15	
$\overline{\text{TRST}}$[7]	R14	I	**JTAG Module Reset/Enable Input** A low level at this pin resets and disables the JTAG module. A high level enables the JTAG module.	
TCK[7]	T13	I	**JTAG Module Clock Input**	
TDI[8]	T14	I	**JTAG Module Serial Data Input**	

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
TDO	R12	O	**JTAG Module Serial Data Output**[3]
TMS[8]	V15	I	**JTAG Module State Machine Control Input**
$\overline{\text{OCDSE}}$[8]	R11	I	**OCDS Enable Input** A low level on this pin during power-on reset ($\overline{\text{PORST}}$ = 0) enables the on-chip debug support (OCDS). In addition, the level of this pin during power-on reset determines the boot configuration.
$\overline{\text{BRKIN}}$[8]	U15	I	**OCDS Break Input** A low level on this pin causes a break in the chip's execution when the OCDS is enabled. In addition, the level of this pin during power-on reset determines the boot configuration.
$\overline{\text{BRKOUT}}$	T12	O	**OCDS Break Output**[3] A low level on this pin indicates that a programmable OCDS event has occurred.
$\overline{\text{NMI}}$[8]	U17	I	**Non-Maskable Interrupt Input** A high-to-low transition on this pin causes an NMI-Trap request to the CPU.
$\overline{\text{HDRST}}$[8]	P18	I/O	**Hardware Reset Input / Reset Indication Output**[6] Assertion of this open-drain bidirectional pin causes a synchronous reset of the chip through external circuitry. The internal reset circuitry drives this pin in response to a power-on, hardware, watchdog and power-down wake-up reset for a specific period of time. For a software reset, it is programmable whether this pin is activated or not.
$\overline{\text{PORST}}$	T17	I	**Power-on Reset Input** A low level on $\overline{\text{PORST}}$ causes an asynchronous reset of the entire chip. During power-up of the TC1765, this pin must be held active (low).
BYPASS	N17	I	**PLL Bypass Control Input** This pin is sampled during power-on reset ($\overline{\text{PORST}}$ = 0). If BYPASS is at high level, direct drive mode operation of the clock circuitry is selected and the PLL is bypassed.

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
XTAL1 **XTAL2**	U18 T18	I O	**Oscillator/PLL/Clock Generator Input/Output Pins** XTAL1 is the input to the oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the oscillator amplifier circuit. For clocking the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
ECOUT	P1	O	**EBU Clock Output**[3]
ECIN	N1	–	**EBU Clock Input** The ECIN pin is used to latch the data from external components into the EBU. This pin has to be connected to the ECOUT pin. Additional delay elements might be used to adapt to long delays at the address and data lines.
CPUCLK	R13	O	**CPU Clock Output**[3] General purpose clock output (can be disabled if not used). In addition, the OCDS-2 trace output data are synchronous to this clock.
$\overline{\text{TEST}}$ MODE[8]	V16	I	**Test Mode Select Input** For normal operation of the TC1765 this pin should be connected to V_{DD}.
V_{DDOSC}	R18	–	**Main Oscillator Power Supply (2.5 V)**[9]
V_{SSOSC}	R17	–	**Main Oscillator Ground**
V_{DD}	J3, P2, T4, V7, U11, U13, L2, F17, D11, V9	–	**Core and EBU Power Supply (2.5 V)**[9]

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
V_{DDP}	L17, H17, D16, B12, C8	–	**Port 0 to 5 and Dedicated Pins Power Supply (3.3 - 5 V)**[10]
V_{DDRAM}	G3	–	**Power Supply for PMU Memories (2.5 V)**[9]
$V_{DDSBRAM}$	P17	–	**Power Supply for DMU Memory (2.5 V)**[9] Used for normal and stand-by operating mode.
V_{SS}	D9, K4, K15, G9, G10, H9, H10, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, L9, L10, M9, M10	–	**Ground**

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
V_{DDM}	B4	–	**ADC Analog Part Power Supply (5 V)**[10]
V_{SSM}	A4	–	**ADC Analog Part Ground for V_{DDM}**
V_{DDA0}	A9	–	**ADC0 Analog Part Power Supply (2.5 V)**[9]
V_{SSA0}	B7	–	**ADC0 Analog Part Ground for V_{DDA0}**
V_{DDA1}	G4	–	**ADC1 Analog Part Power Supply (2.5 V)**[9]
V_{SSA1}	D1	–	**ADC1 Analog Part Ground for V_{DDA1}**
V_{AREF0}	A8	–	**ADC0 Reference Voltage**[10]
V_{AGND0}	C6	–	**ADC0 Reference Ground**
V_{AREF1}	C1	–	**ADC1 Reference Voltage**[10]
V_{AGND1}	E2	–	**ADC1 Reference Ground**[10]
N.C.	V17, V18	–	**Not Connected;** reserved for future expansions

1) These pins have a drive capability of 600 µA when used as outputs.

2) These pins can be connected with internal pull-up devices by setting bit SCU_CON.EBUDPEN.

3) These outputs have a drive capability of 600 µA.

4) These pins can be connected with internal pull-up devices by setting bit SCU_CON.EBUAPEN.

5) These pins can be connected with internal pull-up devices by setting bit SCU_CON.EBUCPEN.

6) These pins have a drive capability of 2.4 mA when used as outputs.

7) These pins have an internal pull-down device connected.

8) These pins have an internal pull-up device connected.

9) The voltage on power supply pins marked with 10) has to be raised earlier or at least at the same time (= time window of 1 µs) than on power supply pins marked with 9) (details see power supply section on **Page 54**).

10) See note 9).

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Parallel Ports

The TC1765 has 77 digital input/output port lines organized into four parallel 16-bit ports (Port 0 to Port 3), one 8-bit port (Port 4), and one 5-bit port (Port 5). Additionally, 24 analog input port lines are available. The External Bus Unit (EBU) is provided with dedicated data, address, and control lines. A 16-bit Trace Port is available only in the TC1765T.

The digital parallel ports Port 0 to Port 5 can be all used as general purpose I/O lines or they can perform input/output functions for the on-chip peripheral units. The on-chip External Bus Interface Unit allows to communicate with external memories, external peripherals, or external debugging devices. An overview on the port-to-peripheral unit assignment is shown in **Figure 4**.

*Note: For further details on the three pin classes of the TC1765 I/O pins see also **Table 8** on **Page 56**):*

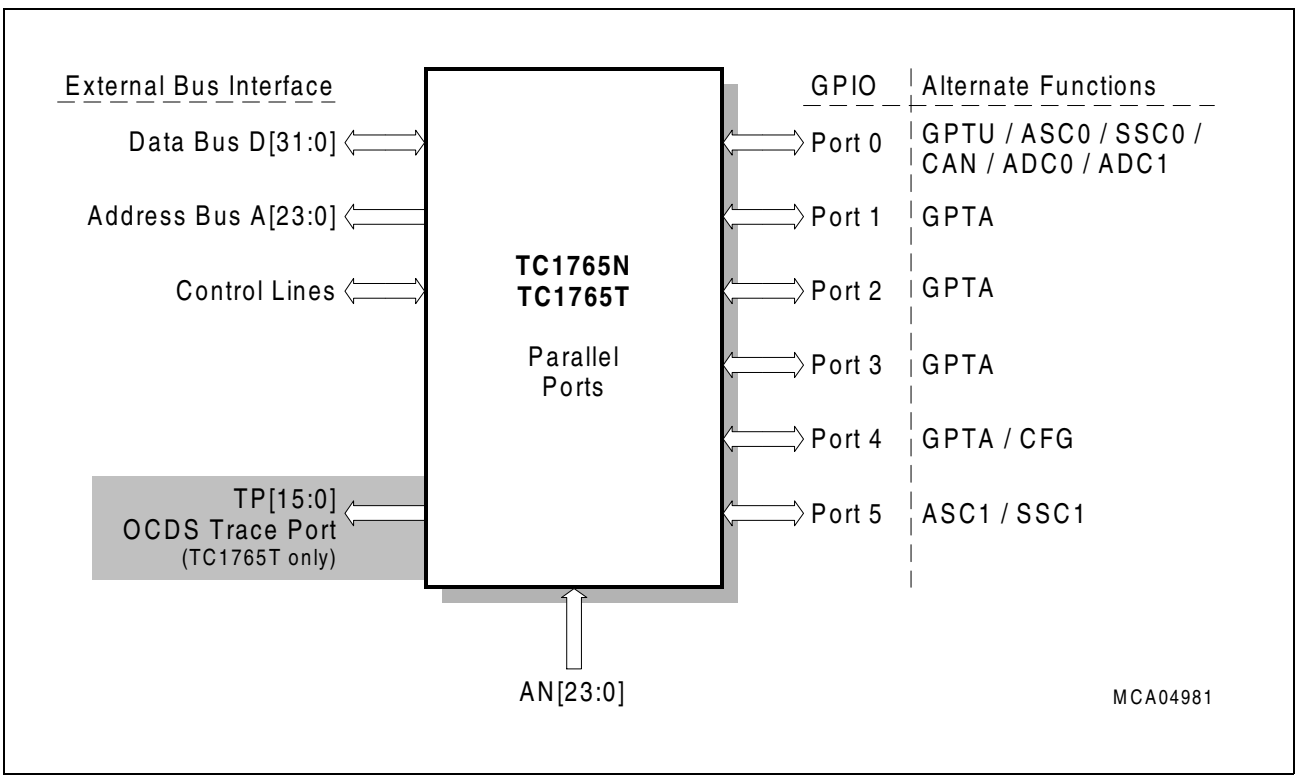

Figure 4 Parallel Ports of the TC1765

Preliminary

Serial Interfaces

The TC1765 includes five serial peripheral interface units:

- Two Asynchronous/Synchronous Serial Interfaces (ASC0 and ASC1)
- Two High-Speed Synchronous Serial Interfaces (SSC0 and SSC1)
- One TwinCAN Interface

Asynchronous/Synchronous Serial Interfaces

Figure 5 shows a global view of the functional blocks of the two Asynchronous/ Synchronous Serial interfaces ASC0 and ASC1.

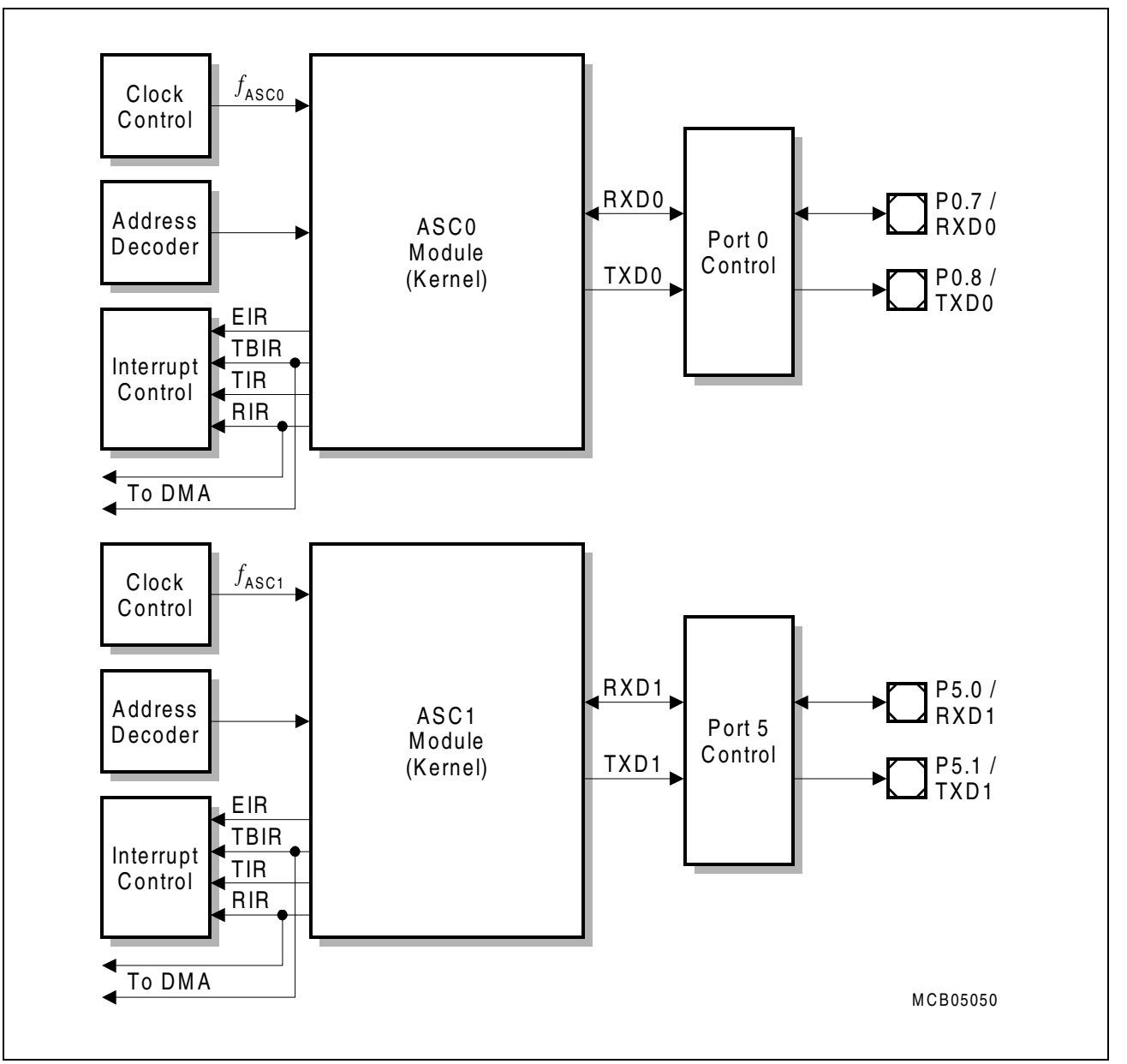

Figure 5 General Block Diagram of the ASC Interfaces

Preliminary

Each ASC module, ASC0 and ASC1, communicates with the external world via two I/O lines. The RXD line is the receive data input signal (in Synchronous Mode also output). TXD is the transmit output signal. Clock control, address decoding, and interrupt service request control are managed outside the ASC module kernel.

The Asynchronous/Synchronous Serial Interfaces provide serial communication between the TC1765 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock which is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data are double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal that can be very accurately adjusted by a prescaler implemented as a fractional divider.

Features:

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baud rate from 2.5 Mbit/s to 0.6 Bit/s (@ 40 MHz clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 5 Mbit/s to 406.9 Bit/s (@ 40 MHz clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - On a transmitter buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receiver buffer full condition
  - On an error condition (frame, parity, overrun error)

High-Speed Synchronous Serial Interfaces

Figure 6 shows a global view of the functional blocks of the two High-Speed Synchronous Serial interfaces SSC0 and SSC1.

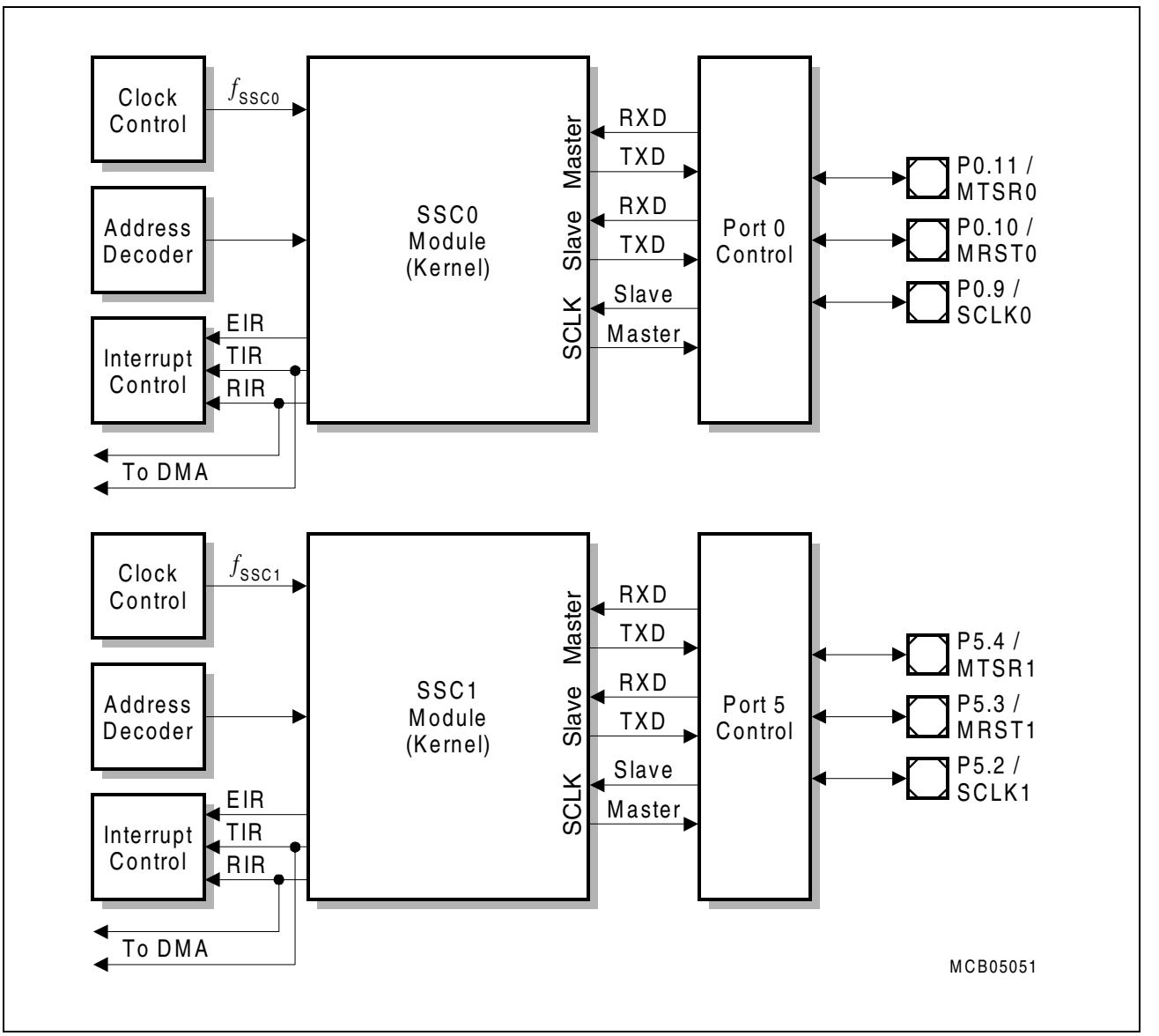

Figure 6 General Block Diagram of the SSC Interfaces

Each of the SSC modules has three I/O lines, located at Port 0 and Port 5. Each of the SSC modules is further supplied by separate clock control, interrupt control, address decoding, and port control logic.

The SSC supports full-duplex and half-duplex serial synchronous communication up to 20 Mbit/s (@ 40 MHz module clock) with receive and transmit FIFO support. The serial clock signal can be generated by the SSC itself (master mode) or can be received from an external master (slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices. Transmission

and reception of data are double-buffered. A 16-bit baud rate generator provides the SSC with a separate serial clock signal.

Features:

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Flexible data format
  - Programmable number of data bits: 2-bit to 16 bit
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate generation from 20 Mbit/s to 305.18 Bit/s (@ 40 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Three-pin interface
  - Flexible SSC pin configuration
- 4-stage receive FIFO (RXFIFO) and 4-stage transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 2 to 16 bit FIFO data width
  - Programmable receive/transmit interrupt trigger level
  - Receive and transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

Preliminary

TwinCAN Interface

Figure 7 shows a global view of the functional blocks of the TwinCAN module.

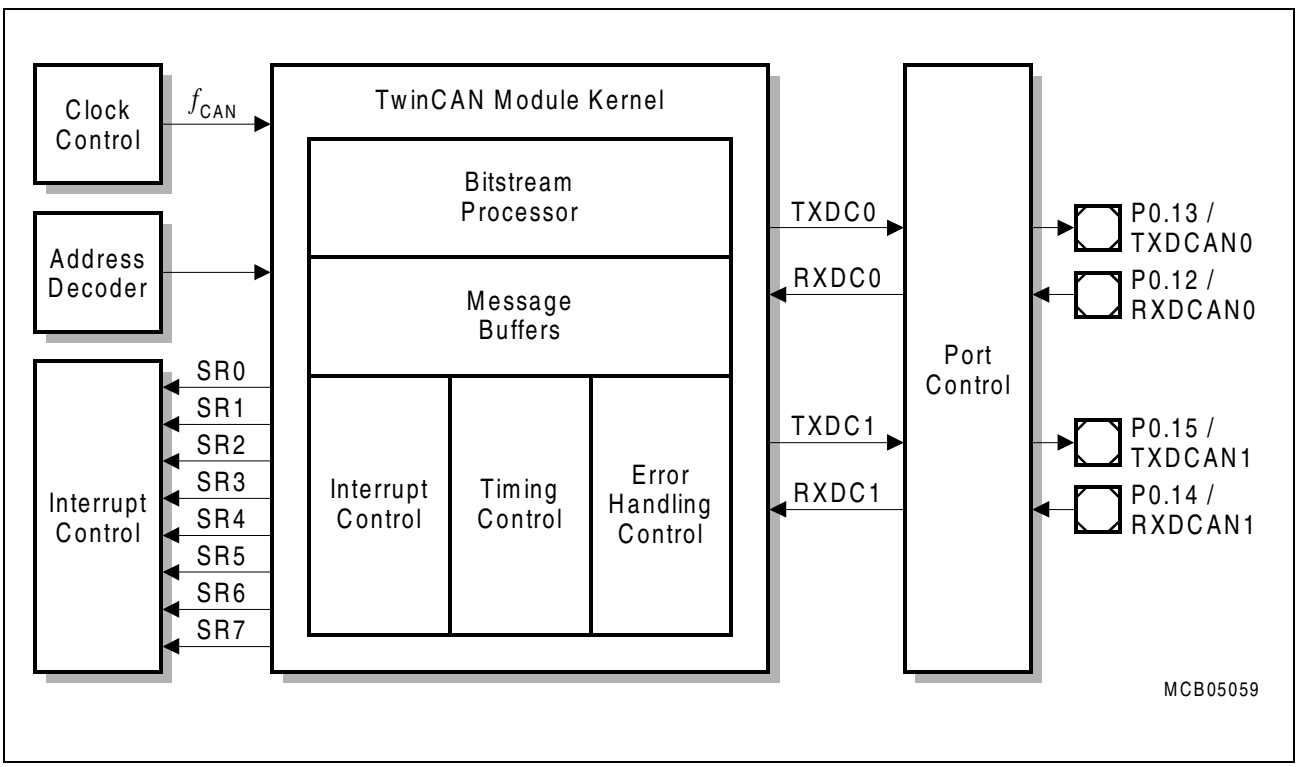

Figure 7 General Block Diagram of the TwinCAN Module

The TwinCAN module has four I/O lines located at Port 0. The TwinCAN module is further supplied by a clock control, interrupt control, address decoding, and port control logic.

The TwinCAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames are handled in accordance to CAN specification V2.0 part B (active). Each of the two Full-CAN nodes can receive and transmit standard frames with 11-bit identifiers as well as with extended frames with 29-bit identifiers.

Both CAN nodes share the TwinCAN module's resources to optimize the CAN bus traffic handling and to minimize the CPU load. The flexible combination of Full-CAN functionality and the FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the increased number of message objects permit precise and convenient CAN bus traffic handling.

Depending on the application, each of the thirty-two message objects can be individually assigned to one of the two CAN nodes. Gateway functionality allows automatic data exchange between two separate CAN bus systems, which decreases CPU load and improves the real time behavior of the entire system.

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The bit timings for both CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 Mbit/s. A pair of receive and transmit pins connect each CAN node to a bus transceiver.

Features:

- CAN functionality conforms to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1 Mbit/s is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Full-CAN functionality: 32 message objects can be individually
  - Assigned to one of the two CAN nodes
  - Configured as transmit or receive object
  - Participate in a 2, 4, 8, 16 or 32 message buffer with FIFO algorithm
  - Set up to handle frames with 11-bit or 29-bit identifiers
  - Provided with programmable acceptance mask register for filtering
  - Monitored via a frame counter
  - Configured to Remote Monitoring Mode
- Up to eight individually programmable interrupt nodes can be used.
- CAN Analyzer Mode for bus monitoring is implemented.

Timer Units

The TC1765 includes two timer units:

- General Purpose Timer Unit (GPTU)
- General Purpose Timer Array (GPTA)

General Purpose Timer Unit

Figure 8 shows a global view of the General Purpose Timer Unit (GPTU) module.

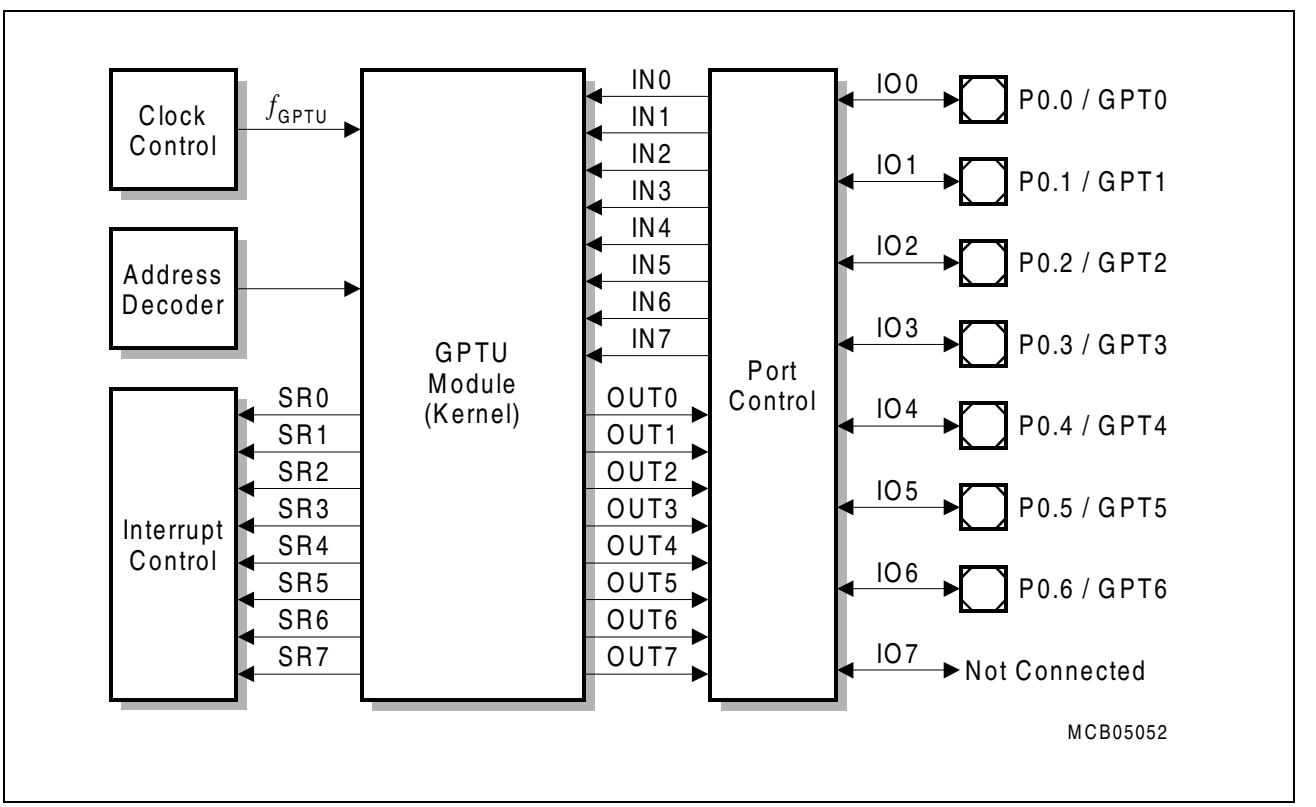

Figure 8 General Block Diagram of the GPTU Interface

The GPTU consists of three 32-bit timers designed to solve such application tasks as event timing, event counting, and event recording. The GPTU communicates with the external world via eight inputs and eight outputs located at Port 0.

The I/O has three timers (T0, T1, and T2) can operate independently from each other, or can be combined.

General Features:

- All timers are 32-bit precision timers with a maximum input frequency of f_{GPTU}.
- Events generated in T0 or T1 can be used to trigger actions in T2.
- Timer overflow or underflow in T2 can be used to clock either T0 or T1.
- T0 and T1 can be concatenated to form one 64-bit timer.

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Features of T0 and T1:

- Each timer has a dedicated 32-bit reload register with automatic reload on overflow.
- Timers can be split into individual 8-, 16-, or 24-bit timers with individual reload registers.
- Overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events.
- Two input pins can define a count option.

Features of T2:

- Count up or down is selectable
- Operating modes:
  - Timer
  - Counter
  - Quadrature counter (incremental/phase encoded counter interface)
- Options:
  - External start/stop, one-shot operation, timer clear on external event
  - Count direction control through software or an external event
  - Two 32-bit reload/capture registers
- Reload modes:
  - Reload on overflow or underflow
  - Reload on external event: positive transition, negative transition, or both transitions
- Capture modes:
  - Capture on external event: positive transition, negative transition, or both transitions
  - Capture and clear timer on external event: positive transition, negative transition, or both transitions
- Can be split into two 16-bit counter/timers
- Timer count, reload, capture, and trigger functions can be assigned to input pins. T0 and T1 overflow events can also be assigned to these functions.
- Overflow and underflow signals can be used to trigger T0 and/or T1 and to toggle output pins.
- T2 events are freely assignable to the service request nodes.

Preliminary

General Purpose Timer Array

Figure 9 shows a global block diagram of the General Purpose Timer Array (GPTA).

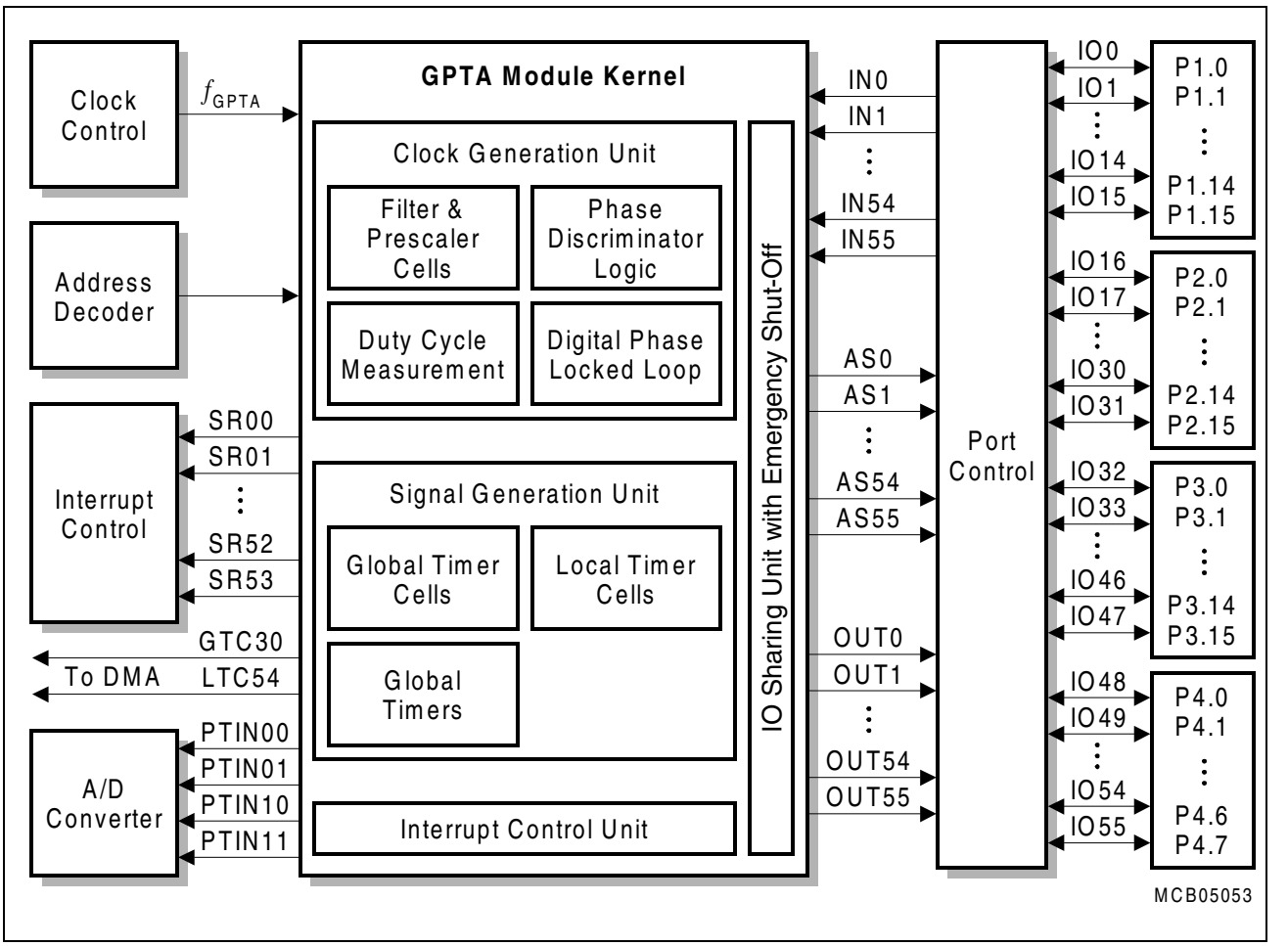

Figure 9 GPTA Module Block Diagram

The GPTA module has 56 input signals and 56 output signals which are connected with 56 Port 1, Port 2, Port 3, and Port 4 pins.

The General Purpose Timer Array (GPTA) provides important digital signal filtering and timer support whose combination enables autonomous and complex functionalities. This architecture allows easy implementation and easy validation of any kind of timer functions.

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The General Purpose Timer Array (GPTA) provides a set of hardware modules required for high speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated "Global Timer Cells".
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an event that occurred at an external port pin or at an internal FPC output. A GTC may be also used to control an external port pin with the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may be also logically tied together to drive a common external port pin with a complex signal waveform. LTCs — enabled in Timer Mode or Capture Mode — can be clocked or triggered by
  - A prescaled GPTA module clock,
  - An FPC, PDL, DCM, PLL, or GTC output signal line,
  - An external port pin.

Some input lines driven by processor I/O pads may be shared by a LTC and a GTC cell to trigger their programmed operation simultaneously.

The following list summarizes all blocks supported:

Clock Generation Unit:

- Filter and Prescaler Cell (FPC):
  - Six independent units
  - Three operating modes (Prescaler, Delayed Debounce Filter, Immediate Debounce Filter)
  - f_{GPTA} down-scaling capability
  - $f_{GPTA}/2$ maximum input signal frequency in Filter Mode
- Phase Discriminator Logic (PDL):
  - Two independent units
  - Two operating modes (2 and 3 sensor signals)
  - $f_{GPTA}/4$ maximum input signal frequency in 2-sensor mode, $f_{GPTA}/6$ maximum input signal frequency in 3-sensor mode
- Duty Cycle Measurement (DCM):
  - Four independent units
  - 0 - 100% margin and time-out handling

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  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency
- Digital Phase Locked Loop (PLL):
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

Signal Generation Unit:

- Global Timers (GT):
  - Two independent units
  - Two operating modes (Free Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency
- Global Timer Cell (GTC):
  - 32 independent units
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency
- Local Timer Cell (LTC):
  - 64 independent units
  - Three operating modes (Timer, Capture and Compare)
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

Interrupt Control Unit:

- 111 interrupt sources generating 54 service requests

I/O Sharing Unit:

- Interconnecting input and output lines from FPC, GTC, LTC and ports
- Emergency function

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Analog-to-Digital Converters

The two on-chip ADC modules of the TC1765 are analog to digital converters with 8-bit, 10-bit or 12-bit resolution including sample & hold functionality. The A/D converters operate by the method of the successive approximation. A multiplexer selects between up to 16 analog input channels for each ADC module. The 24 analog inputs are switched to the analog input channels of the ADC modules by a fixed scheme. Conversion requests are generated either under software control or by hardware (GPTA). An automatic self-calibration adjusts the ADC modules to changing temperatures or process variations.

Features:

- 8-bit, 10-bit, 12-bit A/D Conversion
- Successive approximation conversion method
- Fast conversion times: e.g. 10-bit conversion (without sample time): 2.05 µs
- Total Unadjusted Error (TUE) of ±2 LSB @ 10-bit resolution
- Integrated sample and hold functionality
- 24 analog input pins / 16 analog input channels of each ADC module
- Fix assignment of 24 analog input pins to the 32 ADC0/ADC1 input channels
- Dedicated control and status registers for each analog channel
- Flexible conversion request mechanisms
- Selectable reference voltages for each channel
- Programmable sample and conversion timing schemes
- Limit checking
- Flexible ADC module service request control unit
- Synchronization of the two on-chip A/D Converters
- Automatic control of an external analog input multiplexer for ADC0
- Equidistant samples initiated by timer
- Two trigger inputs, connected with the General Purpose Timer Array (GPTA)
- Two external trigger input pins of each ADC for generating conversion requests
- Power reduction and clock control feature

Figure 10 shows a global view of the ADC module kernel with the module specific interface connections.

The ADC modules communicate with the external world via five (ADC0) or two (ADC0) digital I/O lines and sixteen analog inputs. Clock control, address decoding, digital I/O port control, and service request generation is managed outside the ADC module kernel. The end of a conversion is indicated for each channel n (n = 0-15) by a pulse on the output signals SRCHn. These signals can be used to trigger a DMA transfer to read the conversion result automatically. Two trigger inputs and a synchronization bridge are used for internal control purposes.

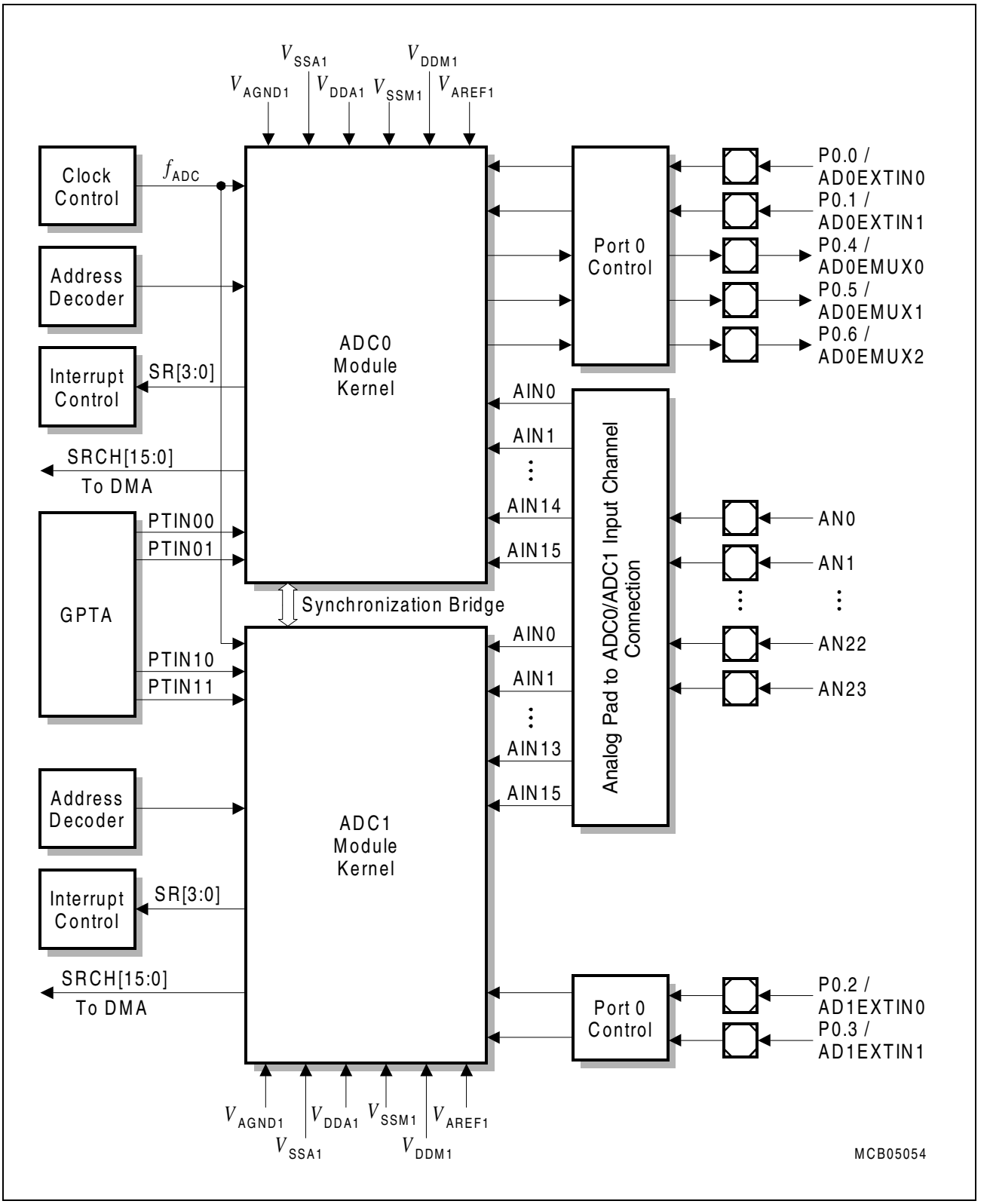

Figure 10 General Block Diagram of the ADC Interface

Preliminary

On-Chip Memories

The memory system of the TC1765 provides the following memories:

- Program Memory Unit (PMU) with
  - 8 Kbytes Boot ROM (BROM)
  - 16 Kbytes Code Scratch-Pad RAM (SPRAM)
  - 1 Kbyte Instruction Cache (ICACHE)
- Data Memory Unit (DMU) with
  - 32 Kbytes Data Memory (SRAM)
  - Can be used for standby operation during power-down states using a separate power supply

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Address Map

Table 2 defines the segment oriented address blocks of the TC1765 with its address range, size, and PMU/DMU access view. Table 3 shows the block address map of segment 15 which includes the on-chip peripheral units.

Table 2 TC1765 Block Address Map

Segment	Address Range	Size	Description	DMU Acc.	PMU Acc.[1]	
0 - 7	0000 0000$_H$ - 7FFF FFFF$_H$	2 GB	Reserved	–	–	
8	8000 0000$_H$ - 8FFF FFFF$_H$	256 MB	Reserved	via FPI	PMU local	cached
9	9000 0000$_H$ - 9FFF FFFF$_H$	256 MB	Reserved	DMU local	via FPI	
10	A000 0000$_H$ - AFFF FFFF$_H$	256 MB	External Memory Space	via FPI	via EBU or FPI	
11	B000 0000$_H$ - BDFF FFFF$_H$	224 MB	External Memory Space mappable into Segment 10	via FPI	via EBU or FPI	non-cached
	BE00 0000$_H$ - BEFF FFFF$_H$	16 MB	External Emulator Space		via FPI	
	BF00 0000$_H$ - BFFF DFFF$_H$	-16 MB	Reserved		PMU local	
	BFFF E000$_H$ - BFFF FFFF$_H$	8 KB	Boot ROM 4 Kbytes general purpose 4 Kbytes factory test support			
12	C000 0000$_H$ - C000 3FFF$_H$	16 KB	Local Code Scratch-Pad RAM (SPRAM)	via FPI	PMU local	
	C000 4000$_H$ - C7FF FEFF$_H$	–	Reserved			
	C7FF FF00$_H$ - C7FF FFFF$_H$	256 B	PMU Control Registers			
	C800 0000$_H$ - CFFF FFFF$_H$	–	Reserved			

Table 2 TC1765 Block Address Map (cont'd)

Segment	Address Range	Size	Description	DMU Acc.	PMU Acc.[1]	
13	$D000\ 0000_H$ - $D000\ 7FFF_H$	32 KB	Local Data Memory (SRAM)	DMU local	via FPI	non-cached
	$D000\ 8000_H$ - $D7FF\ FEFF_H$	–	Reserved			
	$D7FF\ FF00_H$ - $D7FF\ FFFF_H$	256 B	DMU Registers			
	$D800\ 0000_H$ - $DFFF\ FFFF_H$	256 MB	Reserved			
14	$E000\ 0000_H$ - $EFFF\ FFFF_H$	256 MB	External Peripheral and Data Memory Space	via FPI	not possible	
15	$F000\ 0000_H$ - $F000\ 3BFF_H$	-16 KB	On-Chip Peripherals & Ports	via FPI	not possible	non-cached
	$F000\ 3C00_H$ - $F000\ 3DFF_H$	512 B	DMA Registers			
	$F000\ 3E00_H$ - $F00F\ FFFF_H$	–	Reserved			
	$F010\ 0000_H$ - $F010\ 0BFF_H$	12 × 256 B	CAN Module			
	$F010\ 0C00_H$ - $FFFE\ FEFF_H$	–	Reserved			
	$FFFE\ FF00_H$ - $FFFE\ FFFF_H$	256 B	CPU Slave Interface Registers (CPS)			
	$FFFF\ 0000_H$ - $FFFF\ FFFF_H$	64 KB	Core SFRs + GPRs			

[1] The PMU can access external memory directly ("via EBU", only instruction accesses) or via the FPI Bus ("via FPI"). If both paths are possible as defined in this column, selection is done via SCU_CON.EXTIF.

Table 3 Block Address Map of Segment 15

Symbol	Description	Address Range	Size
SCU	System Control Unit	$F000\ 0000_H$ - $F000\ 00FF_H$	256 Bytes
–	Reserved	$F000\ 0100_H$ - $F000\ 01FF_H$	–
BCU	Bus Control Unit	$F000\ 0200_H$ - $F000\ 02FF_H$	256 Bytes
STM	System Timer	$F000\ 0300_H$ - $F000\ 03FF_H$	256 Bytes
OCDS	On-Chip Debug Support	$F000\ 0400_H$ - $F000\ 04FF_H$	256 Bytes
EBU	External Bus Unit	$F000\ 0500_H$ - $F000\ 05FF_H$	256 Bytes
–	Reserved	$F000\ 0600_H$ - $F000\ 06FF_H$	–
GPTU	General Purpose Timer Unit	$F000\ 0700_H$ - $F000\ 07FF_H$	256 Bytes
ASC0	Async./Sync. Serial Interface 0	$F000\ 0800_H$ - $F000\ 08FF_H$	256 Bytes
ASC1	Async./Sync. Serial Interface 1	$F000\ 0900_H$ - $F000\ 09FF_H$	256 Bytes
SSC0	High-Speed Synchronous Serial Interface 0	$F000\ 0A00_H$ - $F000\text{-}0AFF_H$	256 Bytes
SSC1	High-Speed Synchronous Serial Interface 1	$F000\ 0B00_H$ - $F000\text{-}0BFF_H$	256 Bytes
–	Reserved	$F000\ 0C00_H$ - $F000\ 17FF_H$	–
GPTA	General Purpose Timer Array	$F000\ 1800_H$ - $F000\ 1FFF_H$	8 × 256 Bytes
–	Reserved	$F000\ 2000_H$ - $F000\ 21FF_H$	–
ADC0	Analog-to-Digital Converter 0	$F000\ 2200_H$ - $F000\ 23FF_H$	2 × 256 Bytes
ADC1	Analog-to-Digital Converter 1	$F000\ 2400_H$ - $F000\ 25FF_H$	2 × 256 Bytes
–	Reserved	$F000\ 2600_H$ - $F000\ 27FF_H$	–
P0	Port 0	$F000\ 2800_H$ - $F000\ 28FF_H$	256 Bytes
P1	Port 1	$F000\ 2900_H$ - $F000\ 29FF_H$	256 Bytes
P2	Port 2	$F000\ 2A00_H$ - $F000\ 2AFF_H$	256 Bytes
P3	Port 3	$F000\ 2B00_H$ - $F000\ 2BFF_H$	256 Bytes
P4	Port 4	$F000\ 2C00_H$ - $F000\ 2CFF_H$	256 Bytes
P5	Port 5	$F000\ 2D00_H$ - $F000\ 2DFF_H$	256 Bytes
–	Reserved	$F000\ 2E00_H$ - $F000\ 3BFF_H$	–
DMA	DMA Controller	$F000\ 3C00_H$ - $F000\ 3DFF_H$	2 × 256 Bytes
–	Reserved	$F000\ 3E00_H$ - $F00F\ FFFF_H$	–
CAN[1)]	Controller Area Network Module	$F010\ 0000_H$ - $F010\ 0BFF_H$	12 × 256 Bytes

Table 3 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
–	Reserved	F010 0C00$_H$ - FFFE FEFF$_H$	–
CPU	Slave Interface Registers (CPS)	FFFE FF00$_H$ - FFFE FFFF$_H$	256 Bytes
	Reserved	FFFF 0000$_H$ - FFFF BFFF$_H$	–
	Memory Protection Registers	FFFF C000$_H$ - FFFF EFFF$_H$	12 Kbytes
	Reserved	FFFF F000$_H$ - FFFF FCFF$_H$	–
	Core Debug Registers (OCDS)	FFFF FD00$_H$ - FFFF FDFF$_H$	256 Bytes
	Core Special Function Registers (CSFRs)	FFFF FE00$_H$ - FFFF FEFF$_H$	256 Bytes
	General Purpose Registers (GPRs)	FFFF FF00$_H$ - FFFF FFFF$_H$	256 Bytes

1) Access to unused address regions within this peripheral unit don't generate a bus error.

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Memory Protection System

The TC1765 memory protection system specifies the addressable range and read/write permissions of memory segments available to the currently executing task. The memory protection system controls the position and range of addressable segments in memory. It also controls the kinds of read and write operations allowed within addressable memory segments. Any illegal memory access is detected by the memory protection hardware, which then invokes the appropriate Trap Service Routine (TSR) to handle the error. Thus, the memory protection system protects critical system functions against both software and hardware errors. The memory protection hardware can also generate signals to the Debug Unit to facilitate tracing illegal memory accesses.

There are two Memory Protection Register Sets in the TC1765, numbered 0 and 1, which specify memory protection ranges and permissions for code and data. The PSW.PRS bit field determines which of these is the set currently in use by the CPU. Because the TC1765 uses a Harvard-style memory architecture, each Memory Protection Register Set is broken down into a Data Protection Register Set and a Code Protection Register Set. Each Data Protection Register Set can specify up to four address ranges to receive particular protection modes. Each Code Protection Register Set can specify up to two address ranges to receive particular protection modes.

Each of the Data Protection Register Sets and Code Protection Register Sets determines the range and protection modes for a separate memory area. Each contains register pairs which determine the address range (the Data Segment Protection Registers and Code Segment Protection Registers) and one register (Data Protection Mode Register) which determines the memory access modes which apply to the specified range.

Preliminary

On-Chip FPI Bus

The FPI Bus interconnects the functional units of the TC1765, such as the CPU and on-chip peripheral components. The FPI Bus also interconnects the TC1765 to external components by way of the External Bus Controller Unit (EBU). The FPI Bus is designed to be quick to acquire by on-chip functional units, and quick to transfer data. The low setup overhead of the FPI Bus access protocol guarantees fast FPI Bus acquisition, which is required for time-critical applications. The FPI Bus is designed to sustain high transfer rates. For example, a peak transfer rate of up to 160 Mbyte/s can be achieved with a 40 MHz bus clock and 32-bit data bus. Multiple data transfers per bus arbitration cycle allow the FPI Bus to operate at close to its peak bandwidth.

Features:

- Supports multiple bus masters
- Supports demultiplexed address/data operation
- Address and data buses are 32 bits wide
- Data transfer types include 8-, 16-, and 32-bit sizes
- Single- and multiple-data transfers per bus acquisition cycle
- Designed to minimize EMI and power consumption

Preliminary

External Bus Unit

The External Bus Unit (EBU) of the TC1765 is the interface between external memories and peripheral units and the internal memories and peripheral units. The basic structure of the EBU is shown in **Figure 11**.

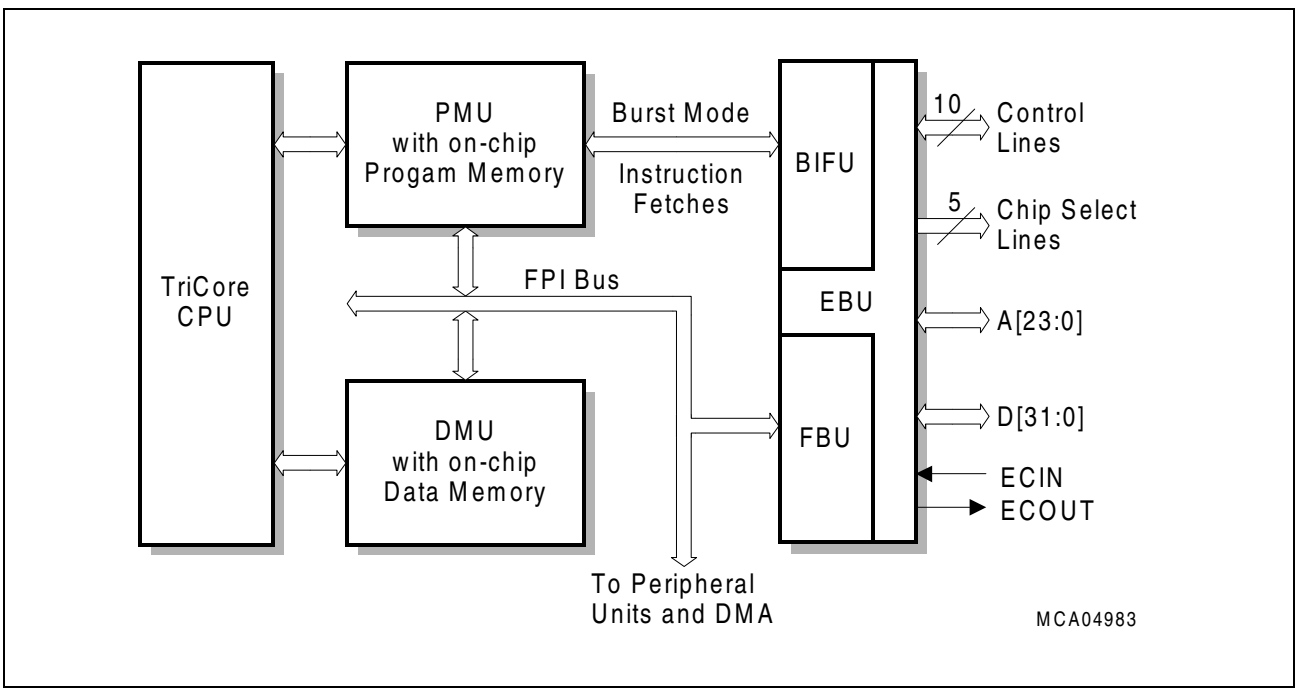

Figure 11 EBU Structure and Interfaces

The EBU consists of two parts and is used for the following two operations:

- FBU (FPI Bus Unit):
  - Communication with external memories or peripheral units via the FPI Bus
  - Non-burst instruction fetches
- BIFU (Burst Instruction Fetch Unit):
  - Instruction fetches from the PMU to external Burst Flash program memories with 16-bit and 32-bit data width

The EBU controls all transactions required for these two operations and in particular handles the arbitration between these two tasks.

The types of external devices/Bus modes controlled by the FBU are:

- INTEL style peripherals (separate $\overline{RD}$ and $\overline{WR}$ signals)
- MOTOROLA style peripherals ($\overline{OE}$ and R/$\overline{W}$)
- ROMs, EPROMs
- Static RAMs
- Peripherals with demultiplexed A/D bus
- Burst Mode Flash Memories
- 8-, 16- and 32-bit data bus width

Preliminary

DMA Controller

The Direct Memory Access (DMA) Controller executes DMA transactions from a source address location to a destination address location, without intervention of the CPU. One DMA transaction is controlled by one DMA channel.

Each of the two blocks in the DMA controller, block 0 and block 1 (see **Figure 12**), provides four DMA channels with sixteen DMA request inputs. The request assignment unit in each sub-block assigns one DMA request input to each DMA channel. The control unit includes a third request unit dedicated especially for request control through I/O pins. This unit connects two of eight request inputs with two request outputs which can be then wired externally of the DMA controller module to the request inputs of the two DMA controller blocks. Request assignment unit 2 evaluates pulses or levels by its edge detect and level select logic.

Features:

- 8 independent DMA channels (4 per DMA block)
  - 4 DMA selectable request inputs per DMA channel
  - Fixed priority of DMA channels within a DMA block
  - Software and hardware DMA request generation
- Support of FPI Bus to FPI Bus DMA transactions
- Individually programmable operation modes for each DMA channel
  - Single mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated
- Full 32-bit addressing capability of each DMA channel
  - 4 Gbyte address range
  - Source and destination transfer individually programmable in steps from 0 to 255 bytes
  - Support of circular buffer addressing mode
- Programmable data width of a DMA transaction: 8-bit, 16-bit, or 32-bit
- Register set for each DMA channel
  - Source and destination start address register
  - Source and destination end address register
  - Channel control and status register
  - Offset and transfer count register
- Bus bandwidth allocation
- Flexible interrupt generation

Figure 12 shows the TC1765 specific implementation details and interconnections of the DMA module. The DMA module is further supplied by a separate clock control, address decoding, interrupt control, port control logic.

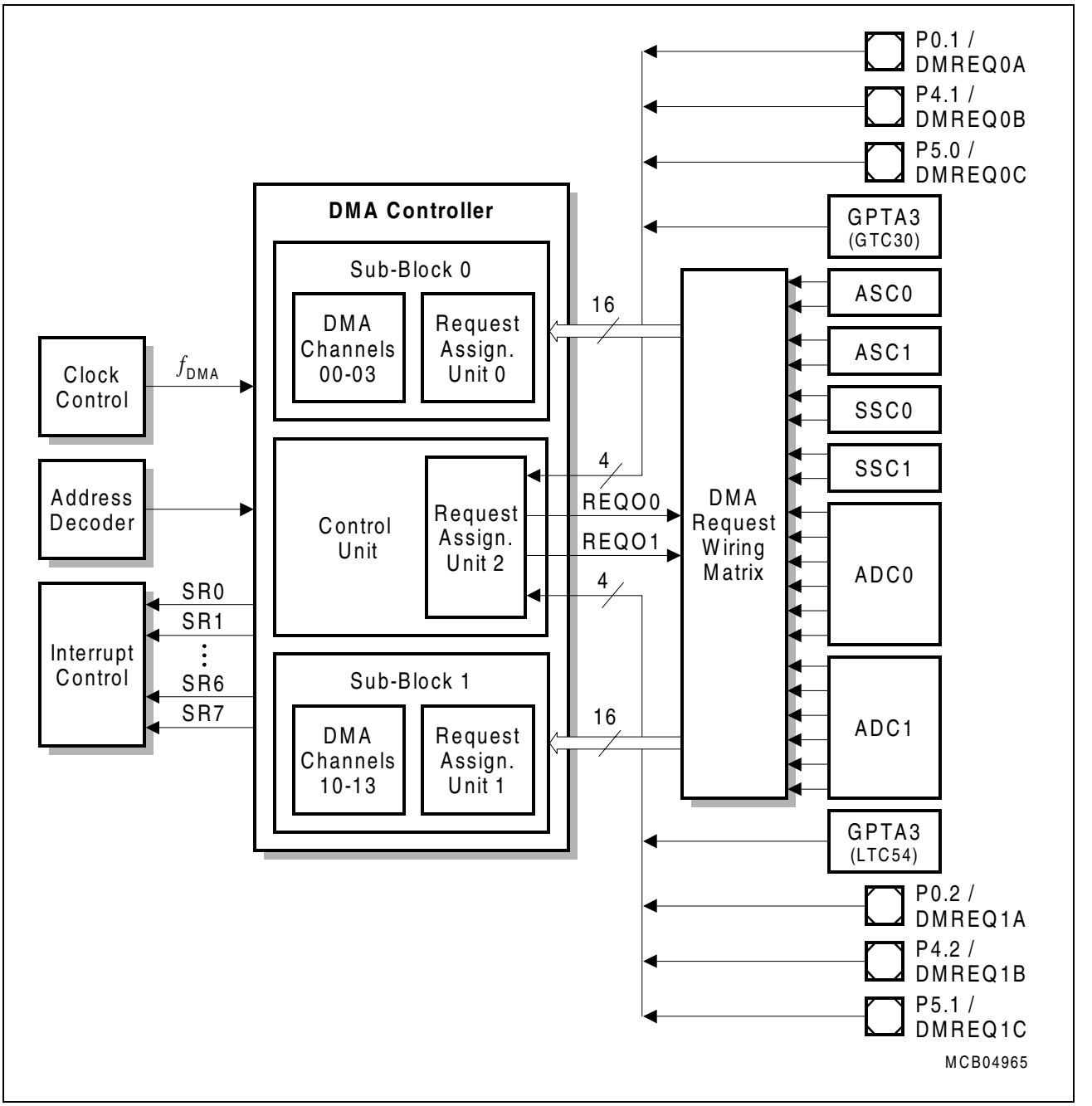

Figure 12 DMA Module Block Diagram with Interconnections

Preliminary

System Timer

The TC1765's System Timer (STM) is designed for global system timing applications requiring both high precision and long range. The STM has the following features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Driven by clock f_{STM} (identical to the system clock f_{SYS})
- Counting starts automatically after a reset operation (except a hardware reset)

The STM is an upward counter, running with the system clock frequency ($f_{STM} = f_{SYS}$). It is enabled per default after reset, and immediately starts counting up. Other than via reset, it is no possible to affect the contents of the timer during normal operation of the application, it can only be read, but not written to. Depending on the implementation of the clock control of the STM, the timer can optionally be disabled or suspended for power-saving and debugging purposes via a clock control register.

The maximum clock period is $2^{56} \times 1 / f_{STM}$. At f_{STM} = 40 MHz, for example, the STM counts 57.1 years before overflowing. Thus, it is capable of continuously timing the entire expected product life-time of a system without overflowing.

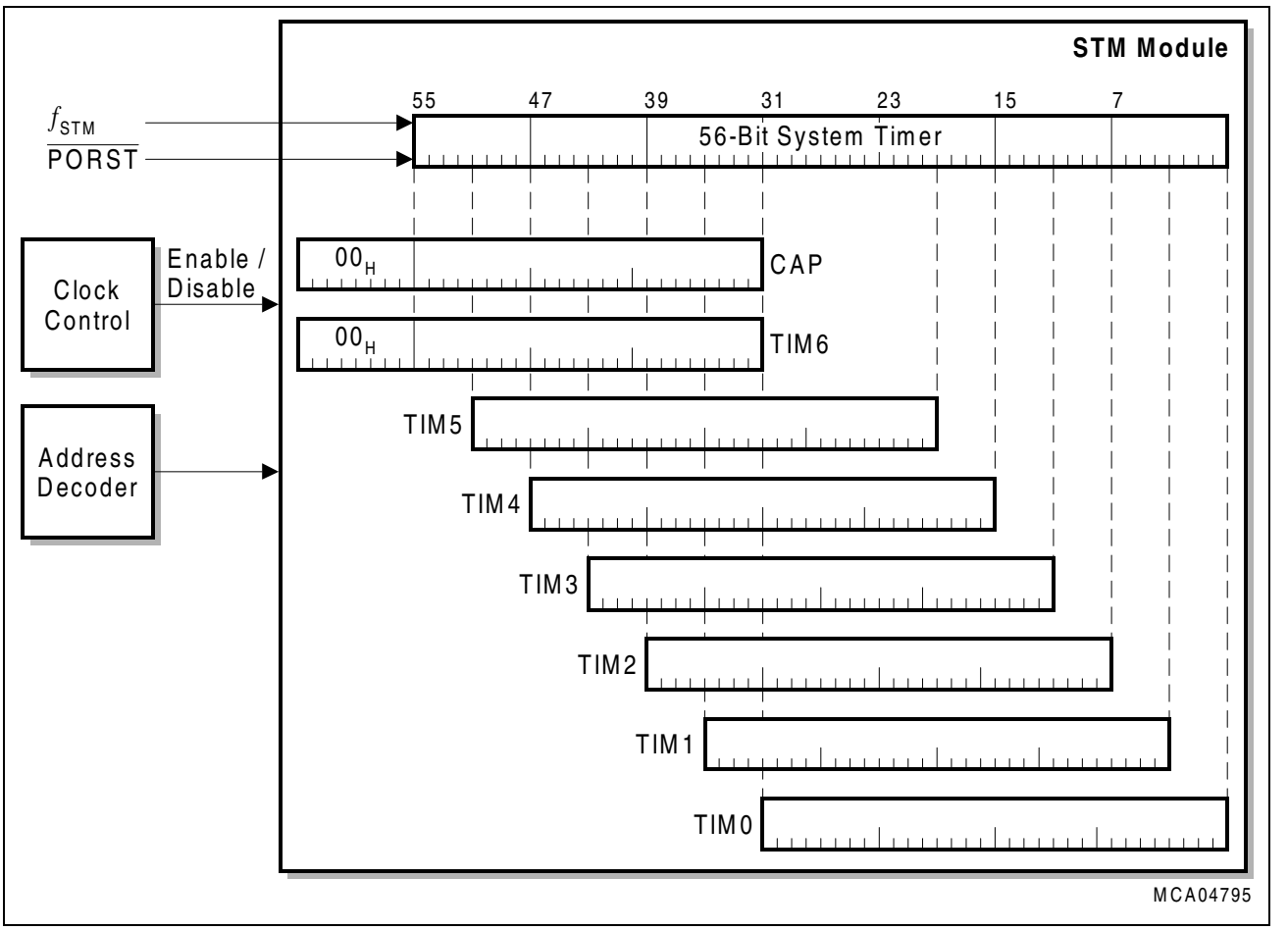

Figure 13 Block Diagram of the System Timer Module

Preliminary

Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1765 in a user-specified time period. When enabled, the WDT will cause the TC1765 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1765 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard “Watchdog” function, the WDT incorporates the EndInit feature and monitors its modifications. A system-wide line is connected to the ENDINIT bit implemented in a WDT control register, serving as an additional write-protection for critical registers (besides Supervisor Mode protection).

A further enhancement in the TC1765’s Watchdog Timer is its reset prewarning operation. Instead of immediately resetting the device on the detection of an error, as known from standard Watchdogs, the WDT first issues an Non-maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, an important aid in debugging.

Features:

- 16-bit Watchdog counter
- Selectable input frequency: $f_{SYS}/256$ or $f_{SYS}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated password access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT and limited.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation.
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation.
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled.
- Double Reset Detection: If a Watchdog induced reset occurs twice without a proper access to its control register in between, a severe system malfunction is assumed and the TC1765 is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed.

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- Important debugging support is provided through the reset prewarning operation by first issuing an NMI to the CPU before finally resetting the device after a certain period of time.

System Control Unit

The System Control Unit (SCU) of the TC1765 handles the system control tasks. All these system functions are tightly coupled, thus, they are conveniently handled by one unit, the SCU. The system tasks of the SCU are:

- Reset Control
  - Generation of all internal reset signals
  - Generation of external $\overline{\text{HDRST}}$ reset signal
- PLL Control
  - PLL_CLC Clock Control Register
- Power Management Control
  - Enabling of several power-down modes
  - Control of the PLL in power-down modes
- Watchdog Timer
- Trace Control and Trace Status indication
- Pull-up/pull-down I/O control
- Device Identification

Preliminary

Interrupt System

An interrupt request is serviced by the CPU. Interrupt requests are also called “Service Requests” because they are serviced by a “Service Provider”, the CPU.

Each peripheral unit in the TC1765 typically generates service requests. Additionally, the Bus Control Unit, the Debug Unit, the DMA controller, and even the CPU itself can generate service requests. Several peripheral units are able to generate in parallel to a service request DMA requests to the DMA Controller.

As shown in **Figure 14**, each TC1765 unit that can generate service requests is connected to one or multiple Service Request Nodes (SRN). Each SRN contains a Service Request Control Register mod_SRCx, where “mod” is the identifier of the service requesting unit and “x” an optional index. The Interrupt arbitration bus connects the SRNs with the Interrupt Control Unit, which handles interrupt arbitration among competing interrupt service requests.

Units which can generate service requests are:

- General Purpose Timer Unit (GPTU) with 8 SRNs
- General Purpose Timer Array (GPTA) with 54 SRNs
- Two High-Speed Synchronous Serial Interfaces (SSC0/SSC1) with 3 SRNs each
- Two Asynchronous/Synchronous Serial Interfaces (ASC0/ASC1) with 4 SRNs each
- TwinCAN controller with 8 SRNs
- Two Analog/Digital Converters (ADC0/ADC1) with 4 SRNs each
- Bus Control Unit (BCU) with 1 SRN
- DMA Controller Processor (DMA) with 8 SRNs
- Central Processing Unit (CPU) with 4 SRNs
- Debug Unit (OCDS) with 1 SRN
- Central Processing Unit (CPU) with 4 SRNs (software activated)

External interrupt inputs in TC1765 are available using the input pins connected to the General Purpose Timer Unit (GPTU). Each of the seven GPTU I/O pins can be used as an external interrupt input, using the Service Request Nodes of the GPTU module. Additionally, such an external interrupt input can also trigger a timer function.

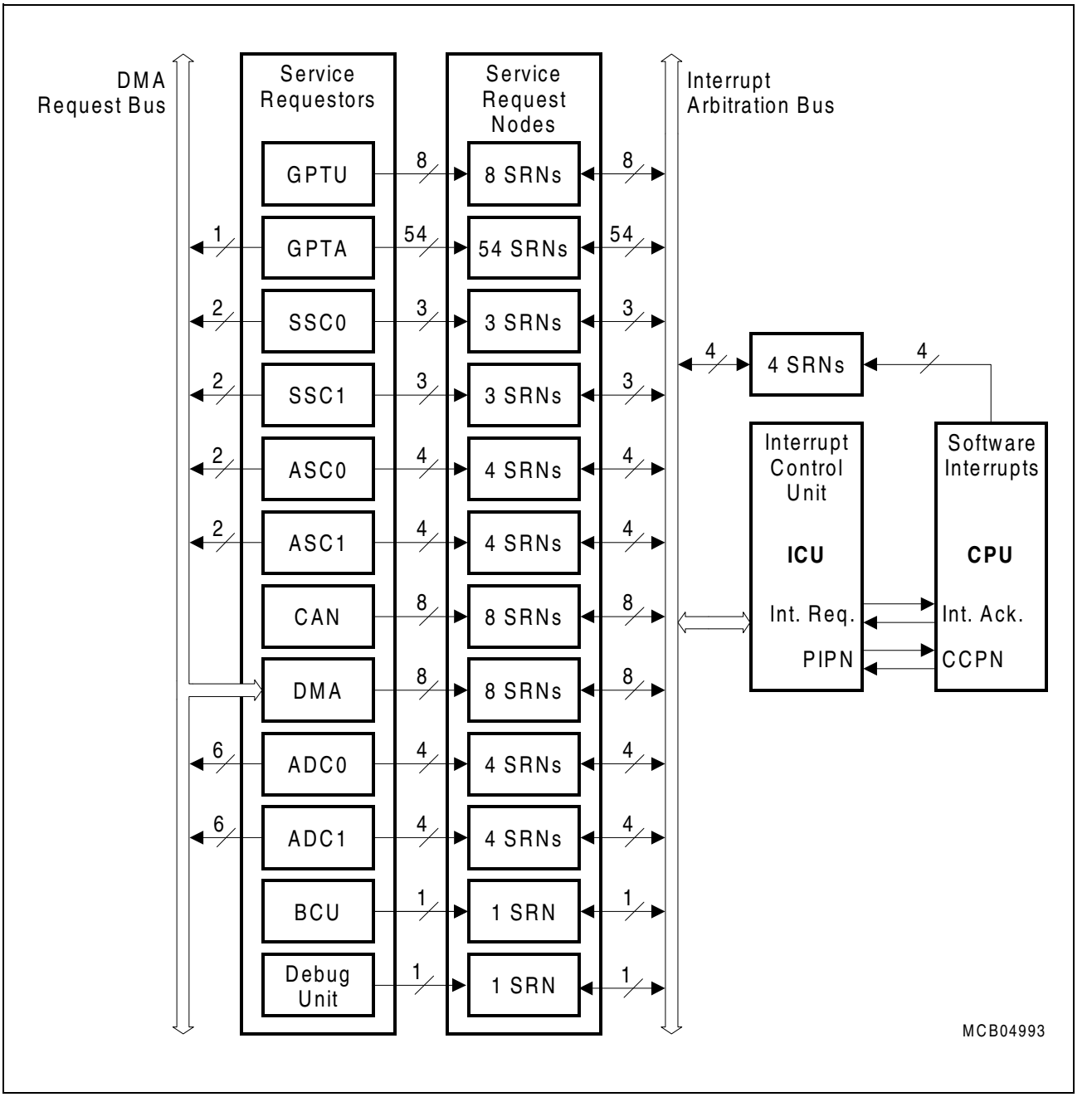

Figure 14 Block Diagram of the TC1765 Interrupt System

Preliminary

Boot Options

The TC1765 booting schemes provides a number of different boot options for the start of code execution. **Table 4** shows the boot options available in the TC1765.

Table 4 TC1765 Boot Selections

$\overline{\text{OCDSE}}$	$\overline{\text{BRKIN}}$	CFG[2:0]	Type of Boot	Boot Source	PC Start Value
1	1	000_B	Start from Boot ROM Entry Point 1	Boot ROM	BFFF FFFC$_H$
		001_B	Start from Boot ROM Entry Point 2		
		010_B	Start from Boot ROM Entry Point 3		
		011_B	Start from Boot ROM Entry Point 4		
		100_B	External memory as master directly PMU - EBU	External Memory	A000 0000$_H$
		101_B	External memory via PMU - FPI Bus - EBU		
		110_B	Reserved; don't use these combinations.		
		111_B			
0	1	100_B or 101_B	Go to halt with EBU enabled as master	–	–
		all other combina-tions	Go to halt with EBU disabled		
0	0	–	Go to external emulator space	–	BE00 0000$_H$
1	0	–	Tri-state chip (deep sleep)	–	–

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Power Management System

The TC1765 power management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application.

There are four power management modes:

- Run Mode
- Idle Mode
- Sleep Mode
- Deep Sleep Mode

Table 5 describes the features of the power management modes.

Table 5 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the $\overline{\text{NMI}}$ pin, or any enabled interrupt event will return the system to Run Mode.
Sleep	The system clock continues to be distributed only to those peripherals programmed to operate in Sleep Mode. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the $\overline{\text{NMI}}$ pin, or a reset event will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.
Deep Sleep	The system clock is shut off; only an external signal will restart the system. Entering this state requires an orderly shut-down controlled by the Power Management State Machine (PMSM).

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On-Chip Debug Support

The On-Chip Debug Support (OCDS) of the TC1765 consists of four building blocks:

- OCDS module in the TriCore CPU
  - On-chip breakpoint hardware
  - Support of an external break signal
- Trace module
  - Outputs 16 bits each f_{SYS} system clock cycle at TP[15:0] with pipeline status information, PC bus information, and breakpoint qualification information
- DMA Controller Trace
  - Indication of address counter updates
- Debugger Interface Cerberus
  - Provided for debug purposes of emulation tool vendors
  - Accessible through a JTAG standard interface with dedicated JTAG port pins

Figure 15 shows a basic block diagram of the building blocks.

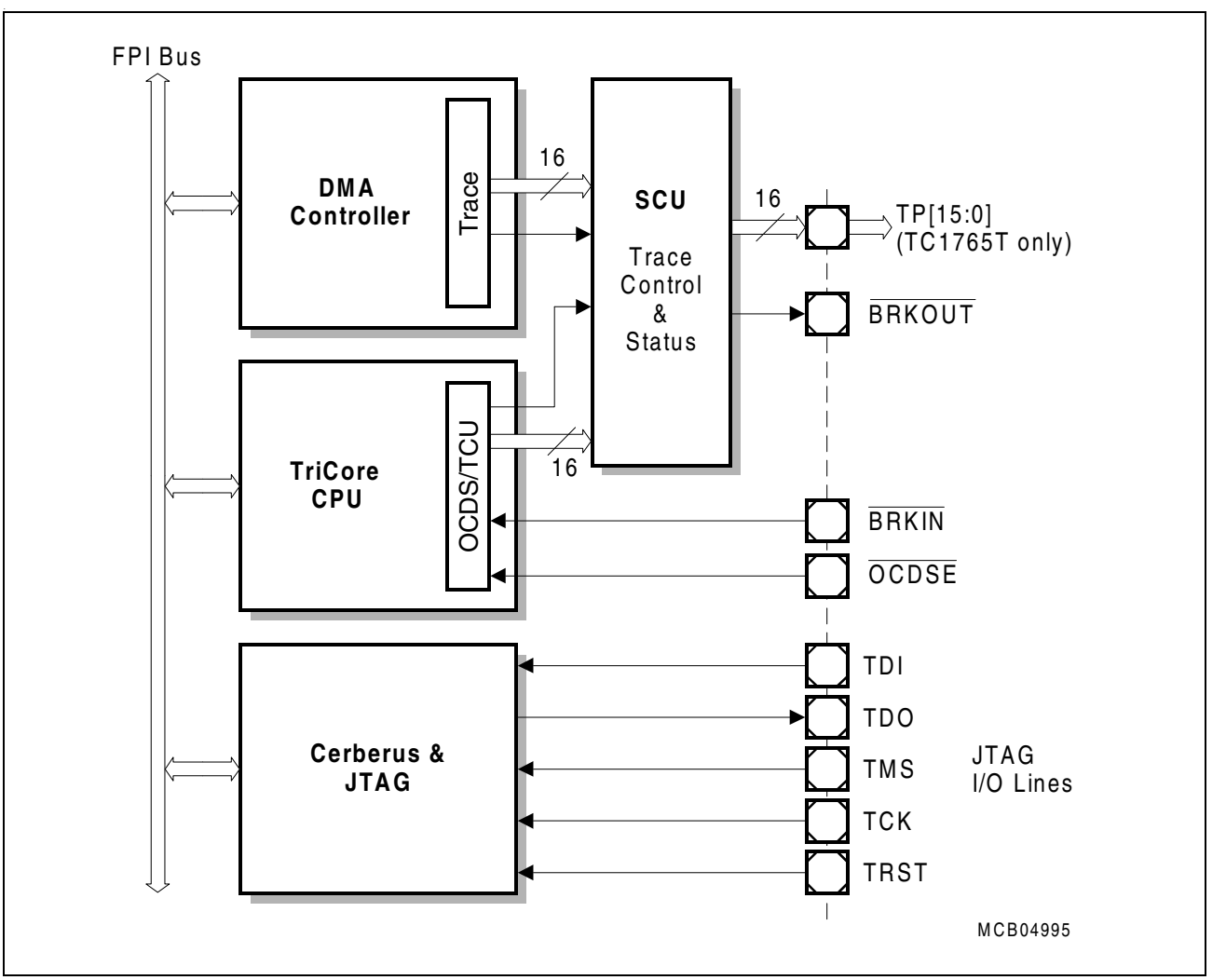

Figure 15 OCDS Basic Block Diagram

Preliminary

Clock Generation Unit

The Clock Generation Unit (CGU) in the TC1765, shown in **Figure 16**, consists of an oscillator circuit and a Phase-Locked Loop (PLL). The PLL can convert a low-frequency external clock signal to a high-speed internal clock for maximum performance. The PLL also has fail-safe logic that detects degenerate external clock behavior such as abnormal frequency deviations or a total loss of the external clock. It can execute emergency actions if it looses its lock on the external clock.

In general, the CGU is controlled through the System Control Unit (SCU) module of the TC1765.

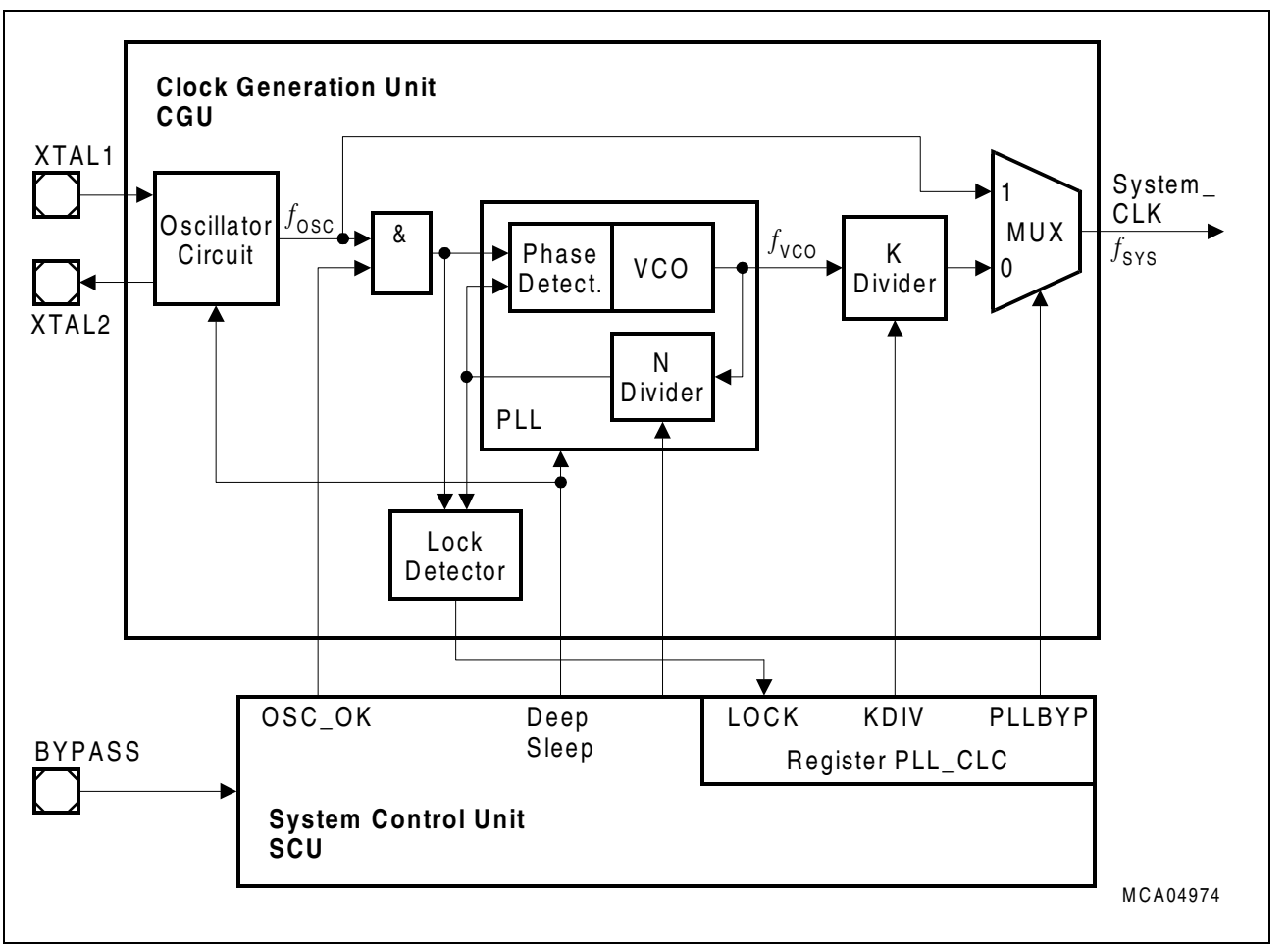

Figure 16 Clock Generation Unit Block Diagram

Preliminary

PLL Operation

The f_{VCO} clock of the PLL has a frequency which is a multiple of the externally applied clock f_{OSC}. The factor for this is controlled through the fix divider value N (N = 10) applied to the divider in the feedback path. The K-Divider is defined by bit field KDIV. **Table 6** lists the possible values for KDIV and the resulting division factor.

The VCO output frequency and the resulting system clock is determined by:

$$f_{VCO} = 10 \times f_{OSC} \qquad f_{SYS} = f_{VCO} / K = \frac{10}{K} \times f_{OSC}$$

Table 6 Output Frequencies f_{SYS} Derived from Various Output Factors

K-Factor		f_{SYS}			Duty Cycle [%]
Selected Factor	KDIV	f_{VCO} = 150 MHz	f_{VCO} = 160 MHz	f_{VCO} = 200 MHz	
2	000_B	75[1)]	80[1)]	100[1)]	50
4	010_B	37.5	40	50[1)]	50
5[2)]	011_B	30	32	40	40
6	100_B	24.5	26.67	33.33	50
8	101_B	18.75	20	25	50
9[2)]	110_B	16.67	17.78	22.22	44
10	111_B	15	16	20	50
16	001_B	9.38	10	12.5	50

1) These combinations cannot be used because the maximum system clock of 40 MHz is exceeded.

2) These odd K-Factors should not be used (not tested because of the unsymmetrical duty cycle).

Recommended Oscillator Circuits

The oscillator circuit, designed to work with both, an external crystal oscillator or an external stable clock source, basically consists of an inverting amplifier with XTAL1 as input and XTAL2 as output. When using a crystal, a proper external oscillator circuitry must be used, connected to both pins, XTAL1 and XTAL2. The on-chip oscillator frequency can be within the range of 4 MHz to 16 MHz. When using an external clock signal it must be connected to XTAL1. XTAL2 is left open (unconnected). For direct drive operation without PLL, the frequency of an external clock must not exceed 40 MHz.

Figure 17 shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode.

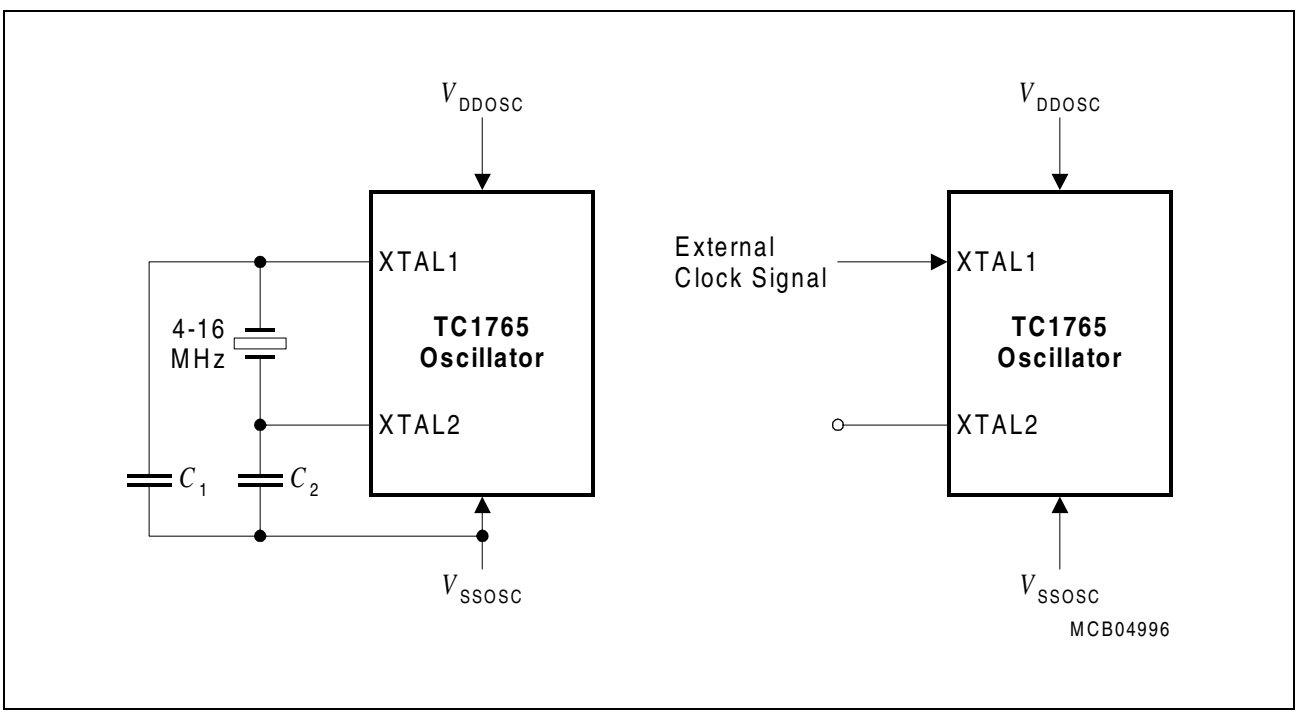

Figure 17 Oscillator Circuitries

For the oscillator of the TC1765 the following external passive components are recommended:

- Crystal: max. 16 MHz
- C_1, C_2: 10 pF

A block capacitor between V_{DDOSC} and V_{SSOSC} is recommended, too.

- C_1, C_2: 12 pF

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

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Power Supply

Figure 18 shows the TC1765's power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling. Also the operation margin is improved in sensitive modules like the A/D converter by noise reduction.

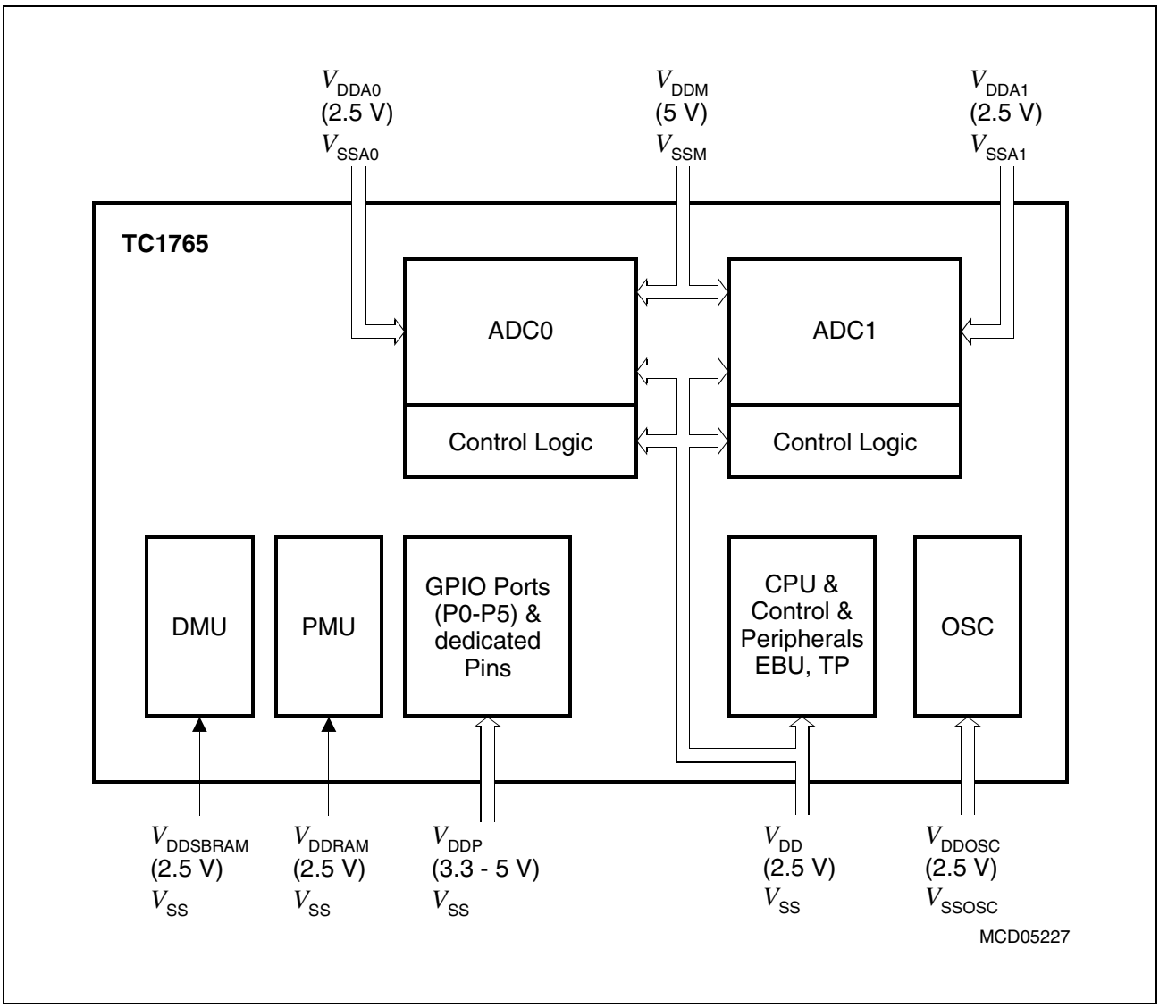

Figure 18 TC1765 Power Supply Concept

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Ports Power Supply

The TC1765's port power supply concept is shown in **Figure 19**. The External Bus Unit (EBU) I/O lines are in the core and EBU V_{DD} power supply group for 2.5 V nominal operating voltage. The general purpose input/outputs (GPIOs) provide 3.3 to 5 V nominal voltage input/output acceptance and drive characteristics.

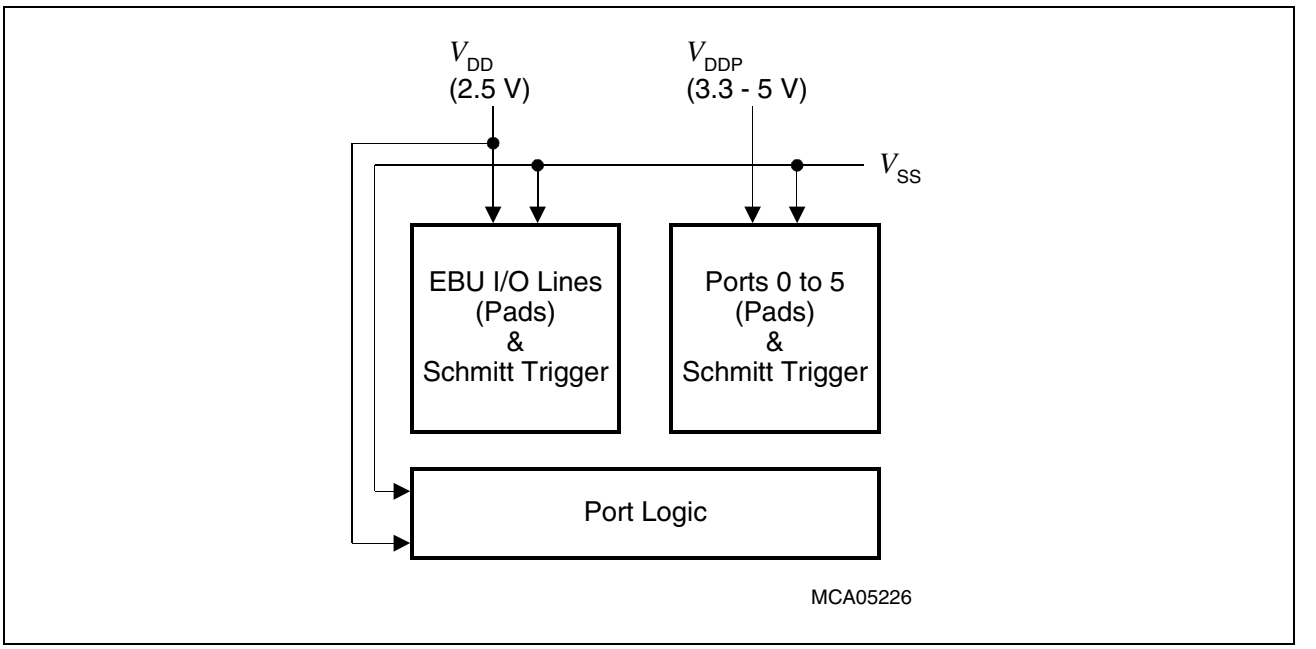


Figure 19 Ports Power Supply Concept

Power-up Sequence

During Power-up the reset pin $\overline{\text{PORST}}$ has to be held active until both power supply voltages have reached at least their minimum values.

During the Power-up time (rising of the supply voltages from 0 to their regular operating values) it has to be ensured, that the difference between V_{DDP} and V_{DD} never drops below -0.5 V.

Power Loss

If V_{DDP} is dropping below V_{DD}, external circuitry in the power supply has to ensure, that V_{DD} is also limited to the same level.

If V_{DDI} is dropping below the operating range, V_{DDP} may stay active.

Powering Down

During powering down (falling of the supply voltages from their regular operating values to zero), it has to be ensured, that the difference between V_{DDP} and V_{DD} never drops below -0.5 V.

Preliminary

Identification Register Values

Table 7 TC1765 Identification Registers

Short Name	Address	Value
PMU_ID	C7FF FF08$_H$	0006 C003$_H$
DMU_ID	D7FF FF08$_H$	0007 C003$_H$
SCU_ID	F000 0008$_H$	0003 C003$_H$
MANID	F000 0070$_H$	0000 1820$_H$
CHIPID	F000 0074$_H$	0000 8601$_H$
RTID	F000 0078$_H$	0000 0000$_H$
BCU_ID	F000 0208$_H$	0000 6A05$_H$
STM_ID	F000 0308$_H$	0000 C002$_H$
JPD_ID	F000 0408$_H$	0000 6301$_H$
EBU_ID	F000 0508$_H$	0005 C004$_H$
GPTU_ID	F000 0708$_H$	0001 C002$_H$
ASC0_ID	F000 0808$_H$	0000 4401$_H$
ASC1_ID	F000 0908$_H$	0000 4401$_H$
SSC0_ID	F000 0A08$_H$	0000 4525$_H$
SSC1_ID	F000 0B08$_H$	0000 4525$_H$
GPTA_ID	F000 1808$_H$	0002 C002$_H$
ADC0_ID	F000 2208$_H$	0000 3103$_H$
DMA_ID	F000 3F08$_H$	0018 C001$_H$
CAN_ID	F010 0008$_H$	0000 4110$_H$
CPU_ID	FFFE FF08$_H$	0000 0202$_H$

Preliminary

Parameter Interpretation

The parameters listed on the following pages partly represent the characteristics of the TC1765 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):

The logic of the TC1765 will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):

The external system must provide signals with the respective timing characteristics to the TC1765.

Pin Classes

The TC1765 has three classes of digital I/O pins:

- **Class A** pins, which are 3.0 to 5.25 V voltage pins
- **Class B** pins, which are 2.5 V nominal voltage pins (input tolerant for 3.3 V)
- **Class C** pins, which are 2.5 V nominal voltage pins only

Table 8 shows the assignments of all digital I/O pins to pin classes and to V_{DD} power supply pins.

Table 8 Assignments of Digital Pins to Pin Classes and Power Supply Pins

Pins	Pin Classes	Power Supply	
Port 0 to Port 5, BYPASS, $\overline{\text{HDRST}}$	Class A (3.0 to 5.25 V)	V_{DDP}	V_{SS}
D[31:0], A[23:0], $\overline{\text{CS}}$[3:0], $\overline{\text{CSEMU}}$/$\overline{\text{CSOVL}}$, $\overline{\text{BC}}$[3:0], $\overline{\text{RD}}$, RD/$\overline{\text{WR}}$, ADV, $\overline{\text{WAIT}}$/$\overline{\text{IND}}$, $\overline{\text{BAA}}$, $\overline{\text{CODE}}$, $\overline{\text{TRST}}$, TCK, TDI, TDO, TMS, $\overline{\text{ODCSE}}$, $\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$, $\overline{\text{NMI}}$, $\overline{\text{PORST}}$, ECOUT, ECIN, CPUCLK, $\overline{\text{TESTMODE}}$, TP[15:0]	Class B (nominal 2.5 V)	V_{DD}	
XTAL1, XTAL2	Class C (nominal 2.5 V)	V_{DDOSC}	V_{SSOSC}
No pins assigned	(nominal 2.5 V)	V_{DDRAM} $V_{DDSBRAM}$	V_{SS}

Preliminary

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_A	-65	150	°C	–
Junction temperature	T_J	–	150	°C	under bias
Voltage on V_{DDP} with respect to V_{SS}	V_{DD}	-0.5	6.2	V	see **Table 8**
Voltage on V_{DD}, V_{DDOSC}, V_{DDRAM} and $V_{DDSBRAM}$ with respect to V_{SS}	V_{DD}	-0.5	3.25	V	–
Voltage on any Class A input pin with respect to V_{SS}	V_{IN}	-0.5	V_{DD} + 0.5	V	–
Voltage on any Class B input pin with respect to V_{SS}	V_{IN}	-0.5	3.7	V	–
Voltage on any Class C input pin with respect to V_{SS}	V_{IN}	-0.5	V_{DDOSC} + 0.5	V	–
Input current on any pin during overload condition	I_{IN}	-10	10	mA	–
Absolute sum of all input currents during overload condition	ΣI_{IN}	–	|100|	mA	–

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Preliminary

Package Parameters (P-LBGA-260)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Power dissipation	P_{DISS}	–	0.9	W	–
Thermal resistance	R_{THA}	–	24.8	K/W	Chip to ambient

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1765. All parameters specified in the following table refer to these operating conditions, unless otherwise noticed.

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage[1]	V_{DDP}	3.0	5.25[2]	V	Class A pins
	V_{DD} V_{DDOSC} V_{DDRAM}	2.3	2.75[3]	V	Class B and Class C pins[4]
	$V_{DDSBRAM}$	2.25	2.75	V	4)5)
Digital ground voltage	V_{SS}	0		V	–
Ambient temperature under bias	T_A	-40	+125	°C	–
Analog supply voltages	V_{DDA}	2.25	2.75	V	–
	V_{DDM}	4.5	5.25	V	–
Analog reference voltage	V_{AREF}	4	V_{DDM} + 0.05	V	6)
Analog ground voltage	V_{AGND}	V_{SSA} - 0.05	V_{SSA} + 0.05	V	7)
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	–
CPU clock	f_{SYS}	–	40	MHz	–
Overload current	I_{OV}	-10	10	mA	8)9)10)
Short circuit current	I_{SC}	-10	10	mA	5)6)11)
Absolute sum of overload + short circuit currents	$\Sigma\|I_{OV}\| + \|I_{SC}\|$	–	|50|	mA	9)
External load capacitance	C_L	–	50	pF	–

1) Digital supply voltages applied to the TC1765 must be static regulated voltages which allow a typical voltage swing of ±10%.

2) Voltage overshoot to 6.5 V is permissible, provided that the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 hour.

3) Voltage overshoot to 4 V is permissible, provided that the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 hour.

4) In order to minimize the danger of latch-up conditions, these 2.5 V V_{DD} power supply pins should be kept at the same voltage level during normal operating mode. This condition is typically achieved by generating the 2.5 V power supplies from a single voltage source. The condition is also valid in normal operating mode if a separate stand-by power supply $V_{DDSBRAM}$ is used.

5) The minimum voltage at pin $V_{DDSBRAM}$ during TC1765 power down mode is 1.8 V in order to keep the contents of SBRAM valid. The core power supply V_{DD} must be below the standby power supply $V_{DD} < V_{DDSBRAM} + 0.3$ V.

6) The value of V_{AREF} is permitted to be within the range of V_{SSA} - 0.05 V < V_{AREF} < V_{DDM} + 0.05 V. The value specified for the total unadjusted error (TUE) is not guaranteed while the V_{AREF} is out of the specified range.

7) The value of V_{AGND} is permitted to be within the range of V_{SSA} - 0.05 V < V_{AGND} < V_{DDM} + 0.05 V. The value specified for the total unadjusted error (TUE) is not guaranteed while the V_{AGND} is out of the specified range.

8) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$ + 0.5 V or $V_{OV} < V_{SS}$ - 0.5 V). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

9) Not 100% tested, guaranteed by design and characterization.

10) Applicable for analog inputs.

11) Applicable for digital inputs.

Preliminary

DC Characteristics

Input/Output DC-Characteristics

V_{SS} = 0 V; T_A = -40 °C to +125 °C;

Parameter[1]	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Class A Pins (V_{DDP} = 3.0 to 5.25 V)						
Output low voltage[2]	V_{OL}	CC	–	0.45	V	I_{OL} = 2.4 mA[3] I_{OL} = 600 µA[4] V_{DDP} = 4.5 to 5.25 V
				$0.2 \times V_{DDP}$	V	I_{OL} = 2.4 mA I_{OL} = 600 µA[4] V_{DDP} = 3.0 to 4.49 V
Output high voltage[2]	V_{OH}	CC	$0.7 \times V_{DDP}$	–	V	I_{OH} = -2.4 mA I_{OH} = -600 µA[4] V_{DDP} = 4.5 to 5.25 V
					V	I_{OH} = -2.4 mA I_{OH} = -600 µA[4] V_{DDP} = 3.0 to 4.49 V
Input low voltage[5]	V_{IL}	SR	-0.5	0.8	V	V_{DDP} = 4.5 to 5.25 V (TTL)
				$0.45 \times V_{DDP}$	V	V_{DDP} = 4.5 to 5.25 V (CMOS)
				$0.2 \times V_{DDP}$	V	V_{DDP} = 3.0 to 4.49 V (CMOS)
Input high voltage[5]	V_{IH}	SR	2.0	V_{DDP} + 0.5	V	V_{DDP} = 4.5 to 5.25 V (TTL)
			$0.73 \times V_{DDP}$		V	V_{DDP} = 3.0 to 5.25 V (CMOS)
Pull-up current[6][7]	$\lvert I_{PUH} \rvert$	CC	–	10	µA	$V_{OUT} = V_{DDP}$ - 0.02 V
	$\lvert I_{PUL} \rvert$	CC	120	600	µA	$V_{OUT} = 0.5 \times V_{DDP}$
Pull-down current[8][7]	$\lvert I_{PDL} \rvert$	CC	–	10	µA	V_{OUT} = 0.02 V
	$\lvert I_{PDH} \rvert$	CC	120	700	µA	$V_{OUT} = 0.5 \times V_{DDP}$

Preliminary

Input/Output DC-Characteristics (cont'd)

V_{SS} = 0 V; T_A = -40 °C to +125 °C;

Parameter[1)]	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Class B Pins (V_{DDP05} = 2.30 to 2.75 V)						
Output low voltage	V_{OL}	CC	–	$0.2 \times V_{DD}$	V	I_{OL} = 2.4 mA
				0.45	V	I_{OL} = 600 µA
Output high voltage	V_{OH}	CC	$0.7 \times V_{DD}$	–	V	I_{OH} = -2.4 mA
			$0.9 \times V_{DD}$	–	V	I_{OH} = -600 µA
Input high voltage	V_{IH}	SR	$0.7 \times V_{DD}$	3.7	V	–
Input low voltage	V_{IL}	SR	-0.5	$0.2 \times V_{DD}$	V	–
Pull-up current[6)7)]	$\lvert I_{PUH} \rvert$	CC	–	10	µA	$V_{OUT} = V_{DD}$ - 0.02 V
	$\lvert I_{PUL} \rvert$	CC	50	250	µA	$V_{OUT} = 0.5 \times V_{DD}$
Pull-down current[8)7)]	$\lvert I_{PDL} \rvert$	CC	–	10	µA	V_{OUT} = 0.02 V
	$\lvert I_{PDH} \rvert$	CC	40	300	µA	$V_{OUT} = 0.5 \times V_{DD}$
Class A and B Pins						
Input Hysteresis	HYS	CC	$0.030 \times V_{DDx}$[9)]	–	V	CMOS only[10)] V_{DDx} limits see[11)]
Input leakage current (Digital I/O)	I_{OZ2}	CC	–	±500	nA	0 V < V_{IN} < V_{DDx}[9)]
Peak short-circuit current Peak back-drive current (per digital pin) Peak time & period time[12)13)]	$I_{SCBDpeak}$	SR	–	±20	mA	[14)10)]
Constant short-circuit current Constant back-drive current (per digital pin)	$I_{SCBDcons}$	SR	–	±10	mA	[14)10)]

Preliminary

Input/Output DC-Characteristics (cont'd)

V_{SS} = 0 V; T_A = -40 °C to +125 °C;

Parameter[1)]	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Pin capacitance[10)] (Digital I/O)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C

Class C Pins (V_{DDOSC} = 2.30 to 2.75 V), see Page 68

1) All Class A pins of the TC1765 are equipped with Low-Noise output drivers, which significantly improve the device's EMI performance. These Low-Noise drivers deliver their maximum current only until the respective target output level is reached. After that the output current is reduced. This results in an increased impedance of the driver, which attenuates electrical noise from the connected PCB tracks. The current, which is specified in column "Test Conditions", is delivered in any case.

2) This specification is not valid for outputs of GPIO lines, which are switched to open drain mode. In open drain mode the output will float and the voltage results from the external circuitry.

3) Output drivers in high current mode.

4) Condition for output driver in dynamic current mode & low current mode – guaranteed by design characterization.

5) Input characteristics can be switched between TTL and CMOS via register Px_PICON except for dedicated pins which have CMOS input characteristics.

6) The maximum current can be drawn while the respective signal line remains inactive.

7) The two pull-up/pull-down current test conditions for V_{OUT} cover the curves as shown in Figure 20 and Figure 21. All pull-up/pull-down currents are given as absolute values.

8) The minimum current must be drawn in order to drive the respective signal line active.

9) In case of Class B pins $V_{DDx} = V_{DD}$. In case of Class A pins $V_{DDx} = V_{DDP}$.

10) Guaranteed by design characterization.

11) The test condition for Class A pins is: V_{DDP} = 4.5 to 5.25 V; for Class B pins: V_{DD} = 2.3 to 2.75 V;

12) The max. peak-short-circuit current resp. max. peak-back-drive current is limited by max. 20 mA and the peak period equivalent of 10 mA constant-short-circuit current resp. 10 mA constant-back-drive current. The integral of $I_{SCBDpeak}$ over the peak period is thus limited to 10 mA (provided: $I_{SCBDpeak} \leq 20$ mA).

13) To be defined for Class B pads.

14) Short-circuit or back-drive conditions during operation occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{SCBD} > V_{DDP}$ **+ 0.5 V or** $V_{SCBD} < V_{SS}$ **- 0.5 V**) or a short circuit condition occurs on the respective pin. The absolute sum of input I_{SCBD} and I_{OV} currents on all port pins must not exceed **100 mA** at any time. The supply voltage (V_{DDP} and V_{SS}) must remain within the specified limits. Under short-circuit conditions the corresponding pin is not ready for use. In case of Class B pins $V_{DDx} = V_{DD}$. In case of Class A pins $V_{DDx} = V_{DDP}$.

Preliminary

Pull-Up/Pull-Down Characteristics

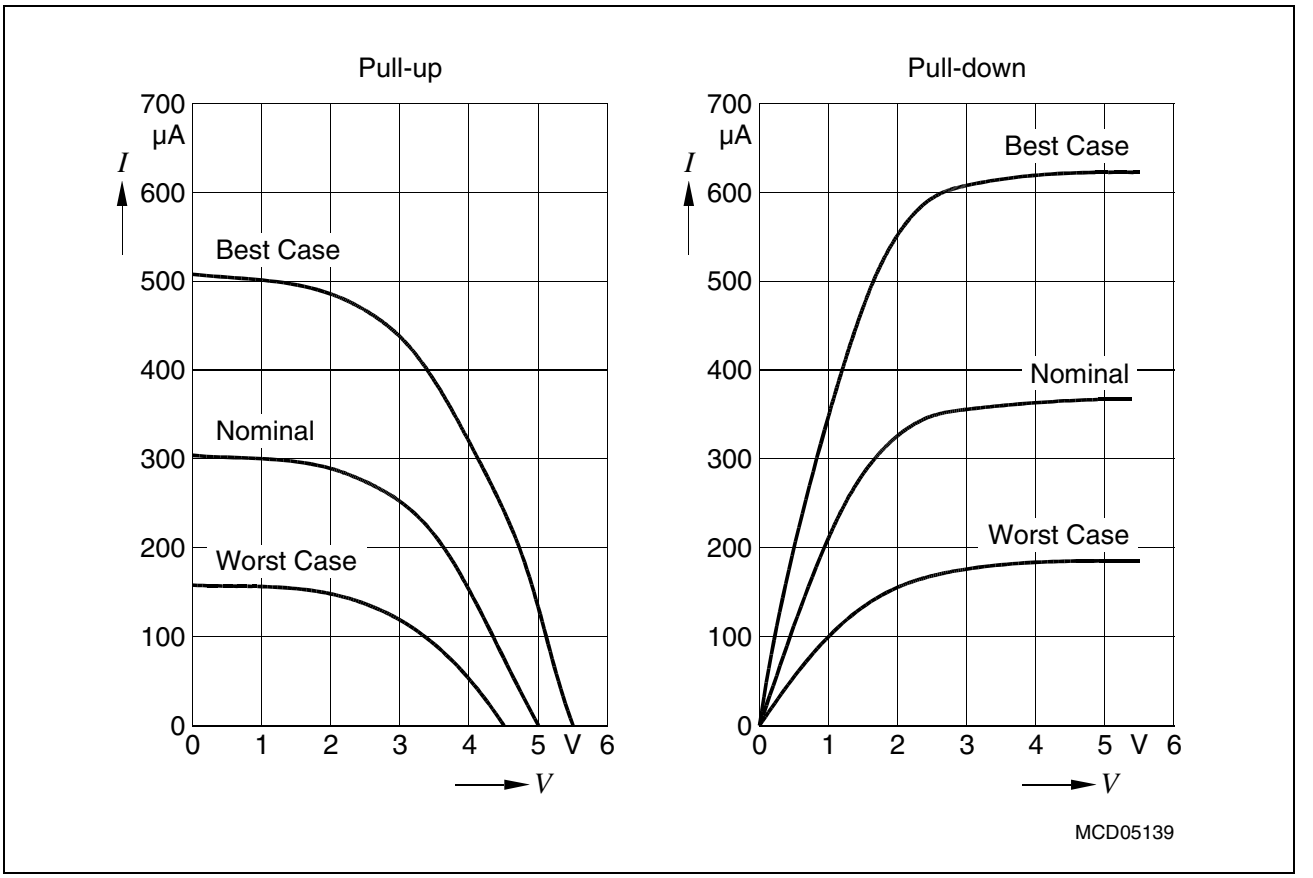


Figure 20 Pull-Up/Pull-Down Characteristics of Class A Pins

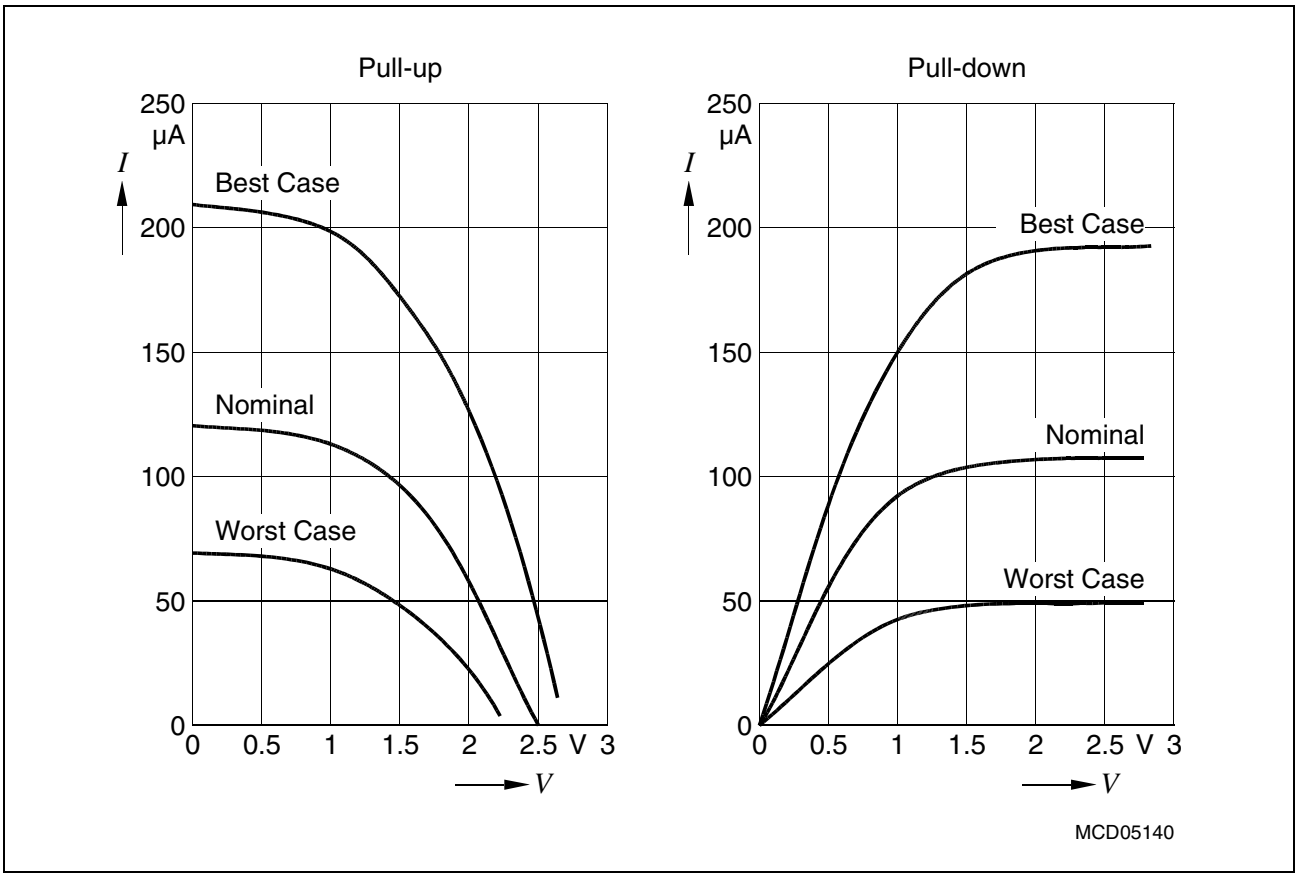


Figure 21 Pull-Up/Pull-Down Characteristics of Class B Pins

*Note: The pull-up/pull-down characteristics as shown in **Figure 20** and **Figure 21** are guaranteed by design characterization.*

Preliminary

AD Converter Characteristics

V_{SS} = 0 V; T_A = -40 °C to +125 °C;

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Analog supply voltages	V_{DDAx}	SR	2.25	2.5	2.75	V	1)
	V_{DDM}	SR	4.5	5	5.25	V	–
Analog ground voltage	V_{SSAx}	SR	-0.1	–	0.1	V	1)
Analog reference voltage	V_{AREFx}	SR	4	–	V_{DDM} + 0.05	V	1)2)
Analog reference ground	V_{AGNDx}	SR	V_{SSAx} - 0.05	–	V_{SSAx} + 0.05	V	1)3)
Analog input voltage range	V_{AIN}	SR	V_{AGNDx}	–	V_{AREFx}	V	1)
Internal ADC clock	f_{ANA}		0.5	–	5	MHz	–
Power-up calibration time	t_{PUC}	CC	–	–	3328 × (3 + CON.CPS) × t_{BC}	µs	–
Sample time	t_S	CC	(3 + CON.CPS) × (CHCONn.STC + 2) × t_{BC}			µs	4)
			6 × t_{BC}	–	–	µs	
Conversion time	t_C	CC	t_S + (30 + CON.CPS × 4) × t_{BC} + 2 × t_{DIV}			µs	for 8-bit conv.4)
			t_S + (36 + CON.CPS × 4) × t_{BC} + 2 × t_{DIV}			µs	for 10-bit conv.4)
			t_s + (42 + CON.CPS × 4) × t_{BC} + 2 × t_{DIV}			µs	for 12-bit conv.4)
Total unadjusted error	TUE5)	CC	–	–	±1	LSB	for 8-bit conv.
			–	–	±2	LSB	for 10-bit conv.
			–	–	±6	LSB	for 12-bit conv.
Overload current6)	I_{AOV1}7)	CC	-2	–	+5	mA	–
			-2		0	mA	$k_A = 1.0 \times 10^{-3}$
			0		+5	mA	$k_A = 1.0 \times 10^{-4}$
	I_{AOV2}8)	CC	-4	–	+10	mA	–
			-4		0	mA	$k_A = 1.0 \times 10^{-3}$
			0		+10	mA	$k_A = 1.0 \times 10^{-4}$
Overload coupling factor 9)	k_A	CC	–	–	1.0×10^{-3}	–	see I_{AOV1} and I_{AOV2}
					1.0×10^{-4}	–	

Preliminary

AD Converter Characteristics (cont'd)

V_{SS} = 0 V; T_A = -40 °C to +125 °C;

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Input leakage current at analog inputs	I_{OZ1}	CC	–	–	±200	nA	0 V< V_{IN} < V_{DDA} [1]
Input leakage current at V_{AGND} and V_{AREF}	I_{OZ2}	CC	–	–	±500	nA	0 V< V_{IN} < V_{DDA} [1]
Switched cap. at positive reference voltage input	C_{AREFSW}	CC	–	15	20	pF	[10]
Switched cap. at negative reference voltage input	C_{AGNDSW}	CC	–	15	20	pF	[10]
Total capacitance at analog voltage input	C_{AINTOT}	CC	–	12	15	pF	–
Switched cap. at analog voltage input	C_{AINSW}	CC	–	–	10	pF	[11]
ON resistance of the transmission gates in the analog voltage path	R_{AIN}	CC	–	–	0.7	kΩ	–

1) Suffix x = 0 refers to ADC0 and suffix x = 1 refers to ADC1.

2) The value of V_{AREF} is permitted to be within the range of V_{SSA} - 0.05 V < V_{AREF} < V_{DDM} + 0.05 V. The value specified for the total unadjusted error (TUE) is not guaranteed while the V_{AREF} is out of the specified range.

3) The value of V_{AGND} is permitted to be within the range of V_{SSA} - 0.05 V < V_{AGND} < V_{DDM} + 0.05 V. The value specified for the total unadjusted error (TUE) is not guaranteed while the V_{AGND} is out of the specified range.

4) Definitions for CPS, STC, t_{BC} and t_{DIV} see **Figure 23**.

5) TUE is tested at V_{AREF} = 5 V, V_{AGND} = 0 V and V_{DDM} = 4.9 V.

6) Analog overload conditions during operation occur if the voltage on the respective ADC pin exceeds the specified operating range (i.e. V_{AOV} > V_{DDM} **+ 0.5 V or** V_{AOV} < V_{SSM} **- 0.5 V**) or a short circuit condition occurs on the respective ADC pin. The absolute sum of input currents on all port pins must not exceed **10 mA** at any time. The supply voltage (V_{DD}, V_{DDA0}, V_{DDA1} and V_{SS}, V_{SSA0}, V_{SSA1}) must remain within the specified limits. Under short-circuit conditions the corresponding pin is not ready for use.

7) Applies for one analog input pin.

8) Applies for two numeric adjacent analog input pins.

9) The overload coupling factor (k_A) defines the worst case relation of an overload condition (I_{OV}) at one pin to the resulting leakage current (I_{leak}) into an adjacent pin: $|I_{leak}| = k_A \times |I_{OV}|$.
Thus under overload conditions an additional error leakage voltage (V_{AEL}) will be induced onto an adjacent analog input pin due to the resistance of the analog input source (R_{AIN}). That means $V_{AEL} = R_{AIN} \times |I_{leak}|$.
See also section 7.1.6 “Error Through Overload Conditions” in the TC1765 Peripheral Units User’s Manual for further explanations.

10) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this smaller capacitances are successively switched to the reference voltage. Alternatively, the redistributed charge could be specified.

11) The switched capacitance at the analog voltage input must be charged within the sampling time. Alternatively, the redistributed charge could be specified.

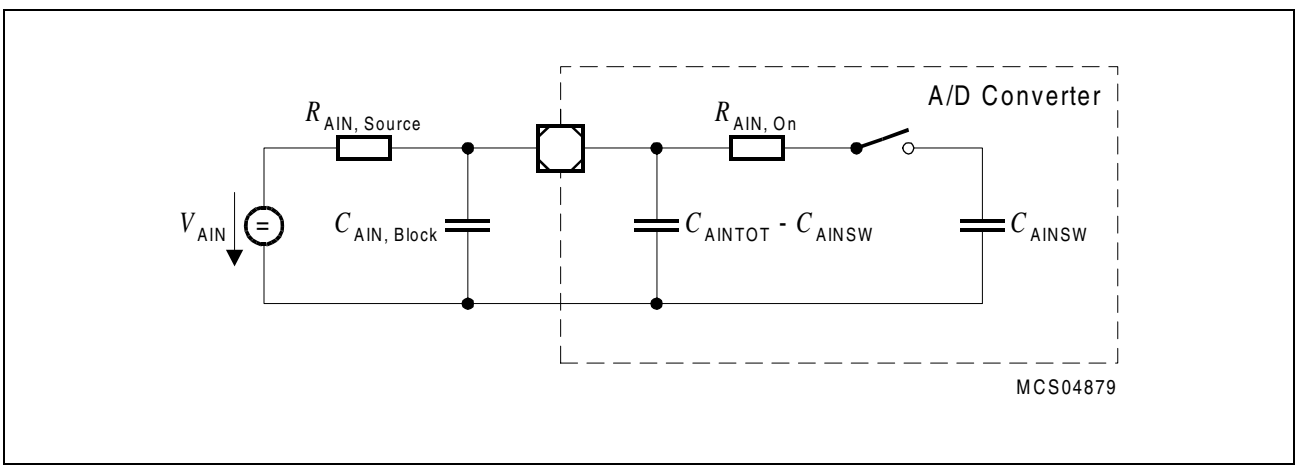


Figure 22 Equivalent Circuitry of Analog Input

Note: This equivalent circuitry for an analog input is also valid for the reference inputs V_{AREF} and V_{AGND}.

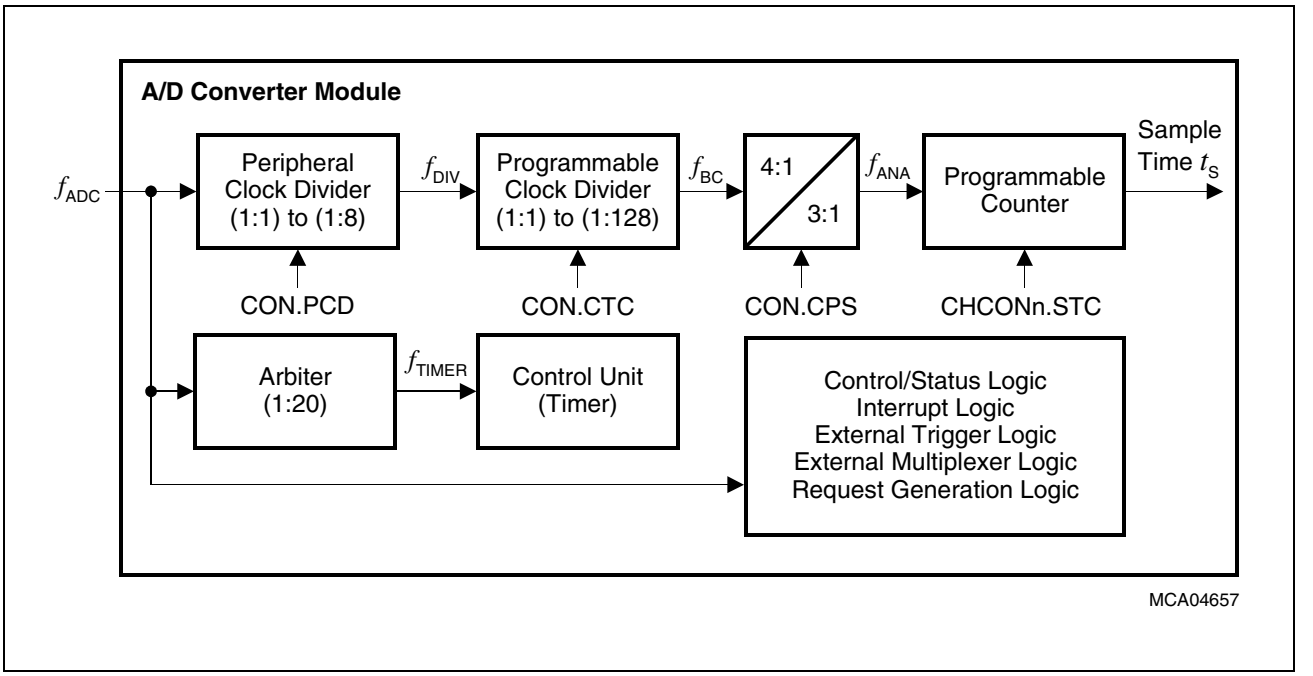


Figure 23 ADC Clock Circuit

Note: The frequency of f_{ADC} is the system clock frequency (f_{SYS}) divided by the value of bit field ADCx_CLC.RMC.

Oscillator Pins (Class C Pins)

T_A = -40 °C to +125 °C; V_{DDOSC} = 2.30 to 2.75 V; V_{SSOSC} = 0 V;

Parameter	Symbol		Limit values		Unit	Test Conditions
			min.	max.		
Input low voltage at XTAL1	V_{ILX}	SR	-0.5	$0.3 \times V_{DDOSC}$	V	–
Input high voltage at XTAL1	V_{IHX}	RR	$0.7 \times V_{DDOSC}$	V_{DDOSC} + 0.5	V	–
Input current at XTAL1	I_{IX1}	CC	–	±20	µA	0 V < V_{IN} < V_{DDOSC}
Input leakage current XTAL1[1)]	I_{OZ}	CC	–	±200	nA	0 V < V_{IN} < V_{DDOSC}

1) Only applicable in deep sleep mode.

Preliminary

Power Supply Current

T_A = -40 °C to +125 °C;

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.[1]	max.		
Active mode supply current	I_{DD}	CC	–	–	200	mA	$\overline{PORST}$ = V_{IL}[2][3]
			–	260	290	mA	Sum of I_{DDS}[4][3]
			–	7	10	mA	I_{DD} at V_{DDP}[4]
			–	201	–	mA	I_{DD} at V_{DD} (Core and EBU)[4]
			–	31	–	mA	I_{DD} at V_{DDRAM}[4]
			–	21[4]	120[5]	mA	I_{DD} at $V_{DDSBRAM}$
			–	0.1	–	mA	I_{DD} at V_{DDAx}[4]
Idle mode supply current	I_{ID}	CC	–	123	–	mA	$\overline{PORST}$ = V_{IH}[2][6][7]
Sleep mode supply current	I_{SL}	CC	–	50	–	mA	$\overline{PORST}$ = V_{IH}[2][7]
Deep sleep mode supply current	I_{DS}	CC	–	5	900	µA	$\overline{PORST}$ = V_{IH}[8]
			–	1	4.4	mA	$\overline{PORST}$ = V_{IH}[9]
Stand-by pin power supply current	I_{SB}	CC	–	1	250	µA	I_{DD} at $V_{DDSBRAM}$[10]
			–	1	200	µA	[11]

1) Parameters in this column are tested at 25 °C, 40 MHz system clock (if applicable) and nominal V_{DD} voltages.

2) These parameters are tested at V_{DDmax} and 40 MHz system clock (bypass mode) with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

3) These power supply currents are defined as the sum of all currents at the V_{DD} power supply lines: V_{DD} + V_{DDP} + V_{DDRAM} + $V_{DDSBRAM}$ + V_{DDOSC} + V_{DDM} + V_{DDA0} + V_{DDA1}

4) These power consumption characteristics are measured while running a typical application pattern. The power consumption of modules can increase or decrease using other application programs. The PLL is inactive during this measurement.

5) This parameter has been evaluated at design characterization using an atypical test pattern that makes extensive usage of the DMU memory.

6) All peripherals are enabled and in idle state.

7) Guaranteed by design characterization.

8) This is the sum of all 2.5 V power supply currents.

9) This is the sum of all 5 V power supply currents.

10) TC1765 in deep sleep mode.

11) All other V_{DD} pins are at 0 V; T_J = 150 °C; $V_{DDSBRAM}$ = 2.0 V.

Preliminary

AC Characteristics

Output Rise/Fall Times

Class A drivers (GPIO Ports 0 to 5): V_{DDP} = 3.0 to 5.25 V; V_{SS} = 0 V

Class B drivers (Bus interface): V_{DD} = 2.30 to 2.75 V; V_{SS} = 0 V

T_A = -40 °C to +125 °C, unless otherwise noted; f_{SYS} = 40 MHz

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Class A Pins						
Nominal output rise/ fall time[1]	t_{RFAnom} CC	–	5	–	ns	T_A = 25 °C, C_L = 50 pF, V_{DDP} = 5.0 V Px_POCON.PDCy = 0 Px_POCON.PECy = 0
Maximal output rise/ fall time[1]	t_{RFAmax} CC	–	–	12	ns	C_L = 50 pF Px_POCON.PDCy = 0 Px_POCON.PECy = 0
Slow output rise/fall time[1]	$t_{RFAslow}$ CC	–	–	55	ns	C_L = 100 pF Px_POCON.PDCy = 0 Px_POCON.PECy = 1
Class B Pins						
Output rise/fall time[1]	t_{RFBmax} CC	–	–	4	ns	for ECOUT C_L = 50 pF
		–	–	7	ns	for all Class B pins except ECOUT C_L = 50 pF

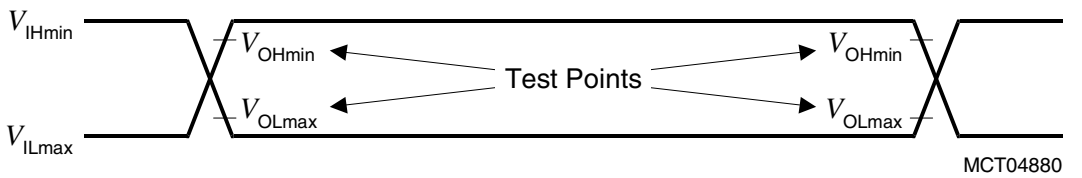
1) Measured from 10% output level to 90% output level and vice versa.

Preliminary

Testing Waveforms

T_A = -40 °C to +125 °C; Frequency: max. 40 MHz;

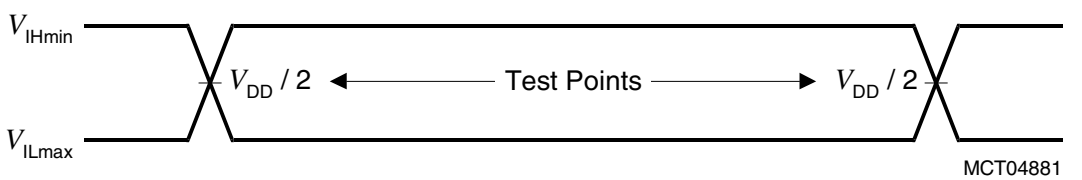
Class A Pins: V_{DDP813} = 3.0 to 5.25 V; V_{SS} = 0 V;



AC inputs during testing are driven with V_{IHmin} for a logic 1 and V_{ILmax} for a logic 0. Timing measurements are made at V_{OHmin} for a logic 1 and V_{OLmax} for a logic 0. Input and Output Low/High max./min. voltages are defined at **Page 60**.

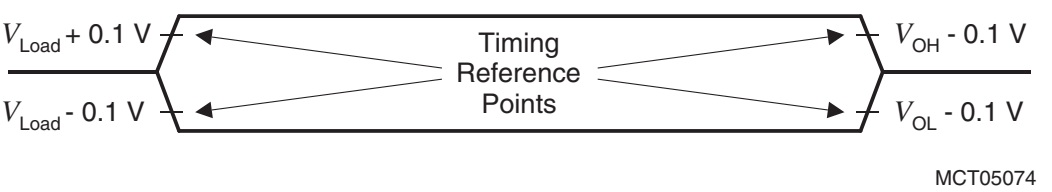
Figure 24 Testing Waveforms for Class A Pins

Class B and Class C Pins: V_{DD} = 2.30 to 2.75 V; V_{SS} = 0 V;
V_{DDOSC} = 2.30 to 2.75 V; V_{SSOSC} = 0 V;



AC inputs during testing are driven with V_{IHmin} for a logic 1 and V_{ILmax} for a logic 0. Timing measurements are made at $V_{DD}/2$ for a logic 1 and for a logic 0. Input Low/High max./min. voltages are defined at **Page 61** and **Page 68**.

Figure 25 Testing Waveforms for Class B and Class C Pins



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 15 mA).

Figure 26 Tri-State Testing Waveforms for Class B Pins

Preliminary

Input Clock Timing

V_{DDOSC} = 2.30 to 2.75 V; V_{SSOSC} = 0 V; T_A = -40 °C to +125 °C;

Parameter		Symbol	Limit Values		Unit
			min.	max.	
Oscillator clock frequency	direct drive	f_{OSC} SR (= $1/t_{OSC}$)	4	16	MHz
	with PLL		10	16	MHz
Input clock frequency driving at XTAL1	direct drive	$1/t_{OSCDD}$ SR	–	40	MHz
	with PLL		10	30	MHz
Input clock high time		t_1 SR	7	–	ns
Input clock low time		t_2 SR	7	–	ns
Input clock rise time		t_3 SR	–	4	ns
Input clock fall time		t_4 SR	–	4	ns

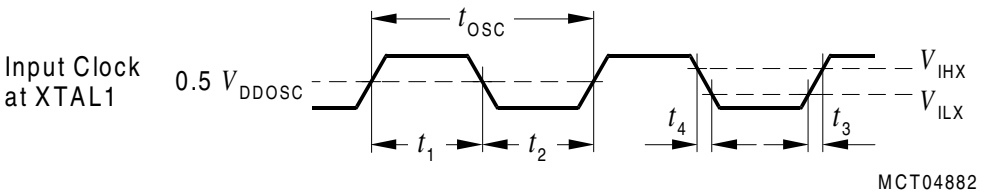


Figure 27 Input Clock Timing

Preliminary

ECOUT and CPUCLK Timing

V_{SS} = 0 V; V_{DD} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values			Unit
			min.	typ.	max.	
Clock period	t_{CPUCLK} t_{ECOUT}	CC	25	–	–	ns
Clock high time	t_5	CC	7.5	–	–	ns
Clock low time	t_6	CC	7.5	–	–	ns
Clock rise time	t_7	CC	–	–	4	ns
Clock fall time	t_8	CC	–	–	4	ns
Clock duty cycle $t_5/(t_5 + t_6)$	DC	CC	45	50	55	%

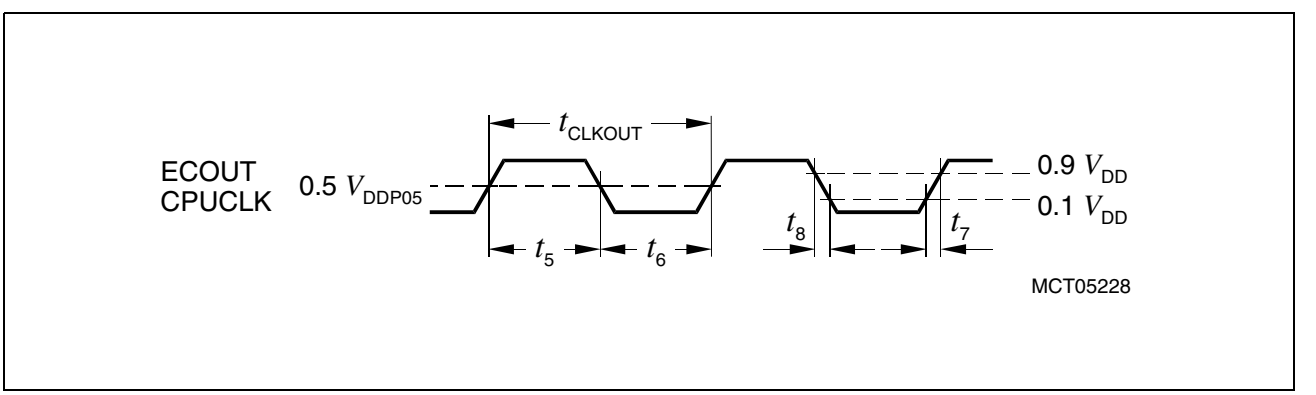


Figure 28 ECOUT/CPUCLK Output Clock Timing

Preliminary

PLL Parameters

Note: All PLL characteristics defined on this and the next page are guaranteed by design characterization.

V_{SS} = 0 V; V_{DD} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C;

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Accumulated jitter	D_N	see Figure 29		–
VCO frequency range	f_{VCO}	150	200	MHz
PLL base frequency	$f_{PLLBASE}$	40	130	MHz
PLL lock-in time	t_L	–	200	µs

Phase Locked Loop Operation

When PLL operation is enabled and configured (see Figure 16 and Page 51), the PLL clock f_{VCO} (and with it the system clock f_{SYS}) is constantly adjusted to the selected frequency. The relation between f_{VCO} and f_{SYS} is defined by: $f_{VCO} = K \times f_{SYS}$. The PLL causes a jitter of f_{SYS} and CPUCLK/ECOUT, which is directly derived from f_{SYS} and which has its frequency.

The following two formulas define the (absolute) approximate maximum value of jitter D_N in ns dependent on the K-factor, the system clock frequency f_{SYS} in MHz, and the number P of consecutive f_{SYS} periods.

$$\text{for } P < \frac{23.5}{K} \qquad D_N\,[\text{ns}] = \pm \frac{3.9}{f_{SYS}\,[\text{MHz}]} \times P + 1.2 \qquad [1]$$

$$\text{for } P \geq \frac{23.5}{K} \qquad D_N\,[\text{ns}] = \pm \frac{91.7}{f_{SYS}\,[\text{MHz}] \times K} + 1.2 \qquad [2]$$

With rising number P of clock cycles the maximum jitter increases linearly up to a value of P that is defined by the K-factor of the PLL. Beyond this value of P the maximum accumulated jitter remains at a constant value. Further, a lower system clock frequency f_{SYS} results in a higher maximum jitter.

Figure 29 gives an example for typical jitter curves with K = 4 @40 MHz, K = 6 @33 MHz, and K = 8@20/25 MHz.

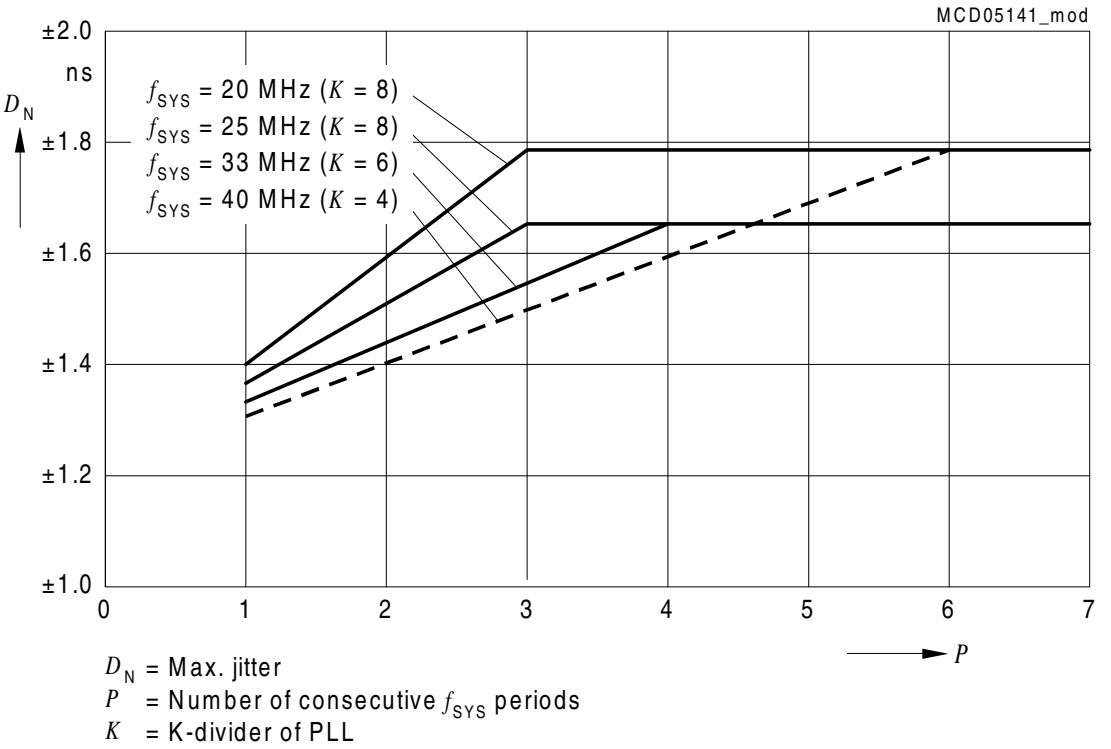


Figure 29 Approximated Maximum Accumulated PLL Jitter for Typical System Clock Frequencies f_{SYS}

*Note: For safe clock generation and PLL operation the definitions and restrictions as defined at pages **50**, **51**, and **72** must be regarded.*

Preliminary

EBU Demultiplexed Timing

V_{SS} = 0 V; V_{DD} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
Output delay from ECOUT ↓	t_{10}	CC	0	9	ns
Output delay from ECOUT ↑	t_{11}	CC	-2	4	ns
Data setup to ECOUT ↑	t_{12}	SR	9	–	ns
Data hold from ECOUT ↑ [1]	t_{13}	SR	1	–	ns
Data valid after ECOUT ↓ [1]	t_{15}	CC	2	–	ns
Data setup to ECIN ↓ [2]	t_{31}	SR	see **Page 80**	–	ns
Data hold from ECIN ↓ [2]	t_{32}	SR	see **Page 80**	–	ns

[1] Valid for EBU_BUSCONx.26 = 0.

[2] Valid for EBU_BUSCONx.26 = 1 (early sample feature).

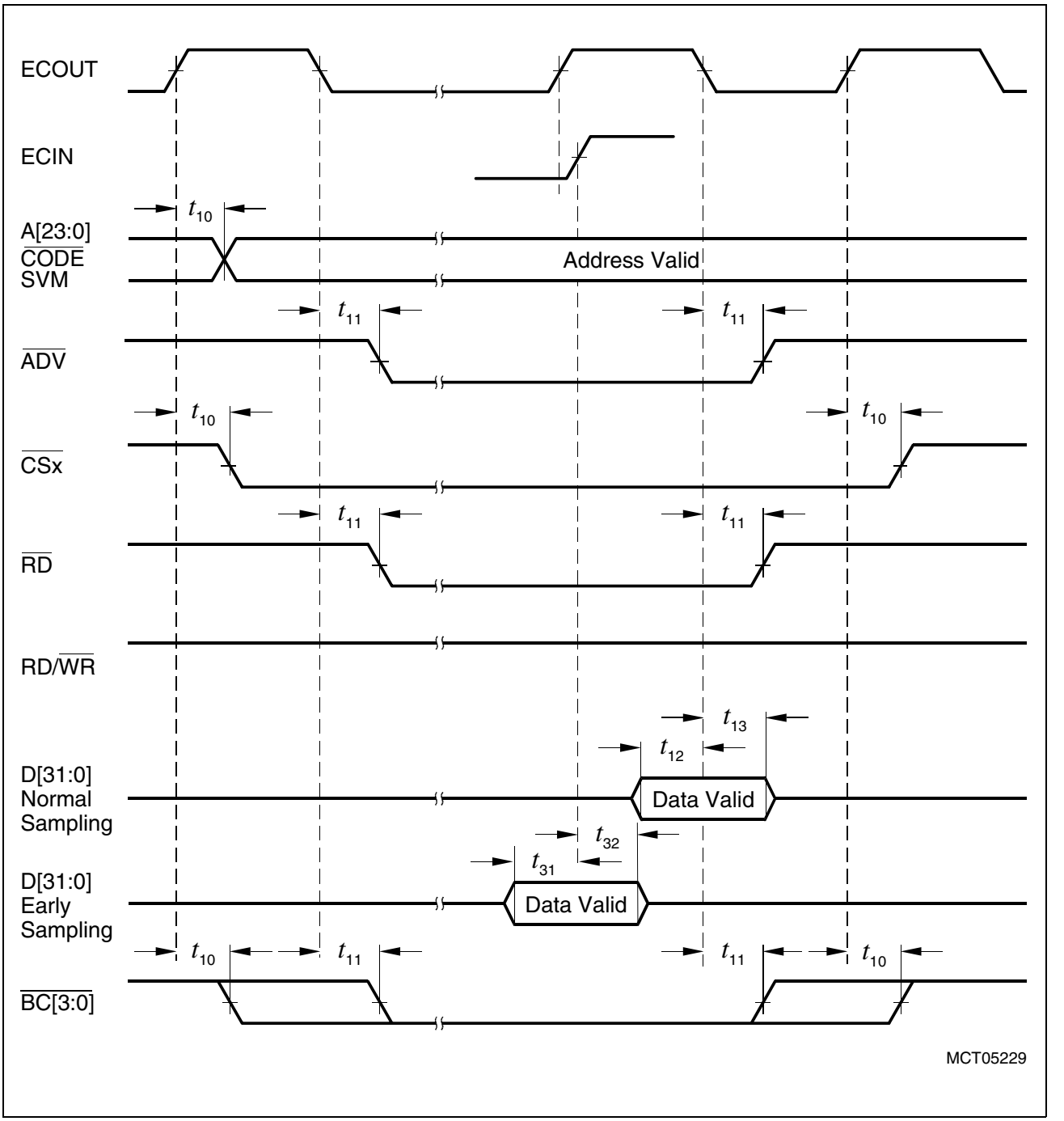


Figure 30 EBU Demultiplexed Read Timing

*Note: WAIT timing see **Figure 32**.*

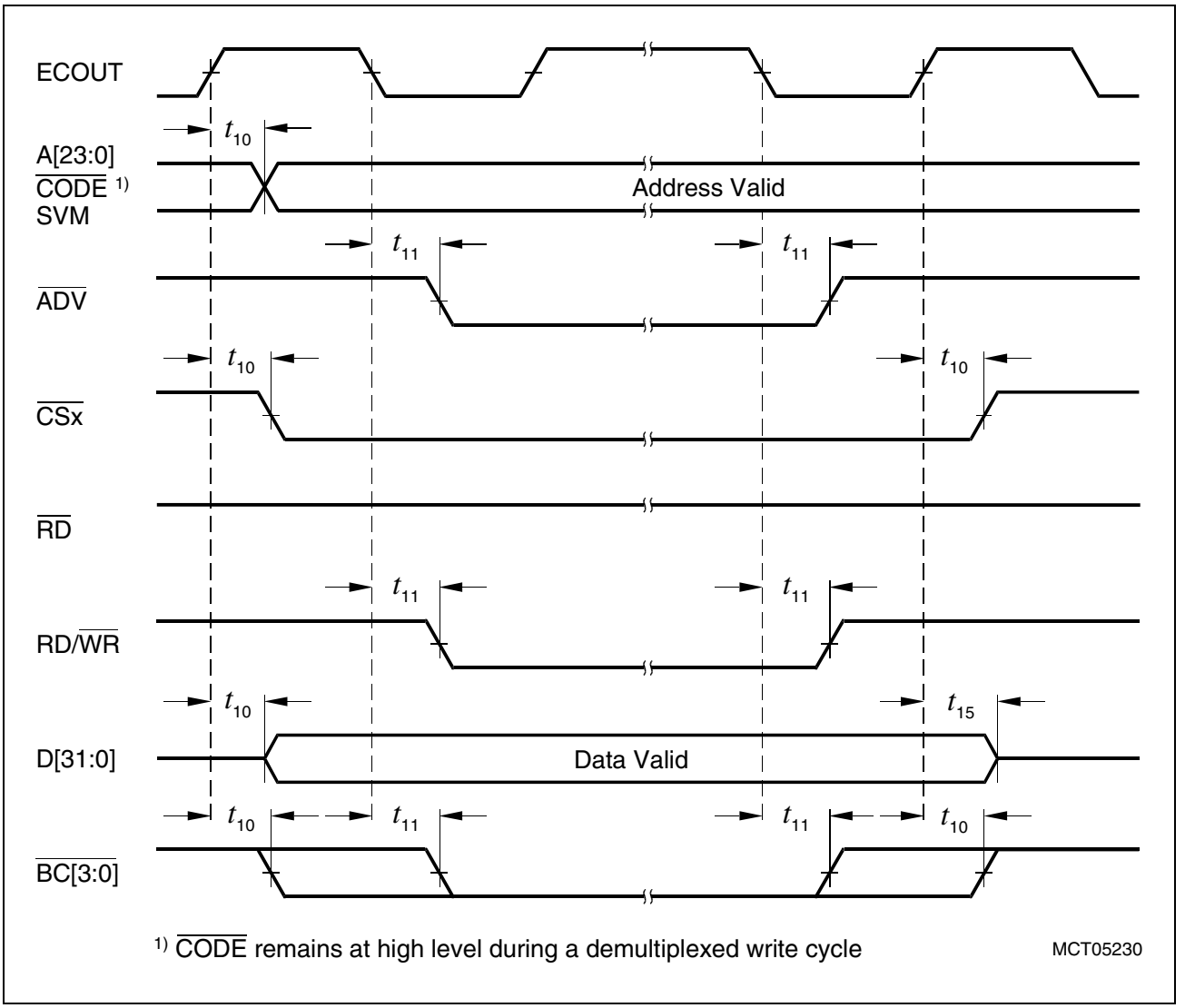


Figure 31 EBU Demultiplexed Write Timing

Preliminary

$\overline{\text{WAIT}}$ Timing (FPI Bus to External Memory)

V_{SS} = 0 V; V_{DD} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
$\overline{\text{WAIT}}$ setup to ECOUT ↓	t_{50}	SR	14[1)]	–	ns
$\overline{\text{WAIT}}$ hold from ECOUT ↓	t_{51}	SR	14[1)]	–	ns
$\overline{\text{WAIT}}$ setup to ECOUT ↑	t_{52}	SR	11	–	ns
$\overline{\text{WAIT}}$ hold from ECOUT ↑	t_{53}	SR	2	–	ns

1) Guaranteed by design characterization.

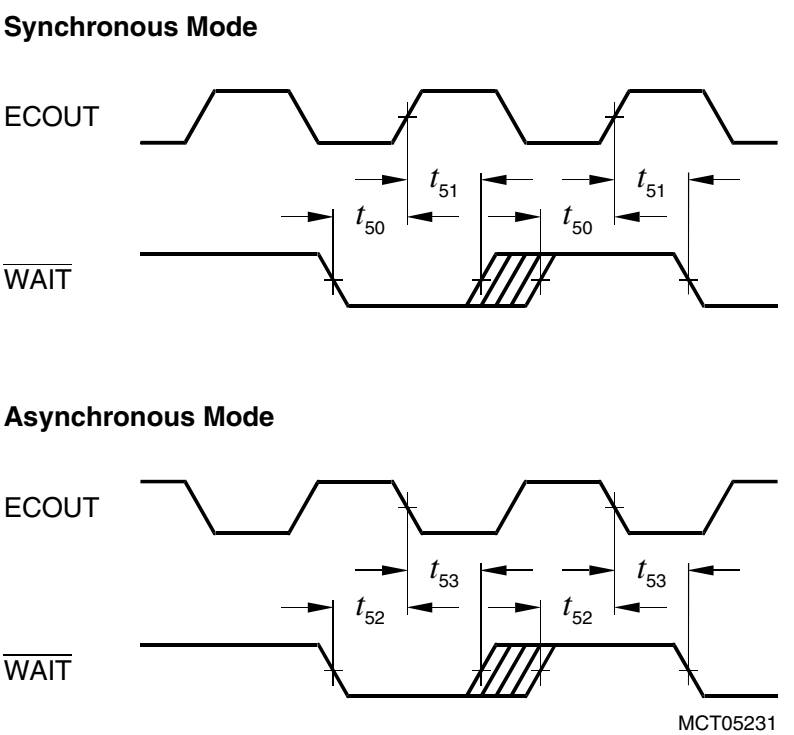


Figure 32 $\overline{\text{WAIT}}$ Timing (from FPI Bus to external Memory)

Preliminary

EBU Burst Mode Timing

V_{SS} = 0 V, V_{DD} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
Output delay from ECIN ↓	t_{30}	CC	2	14	ns
Data setup to ECIN ↓	t_{31}	SR	4[1)]	–	ns
Data hold from ECIN ↓	t_{32}	SR	1[1)]	–	ns

1) Guaranteed by design characterization.

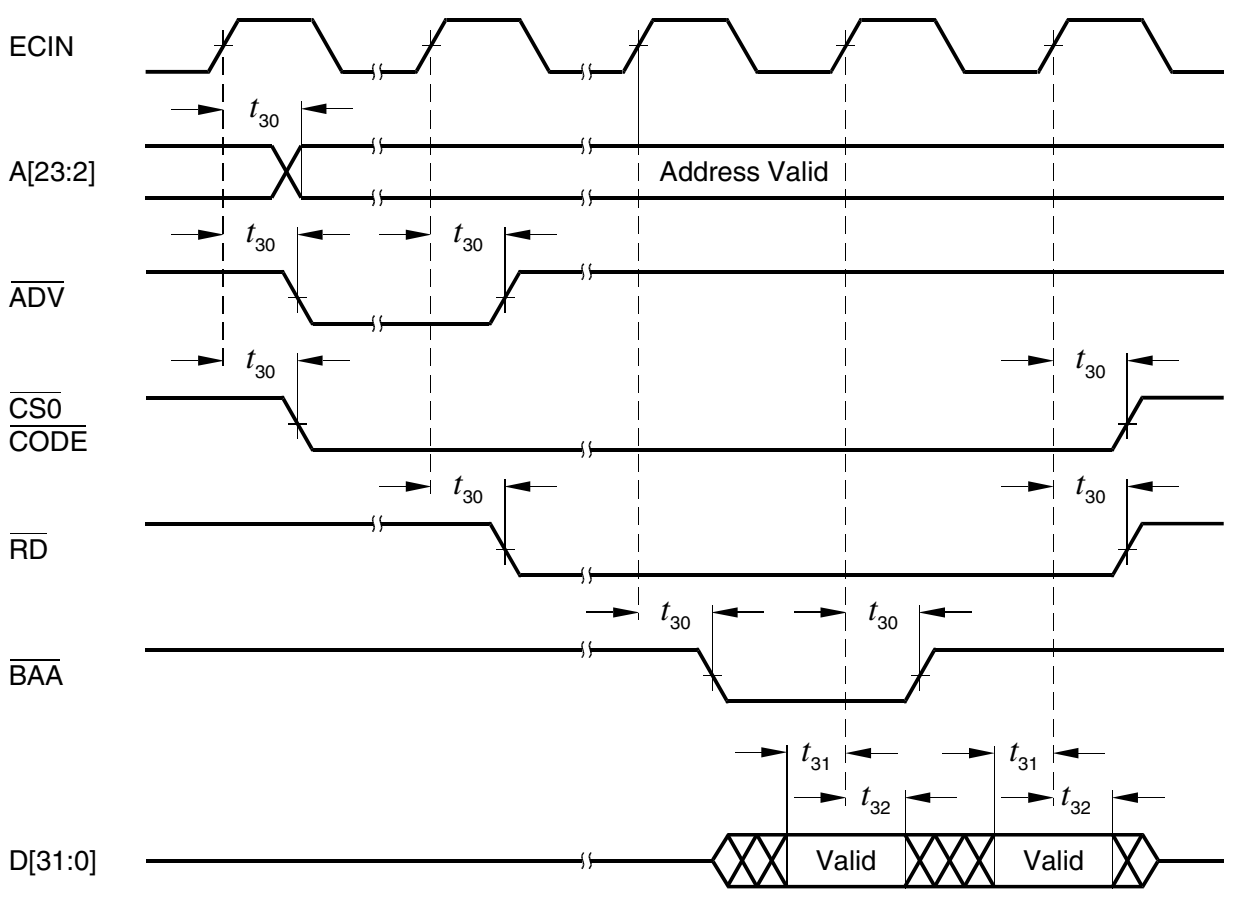


Figure 33 Burst Mode Timing (Instruction Read)

Preliminary

Trace Port Timing (TC1765T only)

This timing is applicable for TP[15:0] when CPU or DMA trace mode is enabled (SCU_CON.ETEN = 1).

V_{SS} = 0 V; V_{DD} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
TP[15:0] and $\overline{\text{BRKOUT}}$ high/low from CPUCLK ↓	t_{55}	CC	0	8	ns

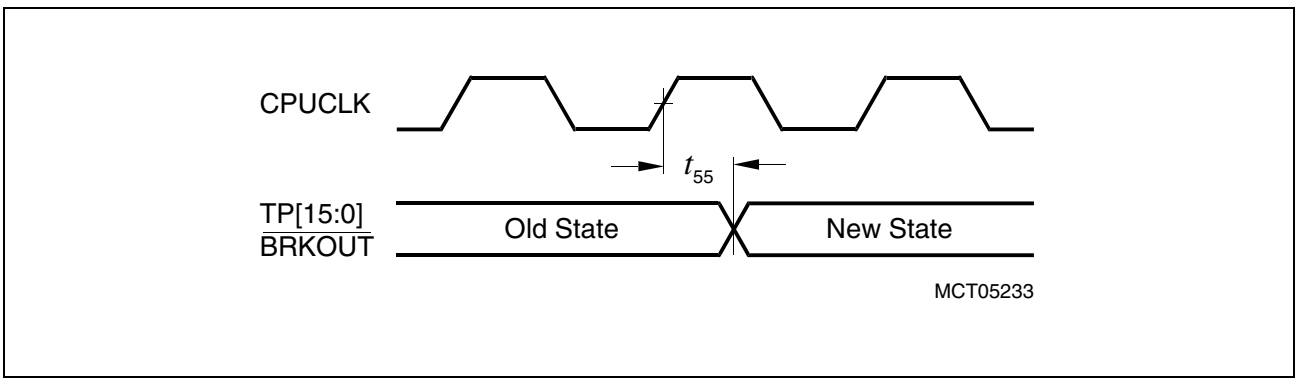


Figure 34 Trace Port Timing

Preliminary

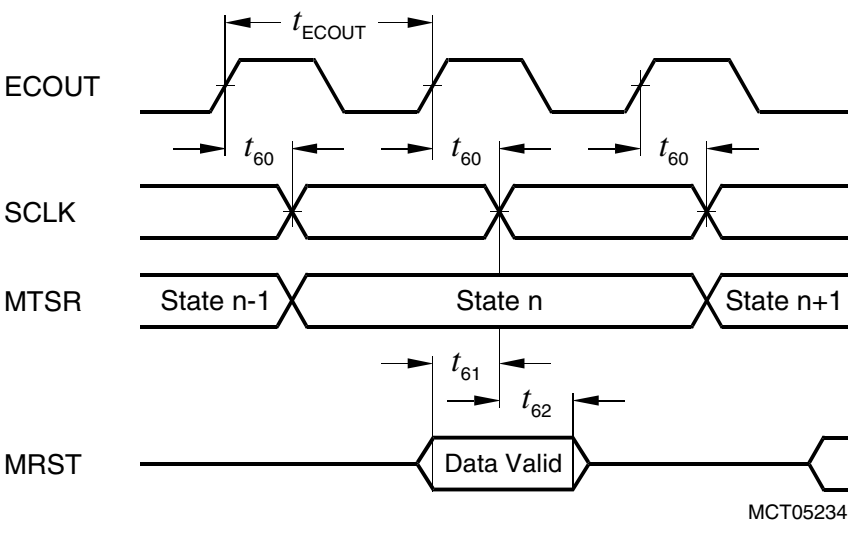
SSC Master Mode Timing

V_{SS} = 0 V; V_{DDP} = 4.5 to 5.25 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK / $\overline{\text{MTSR}}$ low/high from ECOUT ↘↗ [1]	t_{60}	CC	–	7	ns
MRST setup to SLCK rising/falling edge	t_{61}	SR	18[2]	–	ns
MRST hold from SLCK rising/falling edge	t_{62}	SR	10[2]	–	ns

1) This parameter is valid for high current mode output driver characteristic and normal timing edge characteristic (POCON.PECx = 0 and POCON.PDCx = 0) of the corresponding SSC output lines.

2) Guaranteed by design characterization.



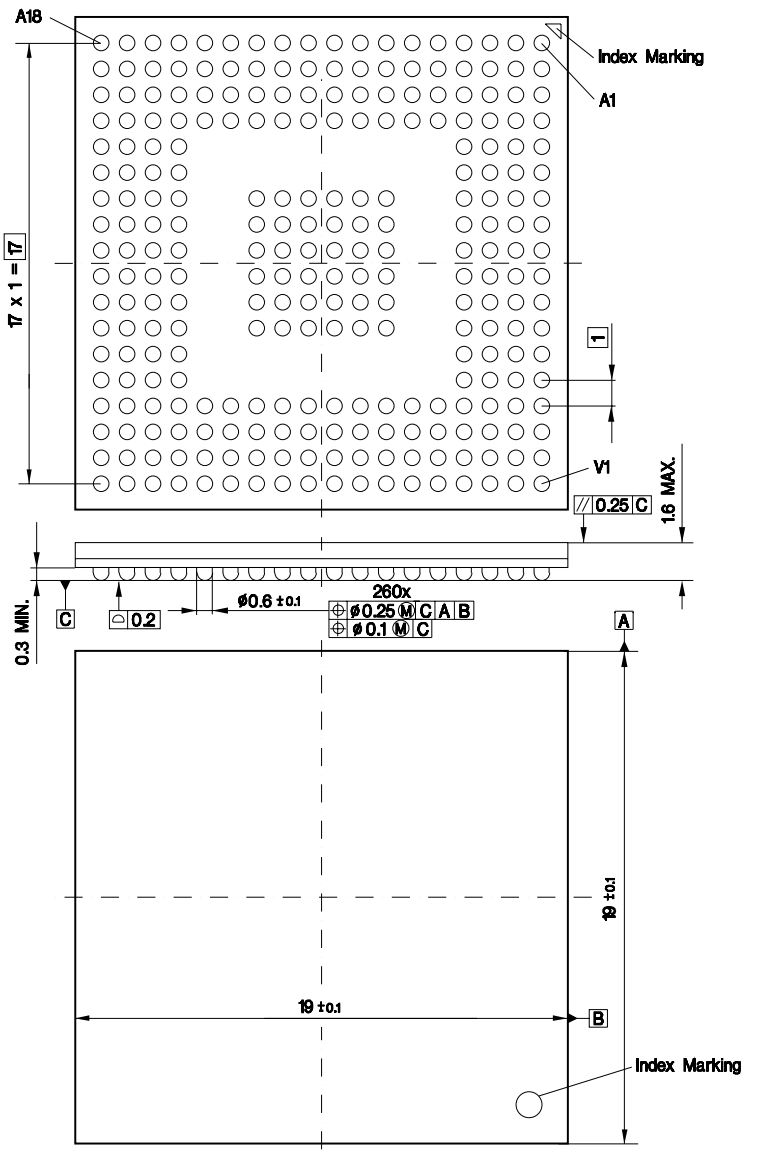
Note: The timing diagram assumes the highest possible baudrate operation.
($f_{SSC} = f_{ECOUT}$, SSCx_CLC.RMC = 1, SSCx_BR.BR_VALUE = 0000_H)

Figure 35 SSC Master Mode Timing

Preliminary

Package Outlines

P-LBGA-260-2
Plastic Low Profile Pitch Ball Grid Array



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