

## **Voltage Controlled Crystal Oscillator**

**5V, HCMOS** 

#### Technical Data S150x / ST150x Series





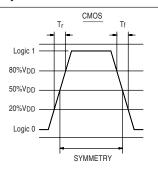
## Description

A voltage controlled crystal oscillator designed with excellent Jitter characteristics - ideal for telecom applications. The HCMOS output can drive high speed CMOS & TTL loads. Devices are in standard 14-pin DIP metal packages. Pin 7(4 on 1/2 size) is grounded to reduce EMI. SMD DIL 14 version is available utilizing adaptor technology (see separate data sheet for dimensions).

#### **Applications & Features**

- Phase Locked Loop (PLL) Clock & Data Recovery, Frequency Translation, Frequency Synthesis in Video, Video Compression, Telephony, and LAN/ WAN Data Communication and other Telecommunication applications.
- HCMOS / TTL compatible
- 3.5ps max RMS period jitter
- $\pm$  50, 100 or 200 ppm APR\*
- $\pm$  20, 25 or 50 ppm Stability
- Tri-State option available
- SMD versions for IR reflow available

#### **Output Waveform**



Frequency Range:	1.5 MHz to 100 MHz ( Full Size ) 1.5 MHz to 28.6363 MHz ( Half Size )	
Frequency Stability:	$\pm 20$ , $\pm 25$ or $\pm 50$ ppm over all conditions: operating temperature, voltage change, load change, calibration tolerance, shock and vibration, with $V_C = 2.5V$	

1 5 MII- 4- 100 MII- ( E-11 C:-- )

Aging @ 25°C: ± 3ppm max per year, ±10ppm max for 10 years

Temperature Range:

0 to +70°C or -40 to +85°C Operating: Storage: -55 to +125°C

**Supply Voltage:** 

Recommended Operating:  $5V \pm 10\%$ 

**Supply Current:** 

Full Size Package: 1.5 to 11.9MHz: 20mA max with 30pF load 12 to 70MHz: 65mA max with 30pF load 70+ to 100MHz: 60mA max with 15pF load

Half Size Package: 1.5 to 28.6363MHz: 25mA max with 30pF load

**Output Drive:** 

Symmetry: 45/55% max @ 50%  $V_{\mbox{\scriptsize DD}}$  1.5 to 70 MHz 40/60% max @ 50% V<sub>DD</sub> 70+ to 100 MHz

Rise & Fall Times: 20% to 80% VDD 8ns max rise, 6ns max fall, full size package 1.5 to 25 MHz: 25+ to 70 MHz: 5ns max rise & fall, full size package

70+ to 100 MHz: 3ns max rise & fall, full size package 1.5 to 28.6363 MHz: 6ns max rise & fall, half size package

> Logic 0: 10% V<sub>DD</sub> max Logic 1: 90% V<sub>DD</sub> min

Load: 30pF to 70 MHz, 15pF from 70+ to 100 MHz

Period Jitter RMS: 3.5ps max

**Pull Characteristics:** 

Input Impedance (pin 1): 50KΩ min Frequency Response (-3dB): 10 kHz min

±50, ±100, ±200ppm APR\* min, See Part Numbering Guide Pullability:

Control Voltage:

Transfer Function: Frequency increases when Control Voltage increases

Linearity: 5 or 10% max

Center Control Voltage: 2.5V

#### Mechanical:

MIL-STD-883, Method 2002, Condition B Shock:

Solderability: MIL-STD-883, Method 2003

Terminal Strength: MIL-STD-883, Method 2004, Conditions B2 Vibration: MIL-STD-883, Method 2007, Condition A

Solvent Resistance: MIL-STD-202, Method 215

MIL-STD-202, Method 210, Conditions A, B or C Resistance to Soldering Heat:

( I or J for Gull Wing or SMD)

Environmental:

Gross Leak Test: MIL-STD-883C, Method 1014, Condition C MIL-STD-883C, Method 1014, Condition A2 Fine Leak Test: Thermal Shock: MIL-STD-883C, Method 1011, Condition A Moisture Resistance: MIL-STD-883C, Method 1004

\* APR = (VCXO Pull relative to specified Output Frequency) - (VCXO Frequency Stability) - (Aging) 10 years aging is inclusive on 1/2 size version

> DS-197 REV E



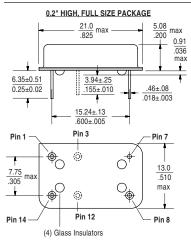
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## Technical Data

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## **Package Details**



#### Pin Function:

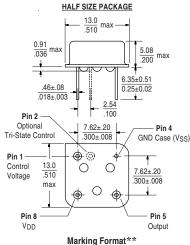
Pin 1: Control Voltage Pin 3: Tri-State Control (optional) Pin 7: GND/Case (VSS) Pin 8: OUTPUT Pin 12: N/C (optional) Pin 14: VDC (VDD)

#### Marking Format\*\*

Includes Date Code, Frequency, Part Number



Denotes Pin I

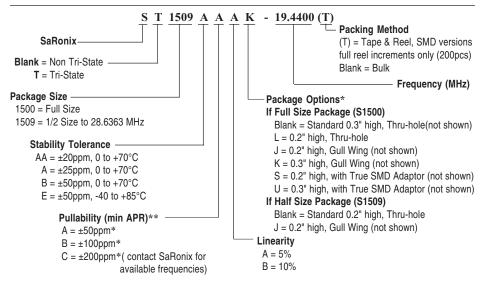


Includes Date Code, Frequency, Part Number



\*\*Exact location of items may vary Scale: None (Dimensions in  $\frac{mm}{inches}$ )

#### Part Numbering Guide



\*Products are available with the following combination of Frequency, Pull and Package

Frequency	Pullability	Full Size (S1500)	Half Size (S1509)
1.5 to 28.6363MHz	A, B	L, J, S	Standard, J
	С	Standard, K, U	
28.6363+ to 100MHz	A, B, C	Standard, K, U	

\*\* APR = (VCXO Pull relative to specified Output Frequency) – (VCXO Frequency Stability) – (Aging)

10 years aging is inclusive on 1/2 size version

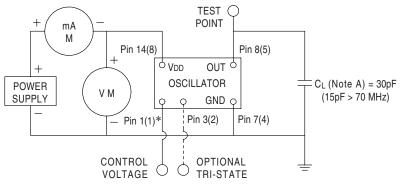
### **Tri-State Logic Table**

Pin 3(2) Input	Pin 8(5) Output	
Logic 1 or NC	Oscillation	
Logic 0 or GND	High Impedance	

Required Input Levels on Pin 3(2):

Logic 1 = 3.0V min Logic 0 = 0.5V max

### **Test Circuit**



NOTE A: C<sub>L</sub> includes probe and fixture capacitance.

\*Items in brackets() represent Half Size model

All specifications are subject to change without notice.

DS-197 REV E



# True SMD Adaptor - 7.57mm High

# Technical Data 20.32 13.4 .527 15.24 .600 RECOMMENDED LAND PATTERN REV A



# True SMD Adaptor - 9.85mm High

