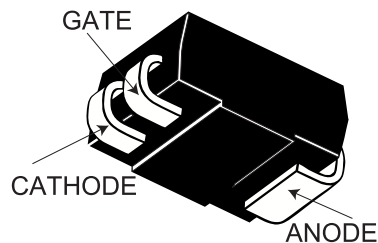


**NEW
Compak
Package**

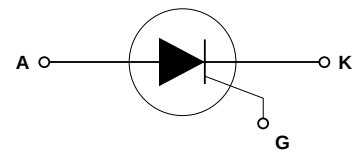


**3-Leaded
Surface Mount**

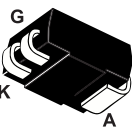
Features

- Surface mount package
- New smaller 3-leaded COMPAK package
- Glass-passivated junctions
- Voltage capacity up to 600 Volts
- 0.8 Amp RMS current capacities
- Four gate sensitivities available
- Operating temperature (T_J) from -40°C to $+110^{\circ}\text{C}$
- Storage temperature (T_S) from -40°C to $+150^{\circ}\text{C}$
- Packaged in embossed carrier tape with 2,500 devices per reel

Sensitive SCR
0.8 Amp



Electrical Specifications

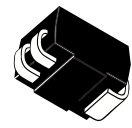
Part Number	I_T		V_{DRM} & V_{RRM}	I_{GT}	I_{DRM} & I_{RRM}		V_{TM}	V_{GT}			I_H
 COMPACT "C" Package	Maximum On-State Current (1) Amps		Repetitive Peak Off-State Forward and Reverse Voltage	DC Gate Trigger Current $V_D=6VDC$ $R_L=100\text{ ohms}$	Peak Off-State Current at V_{DRM} & V_{RRM} (11)		Peak Off-State Voltage (3)	DC Gate Trigger Voltage $V_D=6VDC$ $R_L=100\text{ ohms}$ (4)			DC Holding Current (5) (8)
	Amps		Volts	μAmps	μAmps		Volts	Volts			milliAmps
	RMS	AV			$T_L = 25^\circ C$	$T_L = 110^\circ C$	$T_L = 25^\circ C$	$T_L = -40^\circ C$	$T_L = 25^\circ C$	$T_L = 110^\circ C$	
	MAX		MIN	MAX	MAX						
S1S1	0.8	0.51	100	12	2.0	100	1.7	1.2	0.8	0.2	5.0
S2S1	0.8	0.51	200	12	2.0	100	1.7	1.2	0.8	0.2	5.0
S4S1	0.8	0.51	400	12	2.0	100	1.7	1.2	0.8	0.2	5.0
S6S1	0.8	0.51	600	12	2.0	100	1.7	1.2	0.8	0.2	5.0
S1S2	0.8	0.51	100	50	2.0	100	1.7	1.2	0.8	.25	5.0
S2S2	0.8	0.51	200	50	2.0	100	1.7	1.2	0.8	.25	5.0
S4S2	0.8	0.51	400	50	2.0	100	1.7	1.2	0.8	.25	5.0
S6S2	0.8	0.51	600	50	2.0	100	1.7	1.2	0.8	.25	5.0
S1S	0.8	0.51	100	200	2.0	100	1.7	1.2	0.8	.25	5.0
S2S	0.8	0.51	200	200	2.0	100	1.7	1.2	0.8	.25	5.0
S4S	0.8	0.51	400	200	2.0	100	1.7	1.2	0.8	.25	5.0
S6S	0.8	0.51	600	200	2.0	100	1.7	1.2	0.8	.25	5.0
S1S3	0.8	0.51	100	500	2.0	100	1.7	1.2	0.8	.25	8.0
S2S3	0.8	0.51	200	500	2.0	100	1.7	1.2	0.8	.25	8.0
S4S3	0.8	0.51	400	500	2.0	100	1.7	1.2	0.8	.25	8.0
S6S3	0.8	0.51	600	500	2.0	100	1.7	1.2	0.8	.25	8.0

Notes to Electrical Specifications

- See Figures 1 & 2 for current ratings at specified operating temperatures.
- See Figure 3 for I_{GT} vs. T_L .
- See Figure 4 for instantaneous on-state current (I_T) vs. on-state voltage (V_T) - (typical).
- See Figure 5 for V_{GT} vs. T_L .
- See Figure 6 for I_H vs. T_L .
- For more than one cycle see Figure 7.
- Test condition, $I_{GT} = 100\text{mA}$, pulse width $> 15\mu\text{Sec.}$, rise time $< 0.1\mu\text{Sec.}$ See Figure 8 for t_{gt} vs. I_{GT} .
- DC holding current initial on-state current 20mA.
- di/dt test conditions, $I_{GT} = 50\text{mA}$ with $0.1\mu\text{Sec.}$ rise time.
- Test conditions, $T_L < 80^\circ C$, rectangular current waveform, rate-of-rise of current $< 10\text{A}/\mu\text{Sec.}$, rate-of-reversal of current $< 5\text{A}/\mu\text{Sec.}$, $I_{TM} = 1\text{A}$ ($50\mu\text{Sec.}$ pulse), repetition = 60pps. V_{RRM} = Rated. $V_R = 15\text{V}$ minimum, V_{DRM} = Rated, Gate Bias = 0V, 100 ohm (during turn-off timer interval).
- $T_L = T_J$ for test conditions in off-state.
- Pulse width $< 10\mu\text{Sec.}$

General Notes

- The lead temperature (T_J) is measured as shown on dimensional outline drawing. See Package Dimensions on the next page.
- All measurements (except I_{GT}) are made with an external resistor $R_{GK} = 1\text{K ohms}$ unless otherwise noted.
- All measurements are made at 60Hz with a resistive load at an ambient temperature of $+25^\circ C$ unless otherwise specified.
- Operating temperature (T_J) from $-40^\circ C$ to $+110^\circ C$
- Storage temperature (T_S) from $-40^\circ C$ to $+150^\circ C$

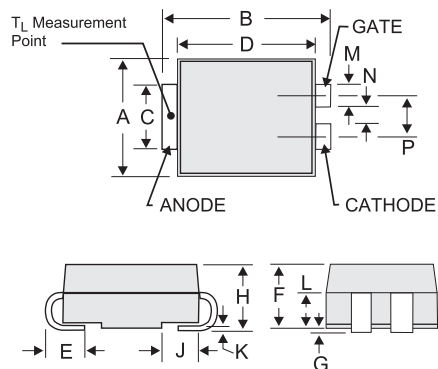
	
Thermal Resistance (Steady State) $R_{\theta JL}$ (Typ.) $^\circ C/W$	
60	

Sensitive SCR 0.8 Amp

I_{GM}	V_{GRM}	P_{GM}	$P_{G(AV)}$	I_{TSM}		dv/dt	di/dt	t_{gt}	t_q	I^2t
Peak Gate Current (12)	Peak Reverse Gate Voltage	Peak Gate Power Dissipation (12)	Average Gate Power Dissipation	Peak One Cycle Surge Forward Current (1) (6)		Critical Rate-of-Rise of Forward Off-State Voltage	Maximum Rate-of-Change of On-State Current (9)	Gate Controlled Turn-On Time (7)	Circuit Commutated Turn-Off Time (10)	RMS Surge (Non-repetitive) On-State current for a period of 8.3ms for fusing
Amps	Volts	Watts	Watts	Amps		Volts/ μ Sec	Amps/ μ Sec	μ Sec	μ Sec	Amps ² /Sec
				60Hz	50Hz					
	MIN					MIN		TYP	MAX	
1.0	5.0	1.0	0.1	20	16	20	50	2.0	60	1.6
1.0	5.0	1.0	0.1	20	16	20	50	2.0	60	1.6
1.0	5.0	1.0	0.1	20	16	20	50	2.0	60	1.6
1.0	5.0	1.0	0.1	20	16	10	50	2.0	60	1.6
1.0	5.0	1.0	0.1	20	16	25	50	3.0	60	1.6
1.0	5.0	1.0	0.1	20	16	25	50	3.0	60	1.6
1.0	5.0	1.0	0.1	20	16	25	50	3.0	60	1.6
1.0	5.0	1.0	0.1	20	16	10	50	3.0	60	1.6
1.0	5.0	1.0	0.1	20	16	30	50	4.0	50	1.6
1.0	5.0	1.0	0.1	20	16	30	50	4.0	50	1.6
1.0	5.0	1.0	0.1	20	16	30	50	4.0	50	1.6
1.0	5.0	1.0	0.1	20	16	15	50	4.0	50	1.6
1.0	5.0	1.0	0.1	20	16	40	50	5.0	45	1.6
1.0	5.0	1.0	0.1	20	16	40	50	5.0	45	1.6
1.0	5.0	1.0	0.1	20	16	40	50	5.0	45	1.6
1.0	5.0	1.0	0.1	20	16	20	50	5.0	45	1.6

Package Dimensions

COMPAK
"C" package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.140	0.155	3.56	3.94
B	0.205	0.220	5.21	5.59
C	0.077	0.083	1.96	2.11
D	0.166	0.180	4.22	4.57
E	0.036	0.056	0.91	1.42
F	0.073	0.083	1.85	2.11
G	0.004	0.008	0.10	0.20
H	0.082	0.092	2.08	2.34
J	0.043	0.053	1.09	1.35
K	0.008	0.012	0.20	0.30
L	0.039	0.049	0.99	1.24
M	0.022	0.028	0.56	0.71
N	0.027	0.033	0.69	0.84
P	0.052	0.058	1.32	1.47

Figure 1: Maximum Allowable Lead Temperature vs. RMS On-State Current.

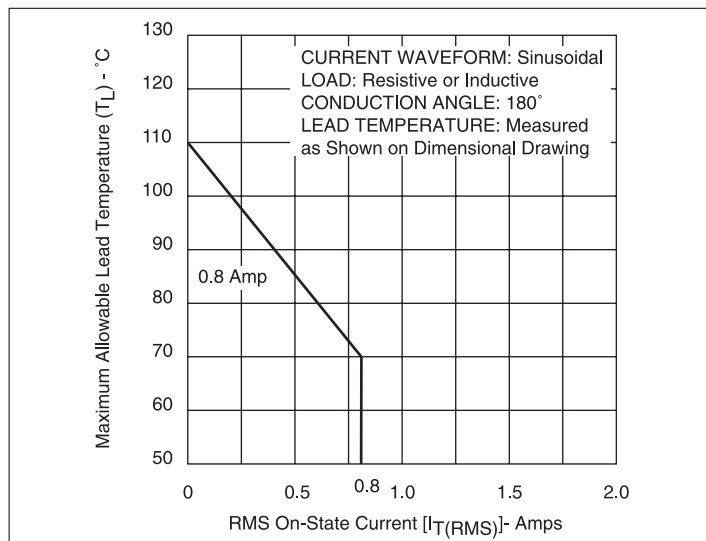


Figure 4: Instantaneous On-State Current vs. On-State Voltage (Typical).

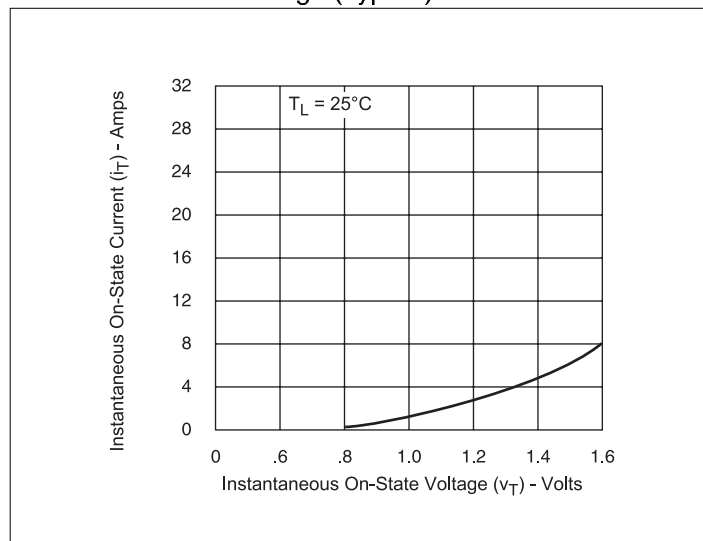


Figure 2: Maximum Allowable Lead Temperature vs. Average On-State Current.

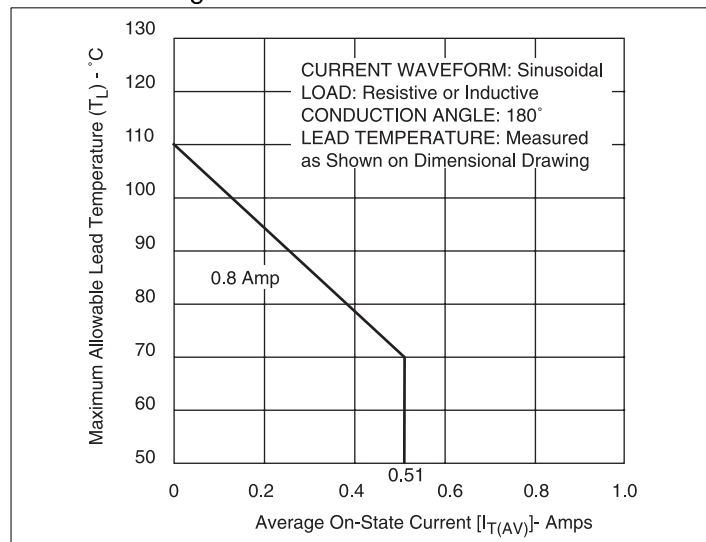


Figure 5: Normalized DC Gate - Trigger Voltage vs. Lead Temperature.

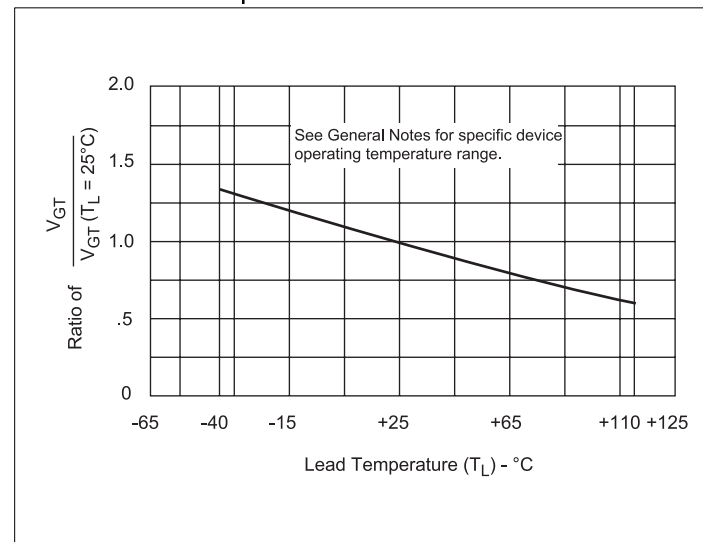


Figure 3: Gate - Trigger Current vs. Lead Temperature

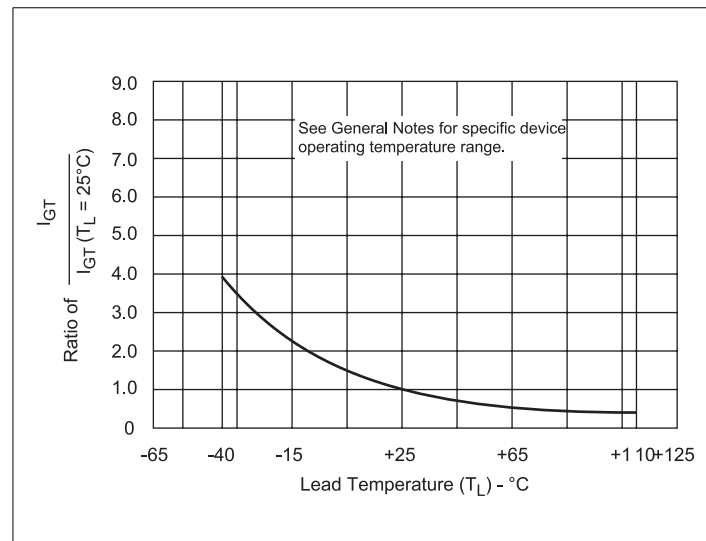


Figure 6: Normalized DC Holding Current vs. Lead Temperature.

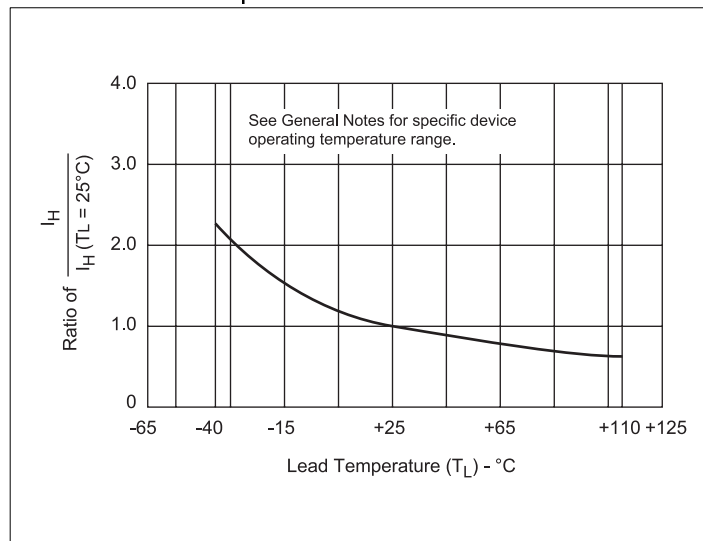


Figure 7: Peak Surge On-State Current vs. Surge Current Duration.

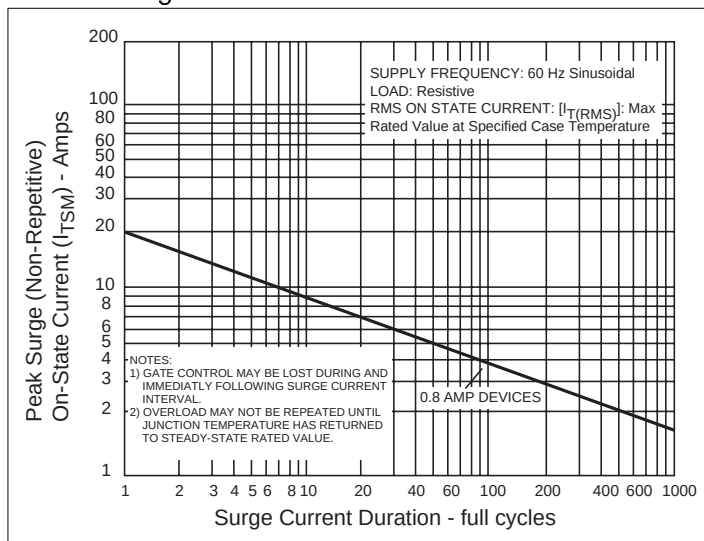


Figure 8: Typical Turn-On time vs. Gate Trigger Current.

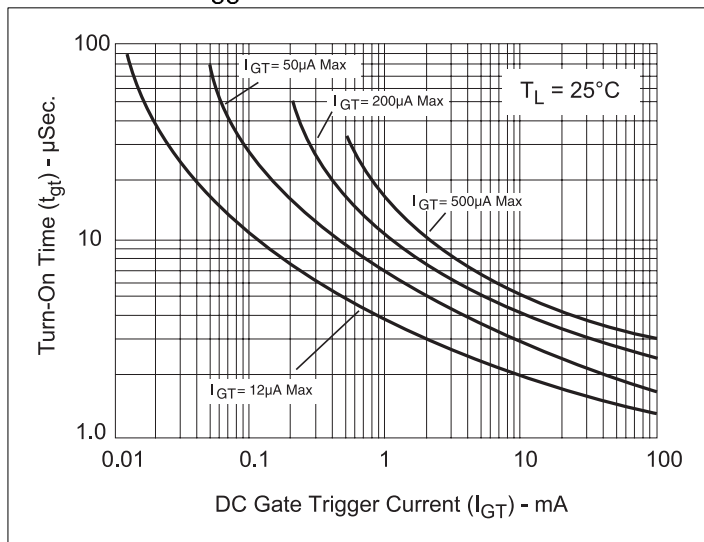


Figure 9: Power Dissipation (Typical) vs. RMS On-State Current.

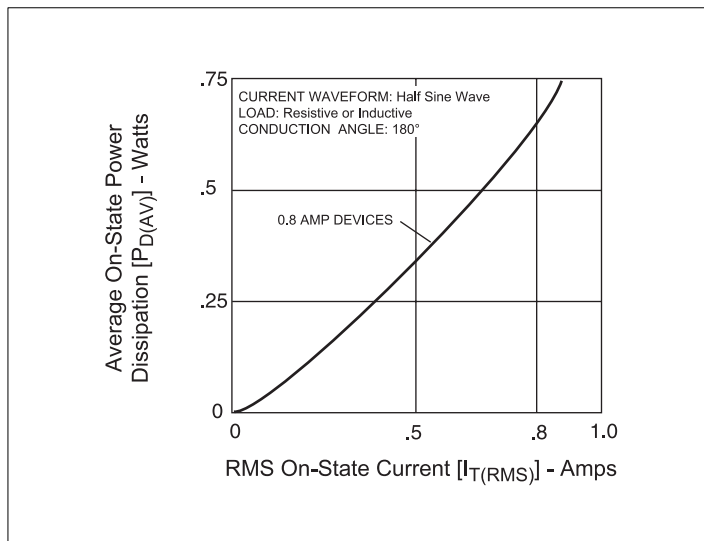


Figure 10: Peak Repetitive Sinusoidal Curve.

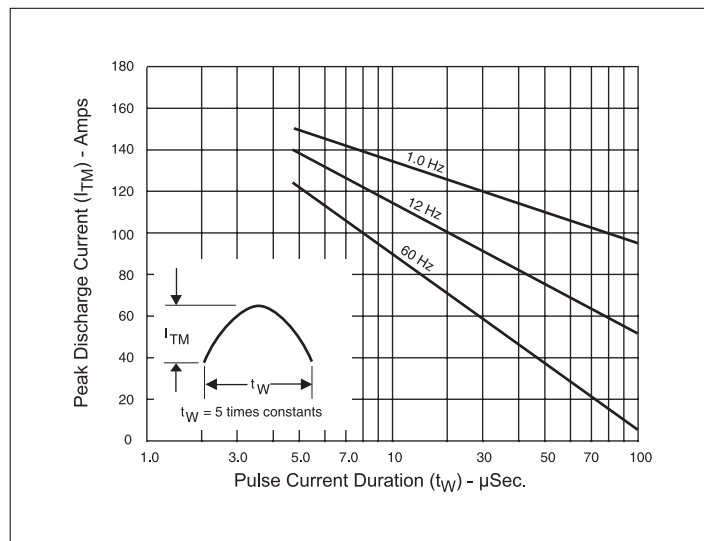
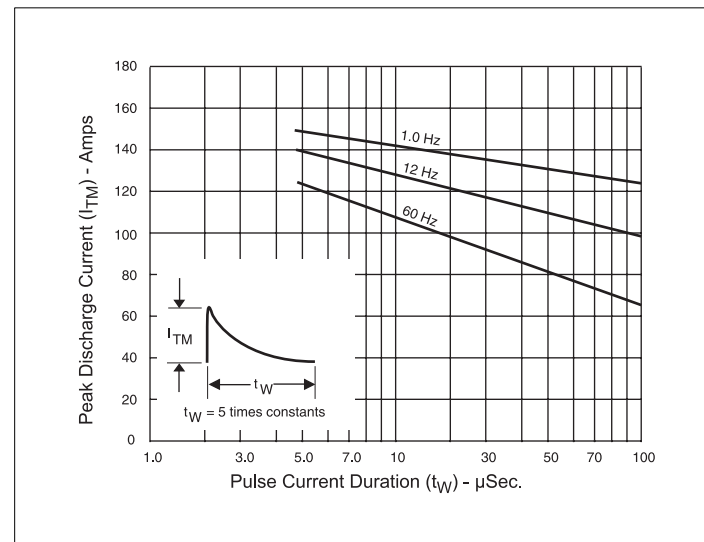
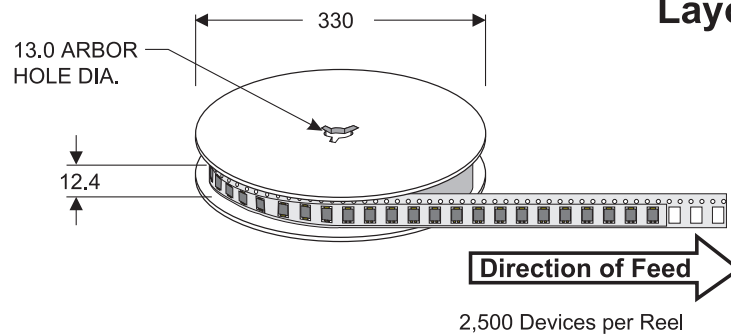
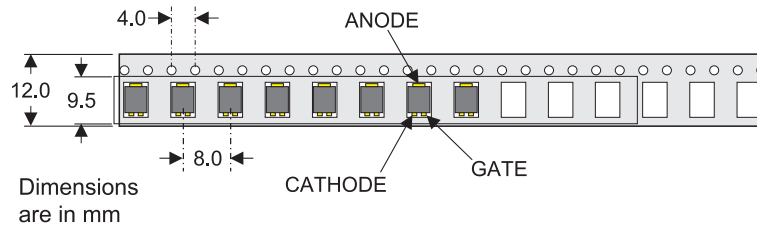


Figure 11: Peak Repetitive Capacitor Discharge Current.



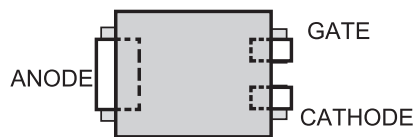
Embossed Carrier Packaging



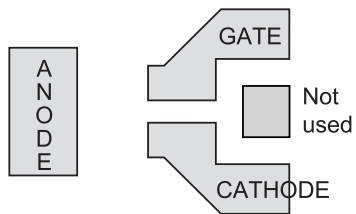
Component/Tape Layout

Standard Reel Pack (RP) for COMPAK (C Package).
Meets all EIA-481-1 Standards.

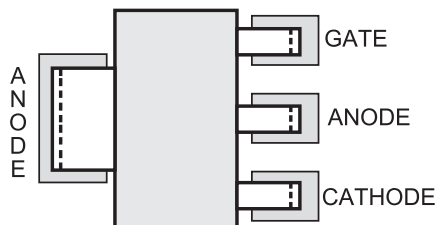
Footprint Dimensions



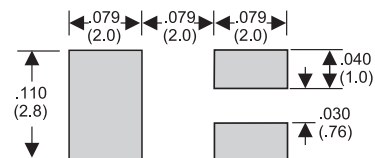
COMPACT Footprint



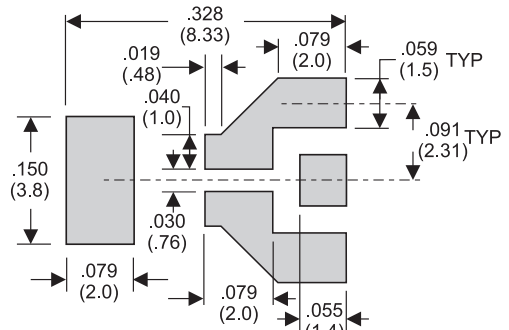
Footprint for either COMPACT or SOT-223



SOT-223 Footprint



PAD OUTLINE (MM)



DUAL PAD OUTLINE (MM)

New 3-leaded COMPACT package makes more board space available. The COMPACT's footprint is less than half that of the older SOT-223, yet package interchangeability is maintained with proper mounting pad placement.

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Please contact the factory for further information.

Data Sheet: Sen.SCR-0.8
July, 1998



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