SDG1203 Series OC-48 Optical Transceiver

with Mux / Demux (16x155.52Mbps)

Features

- **2.488Gbps High Speed Optical I/F**
- **SONET / SDH Compliant**
- **155.52Mbps LVPECL I/F**
- **Pigtailed Compact Package**
- **Single +3.3V Operation**
- **Optical Transmitter Disable**
- **LD Bias Current Monitor**
- **Optical Receiver Loss of Signal Alarm**
- **Multi Sourced Footprint Product**

General Description

The SDG1203 2.5Gb/s Optical Transceiver is a fully integrated SONET OC-48 photonic layer transceiver including serialization and deserialization function of section layer of SONET/SDH. The SDG1203 converts a 16bit 155.52Mb/s parallel electrical data stream to a 2.48832Gb/s optical data signal and a 2.48832Gb/s optical data signal to a 16bit 155.52Mb/s parallel electrical data stream. This SONET/SDH compliant Optical Interface is suitable for SONET/SDH equipment as well as other high-speed data communication equipment. The 16bit LVPECL interface is compatible with CMOS Framer and Mapper chipset.

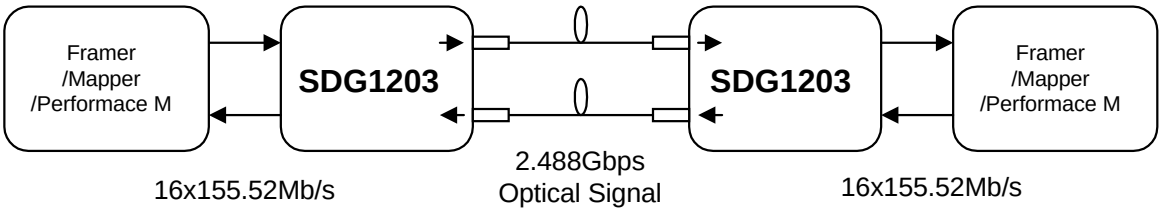


Figure 1. Application Block Diagram

1. SDG1203 Functional Block Diagram

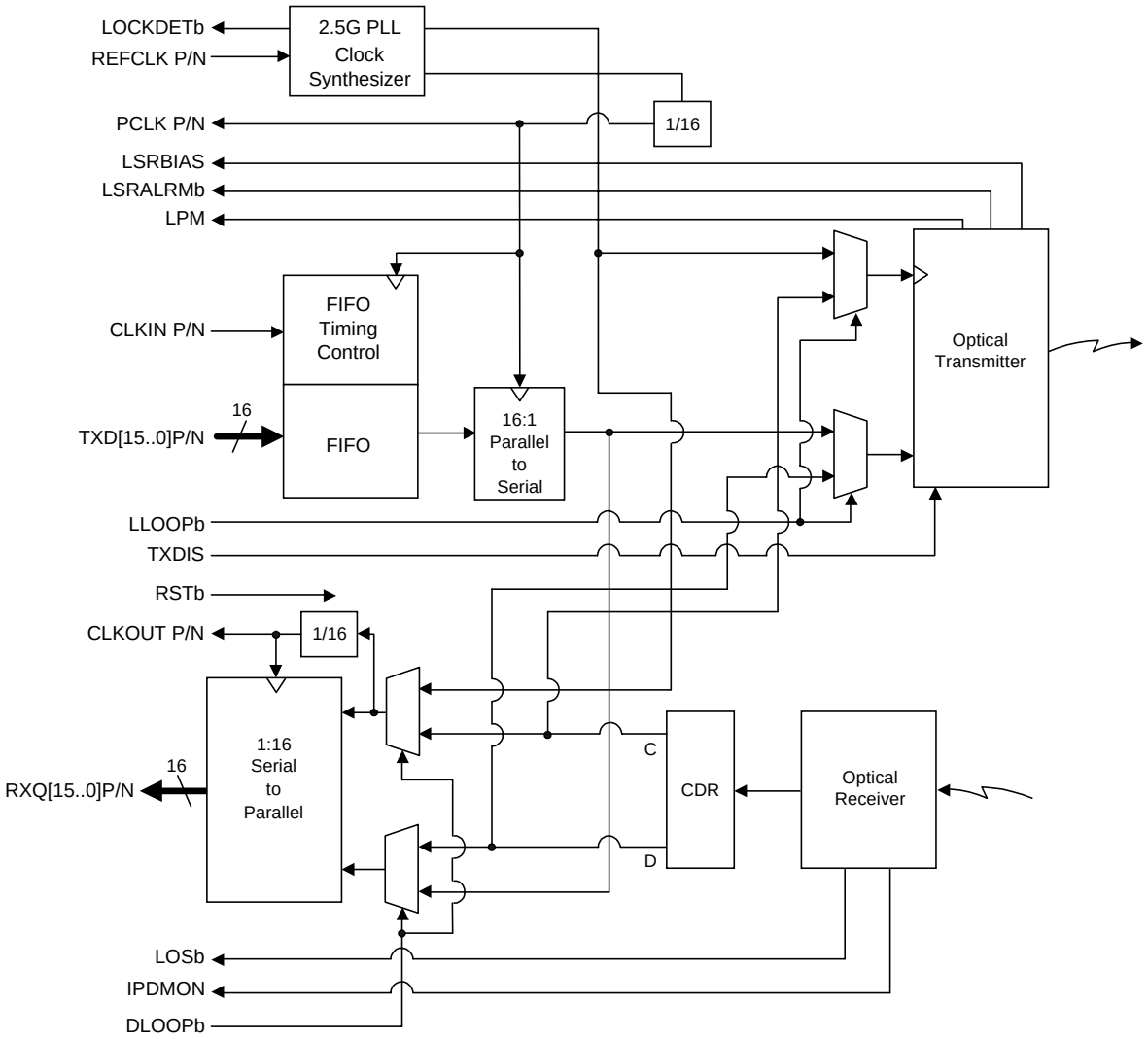
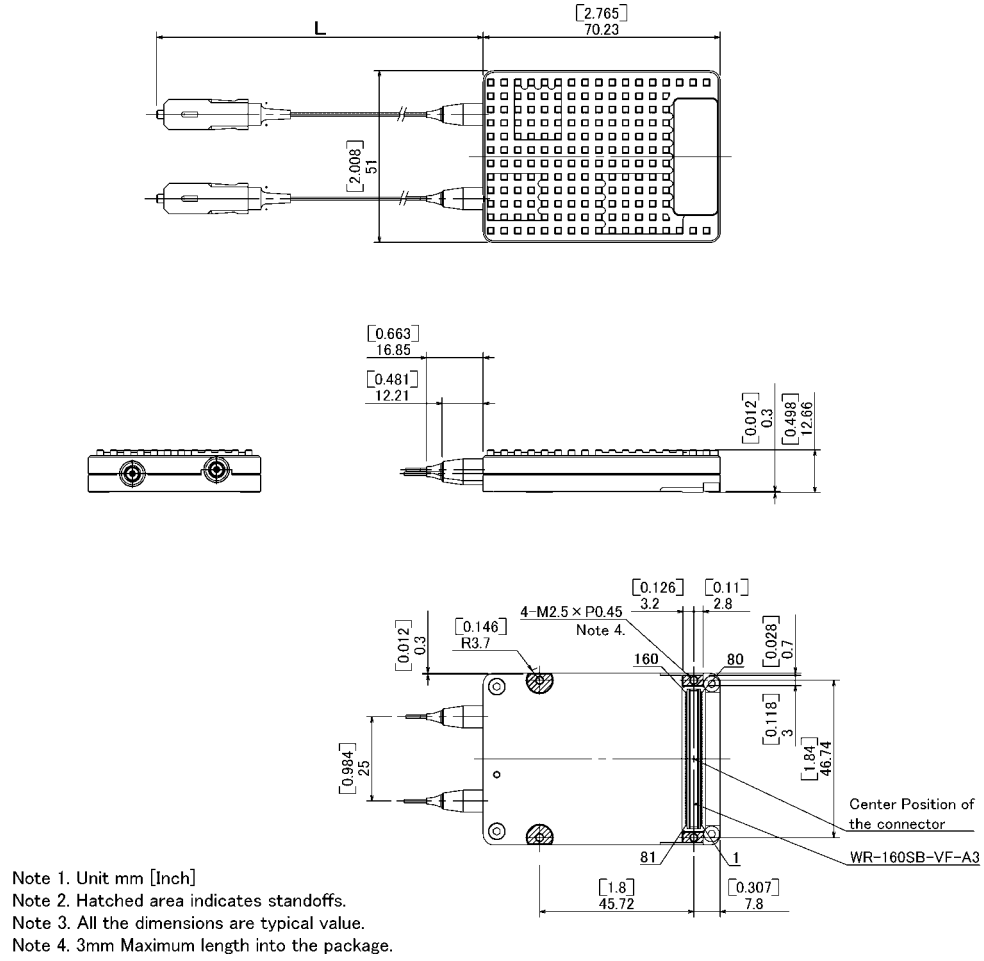


Figure 2. SDG1203 Functional Block Diagram

2. Package Dimension



Note 1. Unit mm [Inch]
Note 2. Hatched area indicates standoffs.
Note 3. All the dimensions are typical value.
Note 4. 3mm Maximum length into the package.

Figure 3. Package Dimension

Board Connector(Module side): 160-PIN JAE Connector P/N : WR-160SB-VF-A3

Mates with WR-160PB-VF50-A3 (PCB side)

Table 1. Fiber Pigtail and Optical Connector

Parameter	Min	Typ	Max	Unit
Fiber Type		Single Mode Fiber		
Outer Jacket Diameter		0.9		mm
Fiber Clad Diameter		125		µm
Mode Field Diameter		9.5		µm
Fiber Bending Radius	25.4			mm
Pigtail Length (“L” in figure 2)	900	1000	1100	mm
Connector Optical Reflectance			-45	dB

3. Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	+85	degC	
Operating Case Temperature	Topcn	-5	70	degC	1
Operating Case Temperature	Topcw	-40	+80	degC	2
Relative Humidity (no condensing)	RH	5	85	%	
Supply Voltage	Vccmdm	0	+3.6	V	
with respect to GND	Vcctx	0	+3.6	V	
	Vccrx	0	+3.6	V	
Voltage on LVPECL Input	Vlvpi	0	Vccmdm	V	
Source Current on LVPECL Output	Ilvpo	0	24	mA	
Voltage on LVTTL Input	Vlvti	0	Vccmdm	V	
Receiver Optical Input Power					
PIN Receiver	Pinpin		+2	dBm	3
APD Receiver	Pinapd		-3	dBm	4

Note:

1: Standard Operating Temperature (N version)

2: Extended Operation Temperature (W version)

3: Applied for SR/I-16 (N1) and IR-1/S16.1(S1) application

4: Applied for LR-1/L-16.1 (L1) and LR-2/L-16.2 (L2) application

4. Pin Assignment and Description

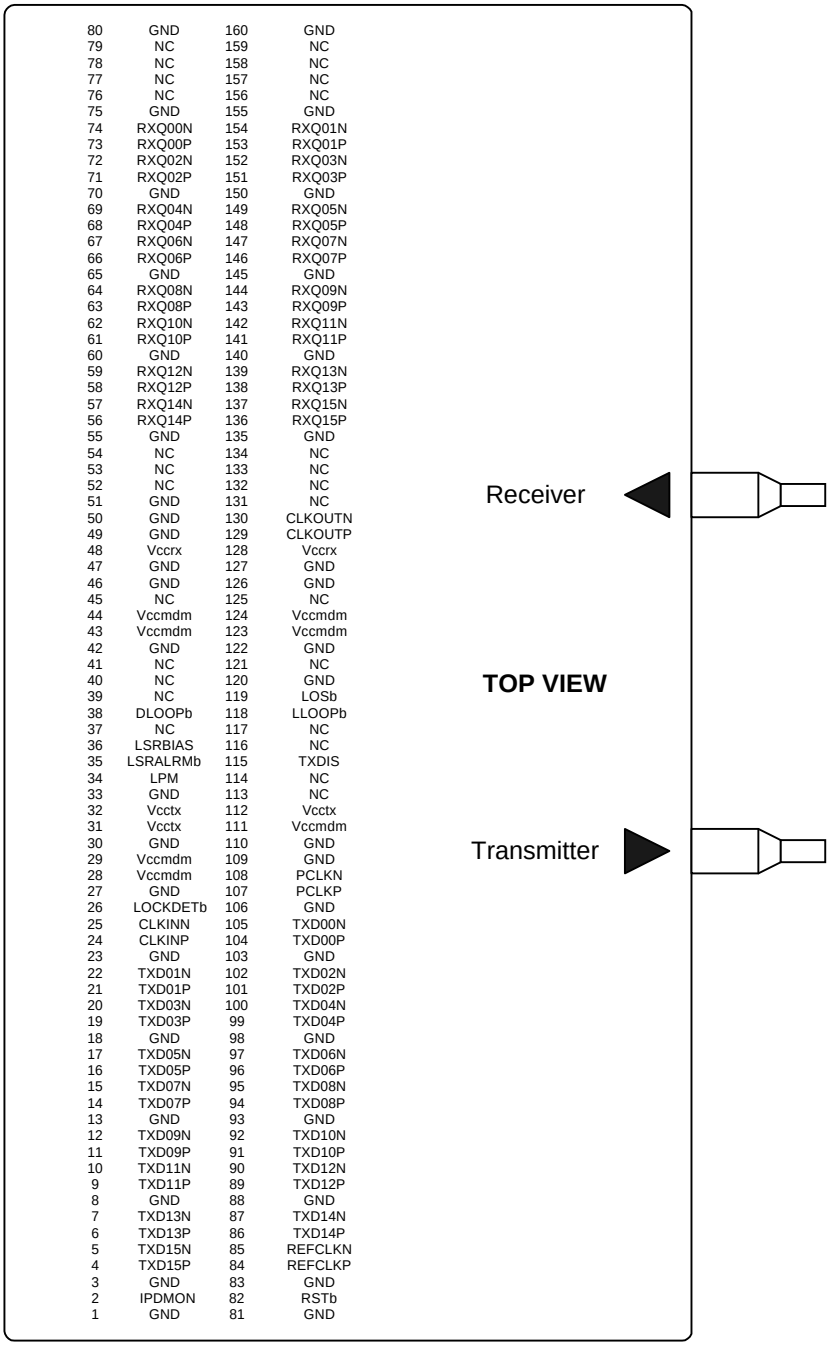


Figure 4. Pin Assignment

Table 3. Pin Assignment and Description (Transmitter Side)

Pin Name	I/O	Description	Pin #
TXD00 P/N	I (LVPECL)	Transmitter parallel data input, Differential LVPECL interface. TXD15 P/N is the Most Significant Bit and transmitted first followed by the subsequent bits with the TXD00 P/N (Least Significant Bit), sampled on rising edge of CLKINP.	104/105
TXD01 P/N			21/22
TXD02 P/N			101/102
TXD03 P/N			19/20
TXD04 P/N			99/100
TXD05 P/N			16/17
TXD06 P/N			96/97
TXD07 P/N			14/15
TXD08 P/N			94/95
TXD09 P/N			11/12
TXD10 P/N			91/92
TXD11 P/N			9/10
TXD12 P/N			89/90
TXD13 P/N			6/7
TXD14 P/N			86/87
TXD15 P/N			4/5
CLKIN P/N	I (LVPECL)	155.52MHz Transmitter parallel clock input. Differential LVPECL. Interface. This clock should be synchronized to REFCLK P/N.	24/25
REFCLK P/N	I (LVPECL)	155.52MHz reference clock input for 2.5Gbps PLL CSU and CDR. Differential LVPECL interface. Internally ac-coupled and biased with 50ohm termination.	84/85
LPM	O (Analog V)	Transmitter Output Power Monitor Voltage. This output is set at 500mV for the nominal transmitter output.	34
LSRALRMb	O (LVTTL)	Transmitter Alarm, LVTTL interface. Low when Optical Output Power has degraded 3dB from its nominal power	35
LSRBIAS	O (Analog V)	Laser Bias Current Monitor Voltage. This output changes at the rate of 20mV/mA.	36
PCLK P/N	O (LVPECL)	155MHz Parallel Byte Clock Output generated from 2.5Gbps CSU. This clock signal can be used to synchronize the data transfer from a framer to the transceiver.	107/108
LOCKDETb	O (LVTTL)	Lock Detect Signal from the PLL of 2.5GHz CSU. Goes low when CSU PLL is locked	26
TXDIS	I (LVTTL)	Transmitter disable input. LVTTL interface. When input signal is High, transmitter will be shut off.	115

Table 4. Pin Assignment and Description (Receiver Side)

Pin Name	I/O	Description	Pin #
RXQ00 P/N	O (LVPECL)	Receiver parallel data output. Differential LVPECL interface. RXQ15 P/N is the Most Significant Bit and received first followed by the subsequent bits with RXQ00 P/N(Least Significant Bit), updated on the falling edge of CLKOUTP	73/74
RXQ01 P/N			153/154
RXQ02 P/N			71/72
RXQ03 P/N			151/152
RXQ04 P/N			68/69
RXQ05 P/N			148/149
RXQ06 P/N			66/67
RXQ07 P/N			146/147
RXQ08 P/N			63/64
RXQ09 P/N			143/144
RXQ10 P/N			61/62
RXQ11 P/N			141/142
RXQ12 P/N			58/59
RXQ13 P/N			138/139
RXQ14 P/N			56/57
RXQ15 P/N			136/137
CLKOUT P/N	O (LVPECL)	155.52MHz Receiver Parallel Clock Out. Differential LVPECL interface.	129/130
LOSb	O (LVTTL)	Loss of Signal. LVTTL interface. A low of this output indicates a loss of signal.	119
IPDMON	O (Analog I)	Receiver optical input power monitor. Analog current source interface.	2

Table 5. Pin Assignment and Description (Supply and Common)

Pin Name	I/O	Description	Pin #
RSTb	I (LVTTL)	Master reset signal for the internal logic IC. Low to reset.	82
DLOOPb	I (LVTTL)	Diagonostic Loopback Enable. LVTTL interface. When a logic low on this input, parallel data to the transmitter will be looped back to the receiver parallel output.	38
LLOOPb	I (LVTTL)	Line Loopback Enable. LVTTL interface. When a logic low on this input, received serial data is looped back to transmitter output.	118
Vccmdm	Supply (3.3V)	+3.3V power supply for Digital Circuit	28, 29, 43, 44, 111, 123, 124
Vcctx	Supply (3.3V)	+3.3V power supply for optical Transmitter	31, 32, 112
Vccrx	Supply (3.3V)	+3.3V power supply for optical Receiver	48, 128
GND	GND	Ground	1, 3, 8, 13, 18, 23, 27, 30,33, 42, 46, 47, 49, 50, 51, 55, 60, 65, 70, 75, 80, 81, 83, 88, 93, 98, 103, 106, 109, 110, 120, 122,126, 127, 135, 140, 145, 150, 155, 160
NC	-	Not connected internally, reserved for future options	137, 39, 40, 41, 45, 52, 53, 54, 76, 77, 78, 79, 113, 114, 116, 117, 121, 125, 131, 132, 133, 134, 156, 157, 158, 159

Table 6. Pin Assignment (Pin#1 - #80)

Pin#	Pin Name	I/O	Logic	Description	Pin#	Pin Name	I/O	Logic	Description
1	GND	Supply	GND	Ground	41	NC	-	-	Internally N.C.
2	IPDMON	O	Analog I	PD Current Monitor	42	GND	Supply	GND	Ground
3	GND	Supply	GND	Ground	43	Vccmdm	Supply	3.3V	Supply for MUX/DEMUX
4	TXD15P	I	LVPECL	Tx Data Input	44	Vccmdm	Supply	3.3V	Supply for MUX/DEMUX
5	TXD15N	I	LVPECL	Tx Data Input	45	NC	-	-	Internally N.C.
6	TXD13P	I	LVPECL	Tx Data Input	46	GND	Supply	GND	Ground
7	TXD13N	I	LVPECL	Tx Data Input	47	GND	Supply	GND	Ground
8	GND	Supply	GND	Ground	48	Vccrx	Supply	3.3V	Supply for ORX
9	TXD11P	I	LVPECL	Tx Data Input	49	GND	Supply	GND	Ground
10	TXD11N	I	LVPECL	Tx Data Input	50	GND	Supply	GND	Ground
11	TXD09P	I	LVPECL	Tx Data Input	51	GND	Supply	GND	Ground
12	TXD09N	I	LVPECL	Tx Data Input	52	NC	-	-	Internally N.C.
13	GND	Supply	GND	Ground	53	NC	-	-	Internally N.C.
14	TXD07P	I	LVPECL	Tx Data Input	54	NC	-	-	Internally N.C.
15	TXD07N	I	LVPECL	Tx Data Input	55	GND	Supply	GND	Ground
16	TXD05P	I	LVPECL	Tx Data Input	56	RXQ14P	O	LVPECL	Rx Data Output
17	TXD05N	I	LVPECL	Tx Data Input	57	RXQ14N	O	LVPECL	Rx Data Output
18	GND	Supply	GND	Ground	58	RXQ12P	O	LVPECL	Rx Data Output
19	TXD03P	I	LVPECL	Tx Data Input	59	RXQ12N	O	LVPECL	Rx Data Output
20	TXD03N	I	LVPECL	Tx Data Input	60	GND	Supply	GND	Ground
21	TXD01P	I	LVPECL	Tx Data Input	61	RXQ10P	O	LVPECL	Rx Data Output
22	TXD01N	I	LVPECL	Tx Data Input	62	RXQ10N	O	LVPECL	Rx Data Output
23	GND	Supply	GND	Ground	63	RXQ08P	O	LVPECL	Rx Data Output
24	CLKINP	I	LVPECL	Tx Clock Input	64	RXQ08N	O	LVPECL	Rx Data Output
25	CLKINN	I	LVPECL	Tx Clock Input	65	GND	Supply	GND	Ground
26	LOCKDETb	O	LVTTL		66	RXQ06P	O	LVPECL	Rx Data Output
27	GND	Supply	GND	Ground	67	RXQ06N	O	LVPECL	Rx Data Output
28	Vccmdm	Supply	3.3V	Supply for MUX/DEMUX	68	RXQ04P	O	LVPECL	Rx Data Output
29	Vccmdm	Supply	3.3V	Supply for MUX/DEMUX	69	RXQ04N	O	LVPECL	Rx Data Output
30	GND	Supply	GND	Ground	70	GND	Supply	GND	Ground
31	Vcctx	Supply	33V	Supply for OTX	71	RXQ02P	O	LVPECL	Rx Data Output
32	Vcctx	Supply	3.3V	Supply for OTX	72	RXQ02N	O	LVPECL	Rx Data Output
33	GND	Supply	GND	Ground	73	RXQ00P	O	LVPECL	Rx Data Output
34	LPM	O	Analog V	Laser power monitor	74	RXQ00N	O	LVPECL	Rx Data Output
35	LSRALMb	O	LVTTL	Lase fault alarm	75	GND	Supply	GND	Ground
36	LSRBIAS	O	Analog V	Laser bias current monito	76	NC	-	-	Internally N.C.
37	NC	-	-	Internally N.C.	77	NC	-	-	Internally N.C.
38	DLOOPb	I	LVTTL	Diagonostic Loopback	78	NC	-	-	Internally N.C.
39	NC	-	-	Internally N.C.	79	NC	-	-	Internally N.C.
40	NC	-	-	Internally N.C.	80	GND	Supply	GND	Ground

Table 7. Pin Assignment (Pin#81 - #160)

Pin#	Pin Name	I/O	Logic	Description	Pin#	Pin Name	I/O	Logic	Description
81	GND	Supply	GND	Ground	121	NC	-	-	Internally N.C.
82	RSTb	I	LVTTL	Master Reset	122	GND	Supply	GND	Ground
83	GND	Supply	GND	Ground	123	Vccmdm	Supply	3.3V	Supply for MUX/DEMUX
84	REFCLKP	I	LVPECL	RefClk input	124	Vccmdm	Supply	3.3V	Supply for MUX/DEMUX
85	REFCLK	I	LVPECL	RefClk input	125	NC	-	-	Internally N.C.
86	TXD14P	I	LVPECL	Tx Data Input	126	GND	Supply	GND	Ground
87	TXD14N	I	LVPECL	Tx Data Input	127	GND	Supply	GND	Ground
88	GND	Supply	GND	Ground	128	Vccrx	Supply	3.3V	Supply for ORX
89	TXD12P	I	LVPECL	Tx Data Input	129	CLKOUTP	O	LVPECL	Rx Clock Output
90	TXD12N	I	LVPECL	Tx Data Input	130	CLKOUTN	O	LVPECL	Rx Clock Output
91	TXD10P	I	LVPECL	Tx Data Input	131	NC	-	-	Internally N.C.
92	TXD10N	I	LVPECL	Tx Data Input	132	NC	-	-	Internally N.C.
93	GND	Supply	GND	Ground	133	NC	-	-	Internally N.C.
94	TXD08P	I	LVPECL	Tx Data Input	134	NC	-	-	Internally N.C.
95	TXD08N	I	LVPECL	Tx Data Input	135	GND	Supply	GND	Ground
96	TXD06P	I	LVPECL	Tx Data Input	136	RXQ15P	O	LVPECL	Rx Data Output
97	TXD06N	I	LVPECL	Tx Data Input	137	RXQ15N	O	LVPECL	Rx Data Output
98	GND	Supply	GND	Ground	138	RXQ13P	O	LVPECL	Rx Data Output
99	TXD04P	I	LVPECL	Tx Data Input	139	RXQ13N	O	LVPECL	Rx Data Output
100	TXD04N	I	LVPECL	Tx Data Input	140	GND	Supply	GND	Ground
101	TXD02P	I	LVPECL	Tx Data Input	141	RXQ11P	O	LVPECL	Rx Data Output
102	TXD02N	I	LVPECL	Tx Data Input	142	RXQ11N	O	LVPECL	Rx Data Output
103	GND	Supply	GND	Ground	143	RXQ09P	O	LVPECL	Rx Data Output
104	TXD00P	I	LVPECL	Tx Data Input	144	RXQ09N	O	LVPECL	Rx Data Output
105	TXD00N	I	LVPECL	Tx Data Input	145	GND	Supply	GND	Ground
106	GND	Supply	GND	Ground	146	RXQ07P	O	LVPECL	Rx Data Output
107	PCLKP	O	LVPECL	Counter Clock Output	147	RXQ07N	O	LVPECL	Rx Data Output
108	PCLKN	O	LVPECL	Counter Clock Output	148	RXQ05P	O	LVPECL	Rx Data Output
109	GND	Supply	GND	Ground	149	RXQ05N	O	LVPECL	Rx Data Output
110	GND	Supply	GND	Ground	150	GND	Supply	GND	Ground
111	Vccmdm	Supply	3.3V	Supply for MUX/DEMUX	151	RXQ03P	O	LVPECL	Rx Data Output
112	Vcctx	Supply	3.3V	Supply for OTX	152	RXQ03N	O	LVPECL	Rx Data Output
113	NC	-	-	Internally N.C.	153	RXQ01P	O	LVPECL	Rx Data Output
114	NC	-	-	Internally N.C.	154	RXQ01N	O	LVPECL	Rx Data Output
115	TXDIS	I	LVTTL	OTX Disable	155	GND	Supply	GND	Ground
116	NC	-	-	Internally N.C.	156	NC	-	-	Internally N.C.
117	NC	-	-	Internally N.C.	157	NC	-	-	Internally N.C.
118	LLOOPb	I	LVTTL	Line Loopback	158	NC	-	-	Internally N.C.
119	LOSb	O	LVTTL	Los of power	159	NC	-	-	Internally N.C.
120	GND	Supply	GND	Ground	160	GND	Supply	GND	Ground

5. Electrical Interface

5-1. DC Characteristics

Table 8. DC Characteristics

Parameter		Sym.	Min	Typ	Max	Unit	Note
Supply Voltage		Vcc33	3.135	3.3	3.465	V	
Supply Current	(Vccmdm)	Iccmdm		650	800	mA	1
	(Vcctx)	Icctx		300	550	mA	1
	(Vccrx)	Iccrx		100	300	mA	1
Total Power Consumption		Ptotal		4.5	6.5	W	
LVPECL Input Voltage	(low)	Vilvpl	Vcc-2.00		Vcc-1.40	V	2
	(high)	Vilvph	Vcc-1.25		Vcc-0.55	V	2
LVPECL diff. Input Swing		dVindiff	500		2000	mV	
LVPECL Output Voltage	(low)	Volvpl	Vcc-1.88		Vcc-1.44	V	2, 3
	(high)	Volvph	Vcc-1.09		Vcc-0.83	V	2, 3
LVPECL diff. Output Swing		dVoutdiff	1000		1600	mV	3
LVTTL Output Voltage	(low)	Vottll			0.5	V	
	(high)	Vottlh	2.4			V	
LVTTL Input Voltage	(low)	Vilvttll	0		0.8	V	
	(high)	Vilvttlh	2		3.465	V	
LPM Voltage		Vlpm	0.25	0.5	0.75	V	
LSBIAS Voltage		Vldbmon	19	20	21	V/A	4
IPDMON Output Current (PIN Receiver)	0dBm	Ipdmon		7.5		mA	
	-10dBm			0.75			
	-20dBm			0.075			
IPDMON Output Current (APD Receiver)	-10dBm	Ipdmon		2.5		mA	
	-20dBm			0.45			
	-30dBm			0.075			

Note:

1. Output Current is not included.
2. Shall be applied for both single-ended and differential LVPECL Input,
   Differential LVPECL Input shall have same DC characteristics as single-ended LVPECL.
3. with 50ohm AC coupled load
4. Vldbmon=20x(LD bias current)

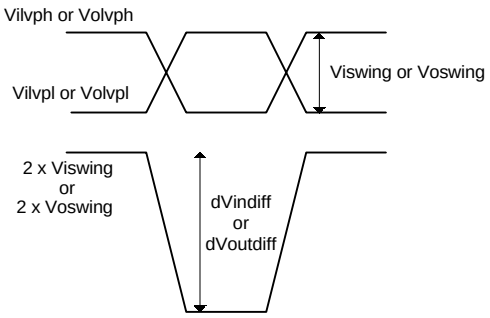


Figure 5. Definition of dV

5-2. Transmitter AC Characteristics

Table 9. Transmitter AC Timing Characteristics

Parameter		Sym.	Min	Typ	Max	Unit	Note
CLKIN Frequency		Fclkin		155.520		MHz	
CLKIN Tolerance		dFclkin	-50		+50	ppm	
REFCLK Input Jitter		Jitterin			1	ps RMS	1
CLKIN Duty Cycle		dcin	40		60	%	
CLKIN Acquisition Time		Tpllaqs			TBD	ms	2
CLKIN Rise/Fall Time		Trc/Tfc			1.5	ns	
TXD Rise /Fall Time		Trd/Tfd			1.5	ns	
Skew drift CLKIN vs PCLK		Tsd	-5		5	ns	3
CLKIN/TXD Alignment	setup	Tiset	1.5			ns	4
	hold	Tihold	0.5			ns	4
TXDIS Response Time	Off	Ttxoff			100	µs	
	On	Ttxon			3	ms	

Note:

1: Jitter frequency range: 12kHz to 10MHz

2: Please refer to Figure 6.

3: After the FIFO is initialized.

4: with respect to the falling edge of CLK_IN

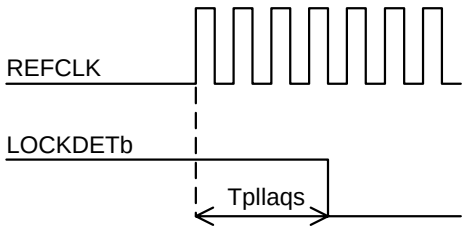


Figure 6. PLL Acquisition Timing

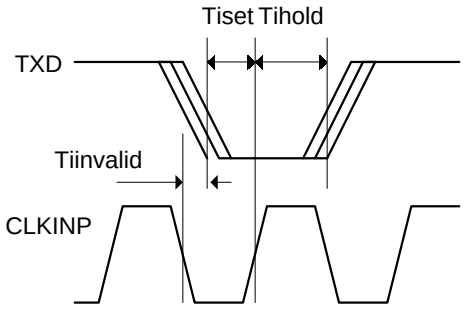


Figure 7. Transmitter Input Timing

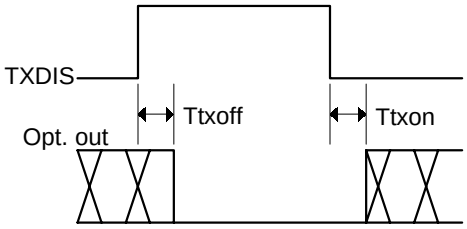


Figure 8. Transmitter Disable Response

5-3. Receiver AC Characteristics

Table 10. Receiver AC Timing Characteristics

Parameter		Sym.	Min	Typ	Max	Unit	Note
CLKOUT Frequency		Fclko		155.520		MHz	
CLKOUT Tolerance		dFclko	-100		+100	ppm	1
CLKOUT Duty Cycle		dco	45		55	%	
CLK Acquisition Time		Tpllaqs			250	µs	2
CLKOUT Rise/Fall Time		Trc/Tfc			1.5	ns	
RXQ Rise /Fall Time		Trd/Tfd			1.5	ns	
CLKOUT/RXQ Alignment	invalid	Toinvalid	-1.8		+1.8	ns	3
	setup	Toset	2.2			ns	4
	hold	Tohold	2			ns	4
LOSb Response Time		Tlightoff	2.3		100	µs	
		Tlighton	2.3		100	µs	

Note:

1: Depends on an optical input signal.

2: After receiving optical signal.

3: with respect to the falling edge of CLK_OUT

4: with respect to the rising edge of CLK_OUT

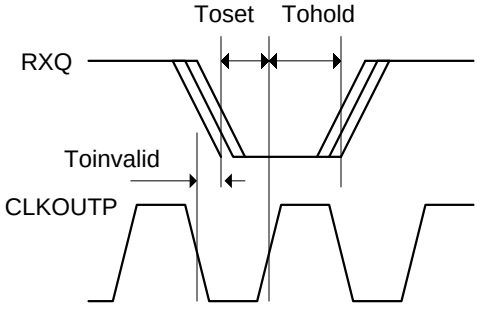


Figure 9. Receiver Output Timing

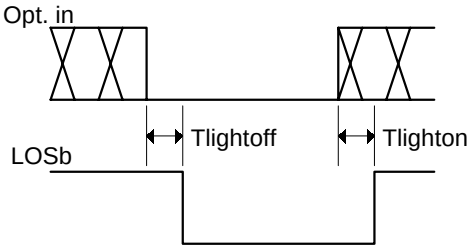


Figure 10. LOSb Response Time

6. Optical Interface

6-1. Transmitter Optical Interface Characteristics

Table 11. Transmitter Optical Interface

Parameter	Sym.	Min	Typ	Max	Unit	Note
Center Wavelength	Lc1	1266		1360	nm	1, 2
	Lc2	1260		1360	nm	1, 3
	Lc3	1280		1335	nm	1, 4
	Lc4	1500		1580	nm	1, 5
Spectral Width RMS	dL	0		4.0	nm	1, 2
Spectral Width -20dB	dL			1	nm	1, 3, 4, 5
Side Mode Suppression Ratio	SSR	30			dB	1, 3, 4, 5
Optical Output Power ave.	Po	-10		-3	dBm	1, 2
Optical Output Power ave.	Po	0		-5	dBm	1, 3
Optical Output Power ave.	Po	-2		+3	dBm	1, 4, 5
Disabled Output Power	Pooff			-45	dBm	
Extinction Ratio	Er			8.2	dB	1
Optical Pulse Mask	-	Compliant with GR-253 and ITU-T G.957			-	6
Jitter Generation rms	Tjgrms	0		0.01	UIrms	7, 8
p-p	Tjgpp	0		0.1	UIp-p	7, 8

Note

1: 2.48832Gbps, PRBS 2^23-1

2: Applied for SR / I-16 application (1.3µmFP-LD)

3: Applied for IR-1/ S-16.1 application (1.3µm DFB-LD)

4: Applied for LR-1/ L-16.1 application (1.3µm DFB-LD)

5: Applied for LR-2/L-16.2 application (1.55µm DFB-LD)

6: Refer to Figure.11.

7: Measured with a bandpass filter having a high-pass cutoff frequency of 12kHz and a low-pass cutoff frequency of 20MHz

8: Input jitter shall not exceed the specified value in Table 5.

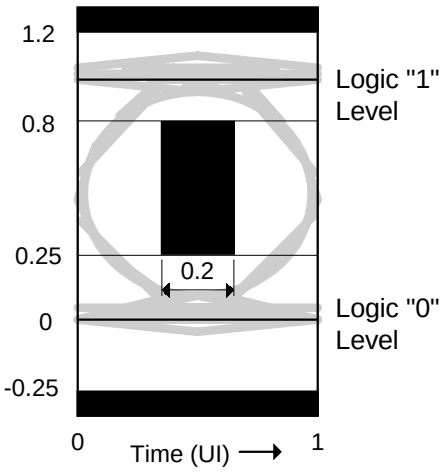


Figure 11. Transmitter Pulse Mask

6-2. Receiver Optical Interface Characteristics

Table 12. Receiver Optical Interface

Parameter		Sym.	Min	Typ	Max	Unit	Note
Input Center Wavelength		Lc	1265		1360	nm	1,2,3,4
Input Center Wavelength		Lc	1500		1580	nm	1, 5
Optical Input Power		Pin	-18		0	dBm	1,2,3
Optical Input Power		Pin	-28		-9	dBm	1,4,5
Receiver Power Penalty		Rpo			1		1,2,3,4
Receiver Power Penalty		Rpo			2		1, 5
Optical Reflectance		ORLr			-27	dB	
Jitter Tolerance		-	Compliant with GR-253 and ITU-T G958			-	6
LOS Input Power Level	->LOS	Plosd		-29	-22	dBm	1,2,3,7
	LOS->	Plosa		-27	-22	dBm	1,2,3,8
LOS Input Power Level	->LOS	Plosd		-36	-30	dBm	1,4,5,7
	LOS->	Plosa		-34	-30	dBm	1,4,5,8

Note:

1: 2.48832Gb/s, PRBS 2^23-1, BER<1x10^-10

2: Applied for SR / I-16 application (1.3μmFP-LD)

3: Applied for IR-1 / S-16.1 application (1.3μm DFB-LD)

4: Applied for LR-1/ L-16.1 application (1.3μm DFB-LD)

5: Applied for LR-2 /L-16.2 application (1.55μm DFB-LD)

6: 1dB power penalty with 15UIp-p from 10Hz to 600Hz, 1.5UIp-p from 6kHz to 100kHz and 0.15UIp-p from 1MHz and above.

7: Decreasing light input

8: Increasing light input

7. Recommended User Interface

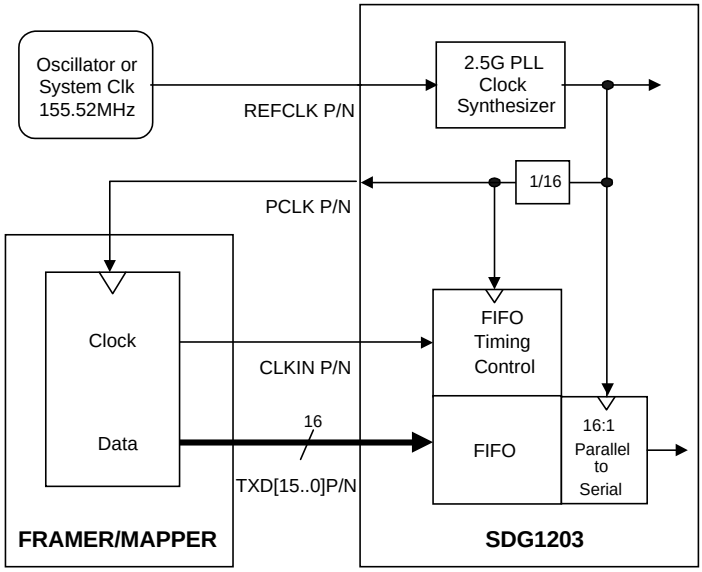


Figure 12. Transmitter input clocking scheme
(Synchronization between REFCLK and CLKIN)

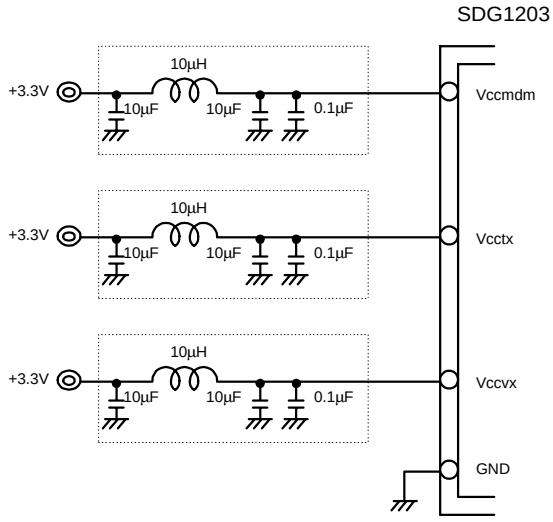


Figure 13. Power Filtering

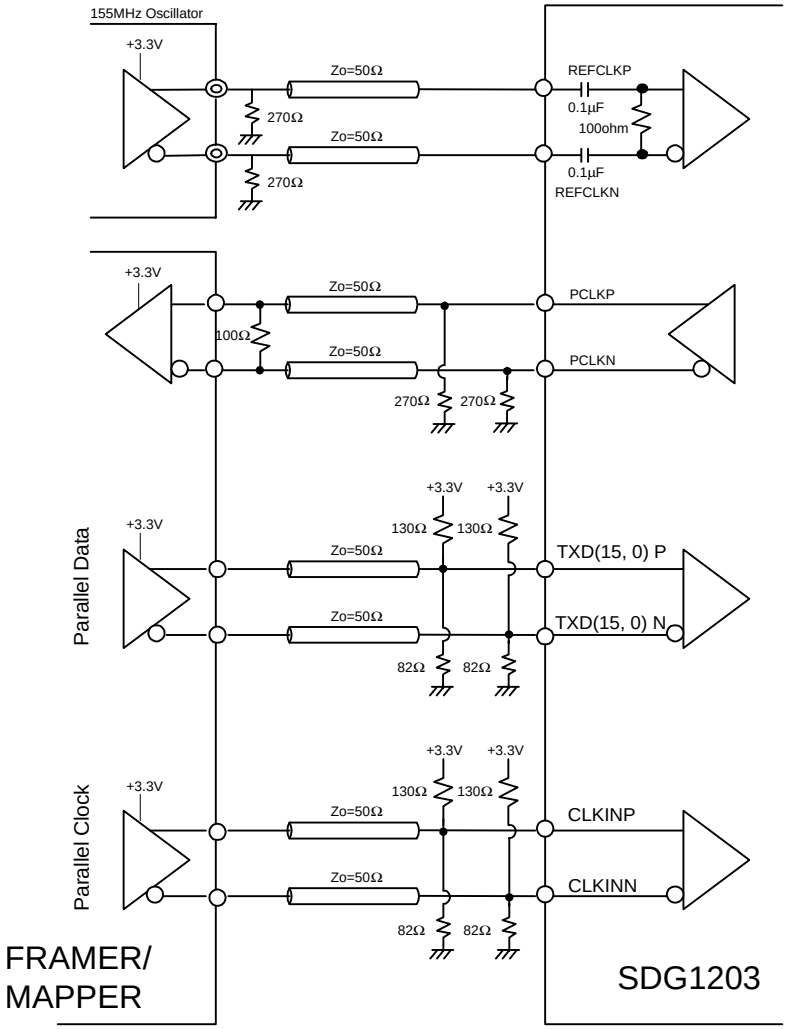


Figure 14 Transmitter LVPECL Interface

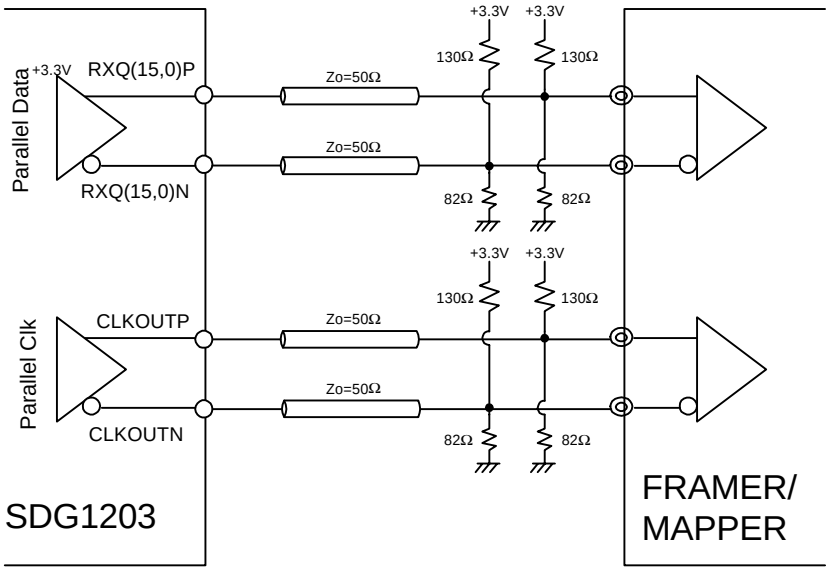


Figure 15 Receiver LVPECL Interface

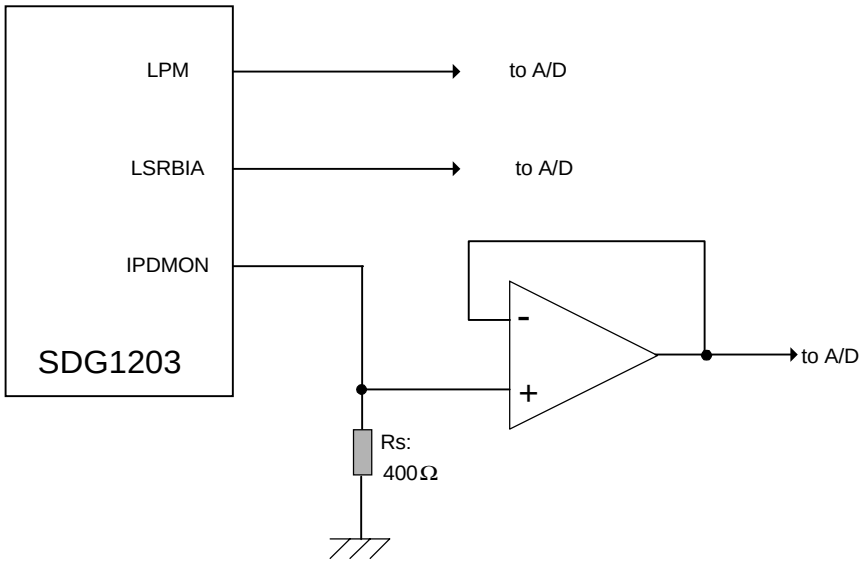
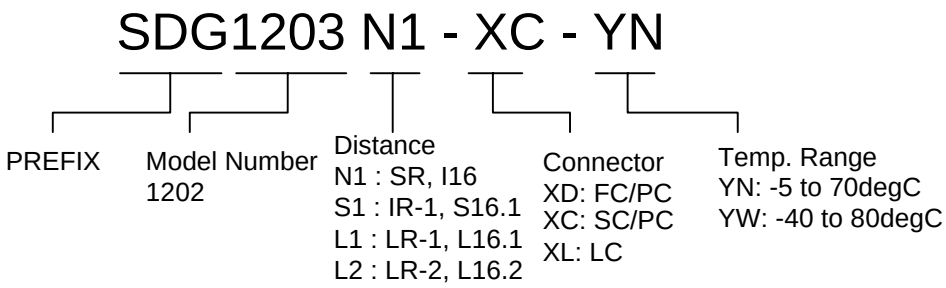


Figure 16. Analog Monitor Interface

8. Part Numbering Information



9. For More Information

JAPAN

Sumitomo Electric Industries, LTD. (International Business Division)

3-12 Moto-Akasaka 1-chome, Minato-ku, Tokyo 107-8468, Japan

Tel. +81-3-3423-5771

Fax. +81-3-3423-5099

Website: www.sei.co.jp/Electro-optic/index_e.html

E-mail: product-info@ppd.sei.co.jp

NORTH AMERICA

Excelight Communications, 4021 Stirrup Creek Drive, Suite 200 Durham, NC 27703

Tel. +1-919-361-1600 / Fax. +1-919-361-1619

Website: www.excelight.com

E-mail: info@excelight.com

EUROPE

Sumitomo Electric Europe, LTD.

220, Centennial Park, Elstree, Herts, WD6 3SL, United Kingdom

Tel. +44-208-953-8681

Fax. +44-208-207-5950

Website: www.sumielectric.com

E-mail: photonics@sumielectric.com