SFH6731/6732

Dual High-Speed 5.0 Mb/s Optocoupler

FEATURES

- **Data Rate 5 MBits/s (2.5 MBit/s over Temperature)**
- **Buffer**
- **Isolation Test Voltage, 5300 V_{RMS}**
- **TTL, LSTTL and CMOS Compatible**
- **Internal Shield for Very High Common Mode Transient Immunity**
- **Wide Supply Voltage Range (4.5 to 15 V)**
- **Low Input Current (1.6 mA to 5.0 mA)**
- **Specified from 0°C to 85°C**

APPLICATIONS

- **Industrial Control**
- **Replace Pulse Transformers**
- **Routine Logic Interfacing**
- **Motion/Power Control**
- **High Speed Line Receiver**
- **Microprocessor System Interfaces**
- **Computer Peripheral Interfaces**

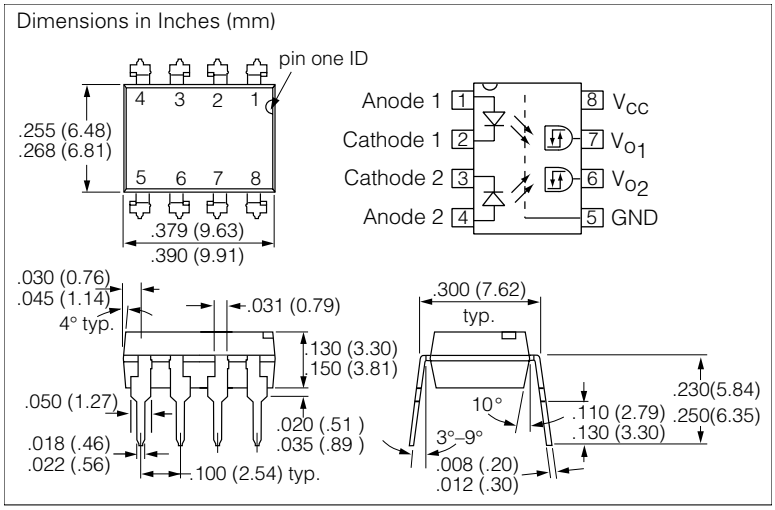
DESCRIPTION

The dual channel 5Mb/s SFH6731 and SFH6732 high speed optocoupler consists of a GaAlAs infrared emitting diode, optically coupled with an integrated photodetector. The detector incorporates a Schmitt-Trigger stage for improved noise immunity. A Faraday shield provides a common mode transient immunity of 1000 V/µs at V_{CM}=50 V for SFH6731 and 5000 V/µs at V_{CM}=300 V for SFH6732.

The SFH6731 and SFH6732 uses an industry standard DIP8 package. With standard lead bending, creepage distance and clearance of ≥7.0 mm with lead bending options 6, 7, and 9 ≥8.0 mm are achieved.

Truth Table SFH6731 and SFH6732 (Positive Logic)

IR Diode	Output
on	H
off	L



Maximum Ratings

Parameter		Sym.	Min.	Max.	Units
Emitter					
Reverse Voltage		V_R	—	3.0	V
DC Forward Current		I_F	—	10	mA
Surge Forward Current (tp≤1.0 µs, 300 pulses/s)		I_{FSM}	—	1.0	A
Total Power Dissipation		P_{tot}	—	20	mW
Detector					
Supply Voltage		V_{CC}	–0.5	15	V
Output Voltage		V_O	–0.5	15	V
Average Output Current		I_O	—	25	mA
Total Power Dissipation		P_{tot}	—	100	mW
Package					
Storage Temperature Range		T_{STG}	–55	125	°C
Ambient Temperature Range		T_A	–40	85	°C
Lead Soldering Temperature (t=10 sec.)		T_S	—	260	°C
Isolation Test Voltage (t=1 s)		V_{ISO}	5300	—	V_{RMS}
Pollution Degree		—	—	2.0	—
Creepage Distance and Clearance	Standard Lead Bending	—	7.0	—	mm
	Options 6, 7, 9	—	8.0	—	
Comparative Tracking Index per DIN IEC112/VDE 0303, part 1		—	175	400	—
Isolation Resistance	V_{IO}=500 V, T_A=25°C	R_{ISO}	10^{12}	—	Ω
	V_{IO}=500 V, T_A=100°C		10^{11}	—	

Recommended Operating Conditions

A 0.1 µF bypass capacitor connected between pins 5 and 8 must be used.

Parameter	Sym.	Min.	Max.	Unit
Supply Voltage	V_{CC}	4.5	15	V
Forward Input Current	I_{Fon}	1.6(1)	5.0	mA
Forward Input Current	I_{Foff}	–	0.1	mA
Operating Temperature	T_A	0	85	°C

1. We recommend using a 2.2 mA to permit at least 20% CTR degradation guard band.

Characteristics

0°C≤ T_A≤85°C; 4.5 V≤V_{CC}≤15 V; 1.6 mA≤I_{Fon}≤5 mA; 2.0≤V_{EH}≤15 V;
0≤ V_{EL}≤0.8 V; 0 mA≤I_{Foff}≤0.1 mA
Typical values: T_A=25°C; V_{CC}=5.0 V; I_{Fon}=3.0 mA unless otherwise specified

Parameter	Sym.	Min.	Typ.	Max.	Unit	Test Condition
Emitter						
Forward Voltage	V_F	—	1.6	1.75	V	I_F=5.0 mA, T_A=25°C
		—	—	1.8	V	I_F=5.0 mA
Input Current Hysteresis	I_{HYS}	—	0.1	—	mA	V_{CC}=5 V, I_{HYS}=I_{Fon}–I_{Foff}
Reverse Current	I_R	—	0.5	10	µA	V_R=3.0 V, T_A=25°C
Capacitance	C_0	—	60	—	pF	V_R=0 V, f=1 MHz, T_A=25°C
Thermal Resistance	R_{thJA}	—	700	—	K/W	—
Detector						
Logic Low Output Voltage	V_{OL}	—	—	0.5	V	I_{OL}=6.4 mA
Logic High Output Voltage	V_{OH}	2.4	*	—	V	I_{OH}=–2.6 mA, *V_{OH}=V_{CC}–1.8 V
Output Leakage Current (V_{OUT}>V_{CC})	I_{OHH}	—	0.5	100	µA	V_O=5.5 V, V_{CC}=4.5 V, I_F=5.0 mA
		—	1.0	500	µA	V_O=15 V, V_{CC}=4.5 V, I_F=5.0 mA
Logic Low Supply Current	I_{CCL}	—	3.7	6.0	mA	V_{CC}=5.5 V, I_F=0
		—	4.1	6.5	mA	V_{CC}=15 V, I_F=0
Logic High Supply Current	I_{CCH}	—	3.4	4.0	mA	V_{CC}=5.5 V, I_F=5.0 mA
		—	3.7	5.0	mA	V_{CC}=15 V, I_F=5.0 mA
Logic Low Short Circuit Output Current	I_{OSL}(2)	25	—	—	mA	V_O=V_{CC}=5.5 V, I_F=0
		40	—	—	mA	V_O=V_{CC}=15 V, I_F=0
Logic High Short Circuit Output Current	I_{OSH}(2)	—	—	–10	mA	V_{CC}=5.5 V, Vo=0 V, I_F=5.0 mA
		—	—	–25	mA	V_{CC}=15 V, Vo=0 V, I_F=5.0 mA
Thermal Resistance	R_{thJA}	—	300	—	K/W	—
Package						
Coupling Capacitance	C_{IO}	—	0.6	—	pF	f=1.0 MHz, pins 1–4 and 5–8 shorted together
Isolation Resistance	R_{ISO}	10^{12}	—	—	Ω	V_{IO}=500 V, T_A=25°C
		10^{11}	—	—	Ω	V_{IO}=500 V, T_A=100°C

2. Output short circuit time ≤10 ms.

Switching Times[3]

0° C≤ T_A≤85°C; 4.5 V≤V_{CC}≤15 V; 1.6 mA≤I_{Fon}≤5 mA; 0 mA≤I_{Foff}≤0.1 mA
Typical values: T_A=25°C; V_{CC}=5.0 V; I_{Fon}=3.0 mA unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Propagation Delay Time to Logic Low Output Level	t_{PHL}	—	120	—	ns	Without Peaking Capacitor
		—	115	300		With Peaking Capacitor
Propagation Delay Time to Logic Low Output Level	t_{PLH}	—	125	—	ns	Without Peaking Capacitor
		—	90	300		With Peaking Capacitor
Output Rise Time	t_r	—	40	—	ns	10% to 90%
Output Fall Time	t_f	—	10	—	ns	90% to 10%

Common Mode Transient Immunity T_A=25°C, V_{CC}=5 V[4]

Parameter	Device	Symbol	Min.	Unit	Test Condition
Logic High Common Mode Transient Immunity	SFH6731	$\|CM_H\|$[4]	1000	V/µs	$\|V_{CM}\|$=50 V, I_F=1.6 mA
	SFH6732		5000	V/µs	$\|V_{CM}\|$=300 V, I_F=1.6 mA
Logic Low Common Mode Transient Immunity	SFH6731	$\|CM_L\|$[4]	1000	V/µs	$\|V_{CM}\|$=50 V, I_F=0
	SFH6732		10000	V/µs	$\|V_{CM}\|$=1000 V, I_F=0

3. A 0.1 µF bypass capacitor connected between pins 5 and 8 must be used.
4. CM_H is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic high level (V_O>2.0 V).
   CM_L is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic low level (V_O<0.8 V).

Figure 1. Permissible total power dissipation vs. temperature

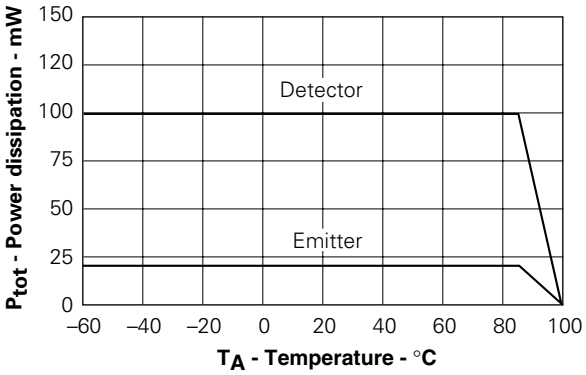


Figure 2. Typical input diode forward current vs. forward voltage

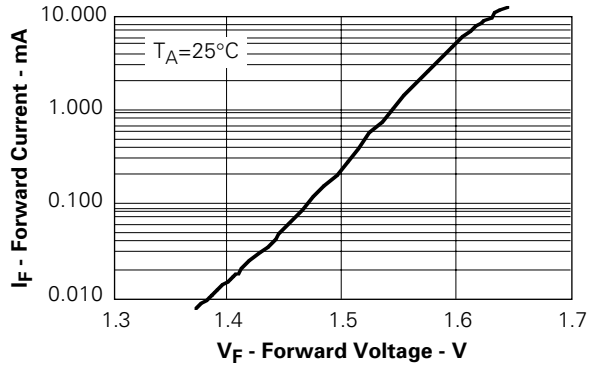


Figure 3. Typical forward input voltage vs. temperature

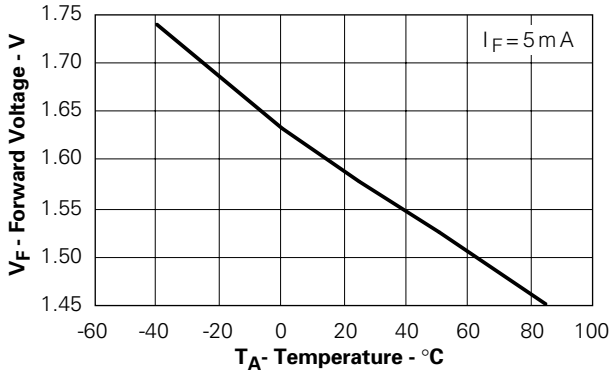


Figure 4. Typical output voltage vs. forward input current

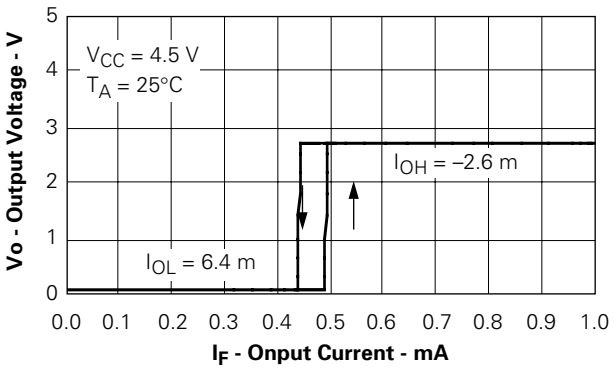


Figure 5. Typical supply current vs. temperature

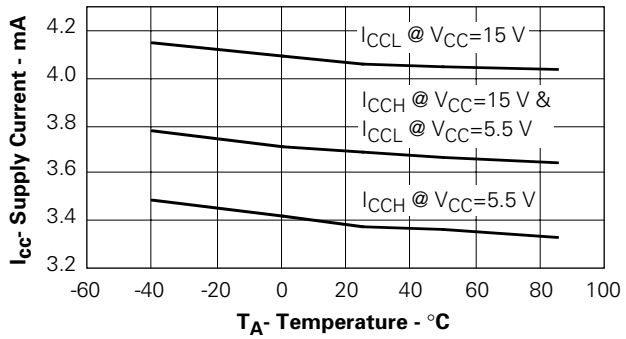


Figure 6. Typical output leakage current vs. temperature

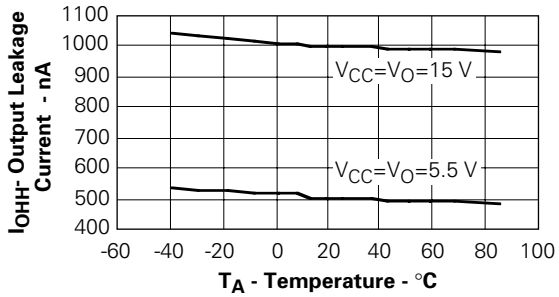


Figure 7. Typical low level output current vs. temperature

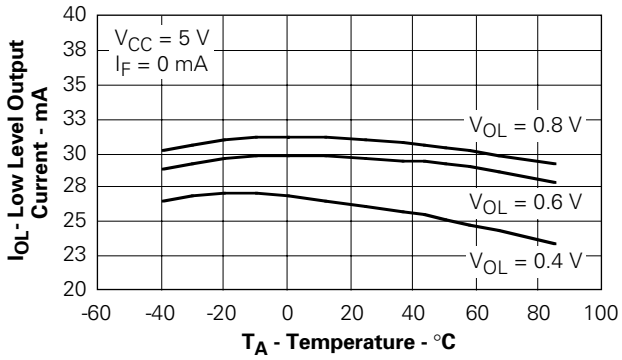


Figure 8. Typical low level output voltage vs. temperature

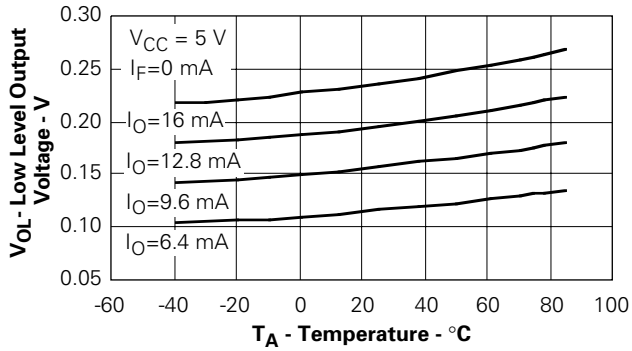


Figure 9. Typical high level output current vs. temperature

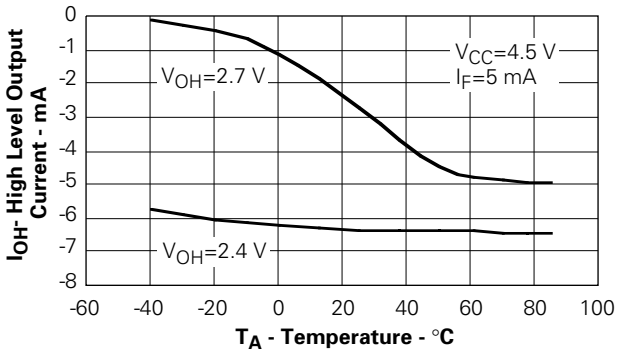


Figure 10. Typical rise, fall time vs. temperature

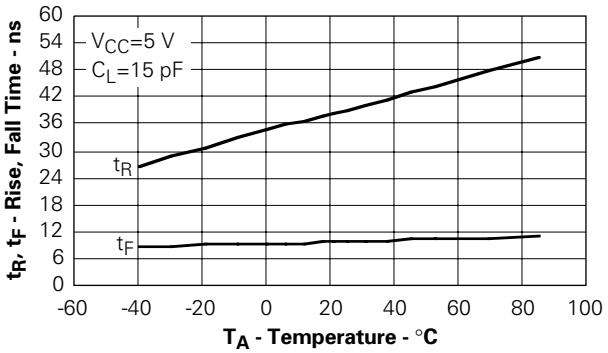


Figure 11. Typical propagation delays to logic high vs. temperature

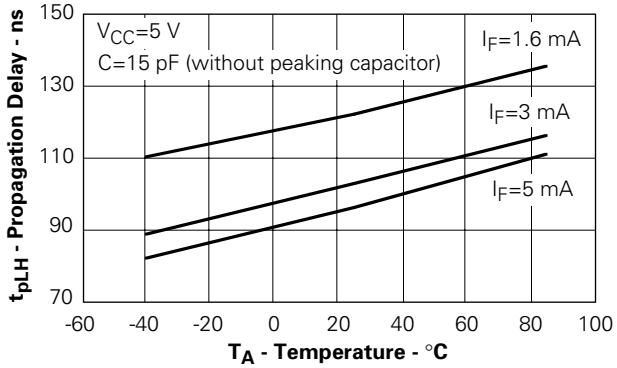


Figure 12. Typical propagation delays to logic low vs. temperature

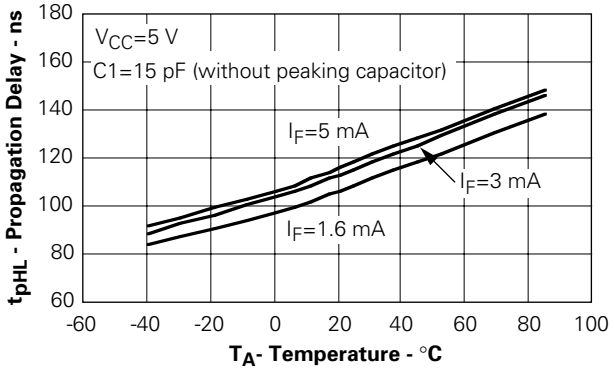


Figure 13. Typical propagation delays to logic high vs. temperature

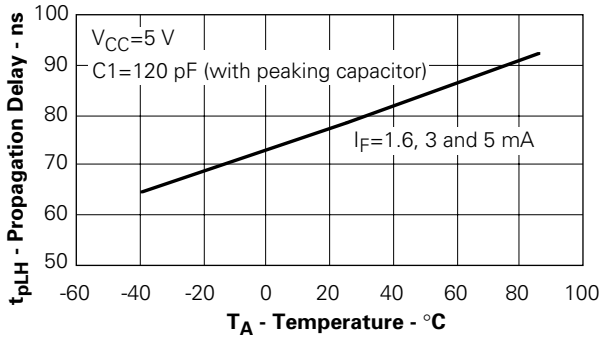


Figure 14. Typical propagation delays to logic low vs. temperature

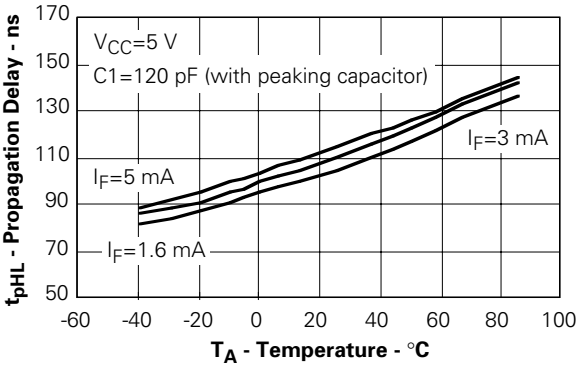


Figure 15. Typical propagation delays to logic high vs. temperature

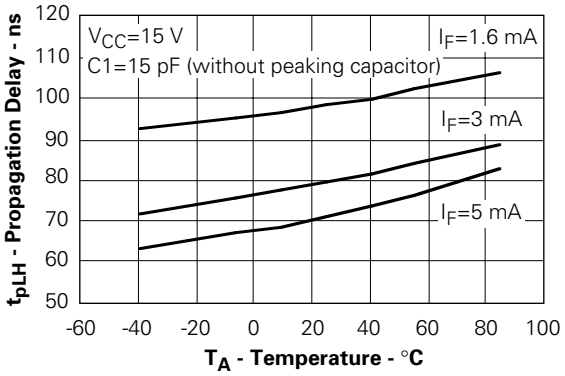


Figure 16. Typical propagation delays to logic low vs. temperature

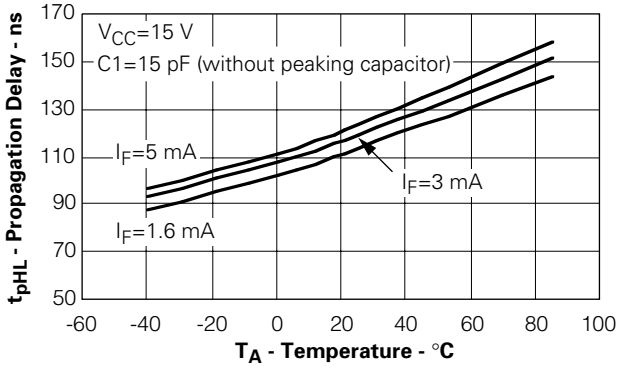


Figure 17. Typical propagation delays to logic high vs. temperature

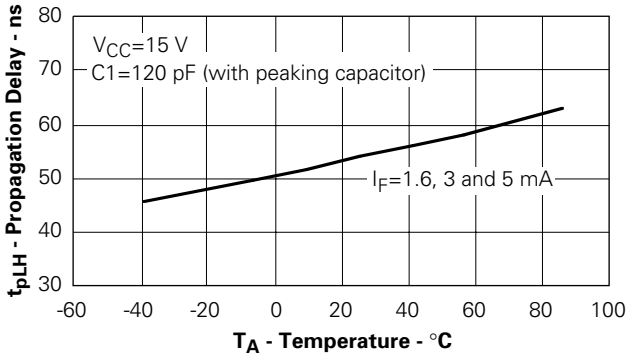


Figure 18. Typical propagation delays to logic low vs. temperature

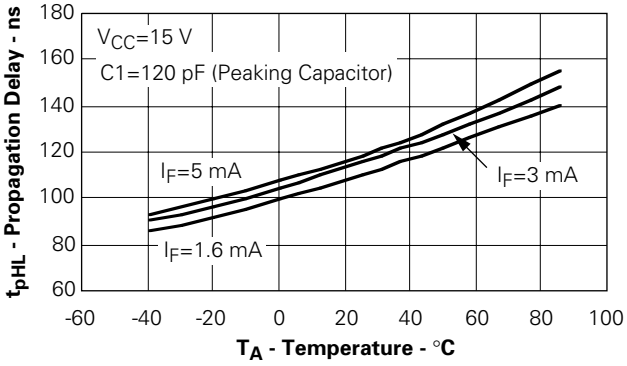


Figure 19. Test circuit for t_{PLH}, t_{PHL}, t_r and t_f

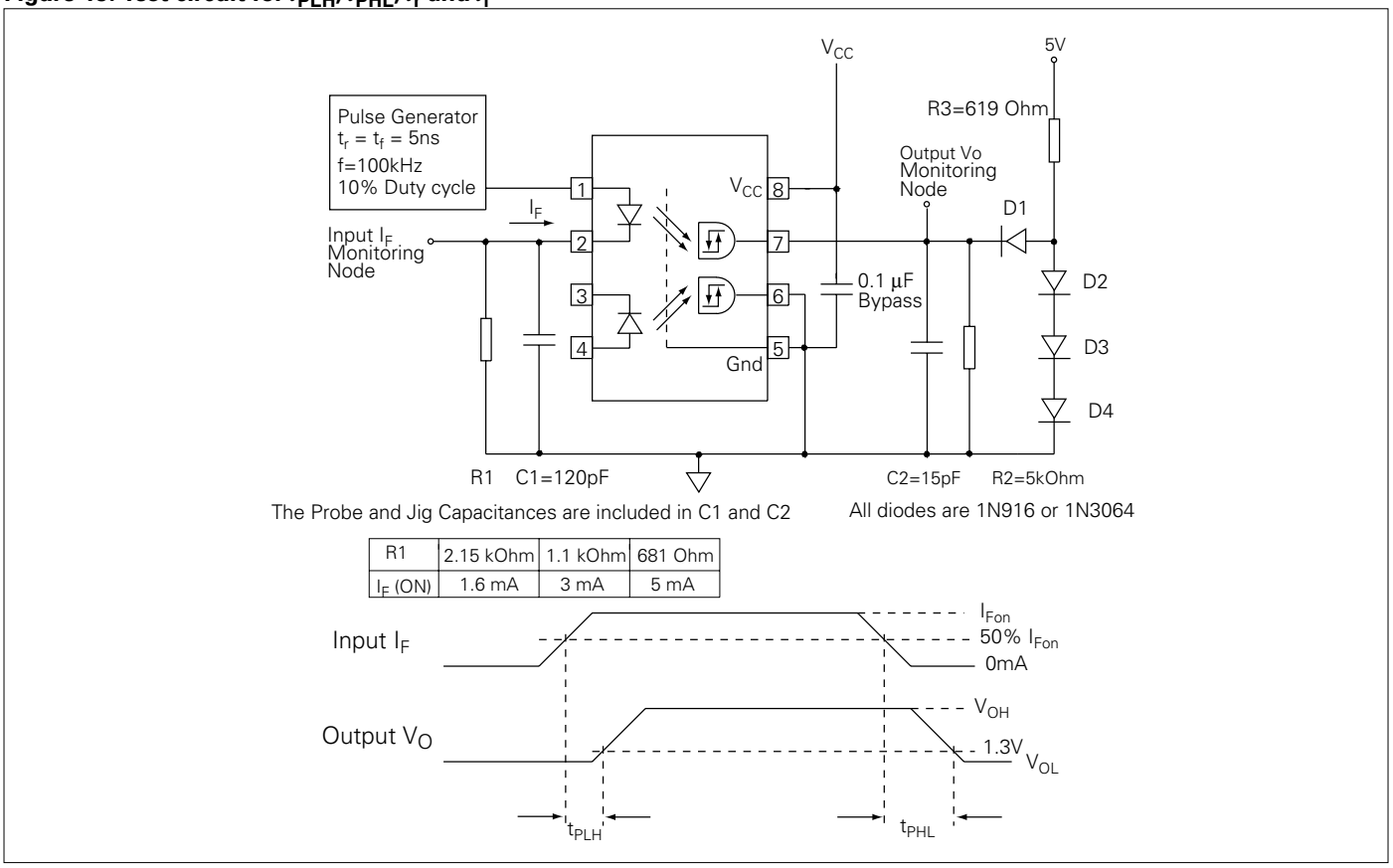


Figure 20. Test circuit for common mode transient immunity and typical waveforms