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Photon Vision Systems, Inc.

SLIS-XXXX Family - High Performance Linear CMOS Image Sensors
SLIS-2048, SLIS-4096, SLIS-6144, SLIS-8196

The Photon Vision Systems SLIS series is a family of high performance linear image sensors that offer high signal to noise ratio, extremely low dark current, and very high speed. The series is designed to fit a wide variety of applications as a superior CCD replacement, including:

- **High Speed, High Resolution Scanning**
- **Contact Imaging**
- **Bar Code Reading**
- **Encoding and Positioning**

Description

The SLIS-XXXX family of linear image sensors consists of an array of extremely low dark current photo-diode pixels with performance exceeding that of most CCD's. The device includes full frame electronic shuttering, allowing simultaneous readout and integration. A variety of readout and reset modes are provided to give exceptional versatility. A key feature over traditional CCD technology is that the device can be read and reread non-destructively, allowing the user to maximize signal to noise ratio and dynamic range.

Operation is simplified by on-chip logic, which requires only a clock running at two times the desired pixel read rate, and a pulse to initiate read-out. *Very high throughput is possible as the devices are equipped with a high speed PVS-BUS™ every 2K pixels, operating at 60 MHz pixel rate, with higher speeds possible.*

The SLIS-XXXX series are supplied in ceramic leadless chip carrier (LCC) and chip scale (CSP) packages.

These devices are protected under patent #6,084,229 and other patents pending.

Key Features

- Single Supply Operation
- 0.001 to 60 M-Pixel/sec Operation
- Low Cost
- High Sensitivity
- High Signal to Noise Ratio
- Non-destructive read capability
- Very Low Dark Current
- Multiple package options: CSP & LCC
- Interfaces to 3.3 Volt logic
- Simple control interface
- Replaces CCD systems, not just the sensor

Table 1 - SLIS Product Variants

MODEL	ARRAY SIZE (1)	PORTS	Throughput (M-Pixel/sec) (2)
SLIS-2048	1 x 2048	1	60
SLIS-4096	1 x 4096	2	120
SLIS-6144	1 x 6144	3	180
SLIS-8192	1 x 8192	4	240

Notes:
1. Pixels are 7.0µm x 7.0µm for all models
2. Throughput with 60 MHz ports. Devices will operate (at reduced Specs.) to 90 MHz per port, with 50% higher throughput.

SLIS Functional Block

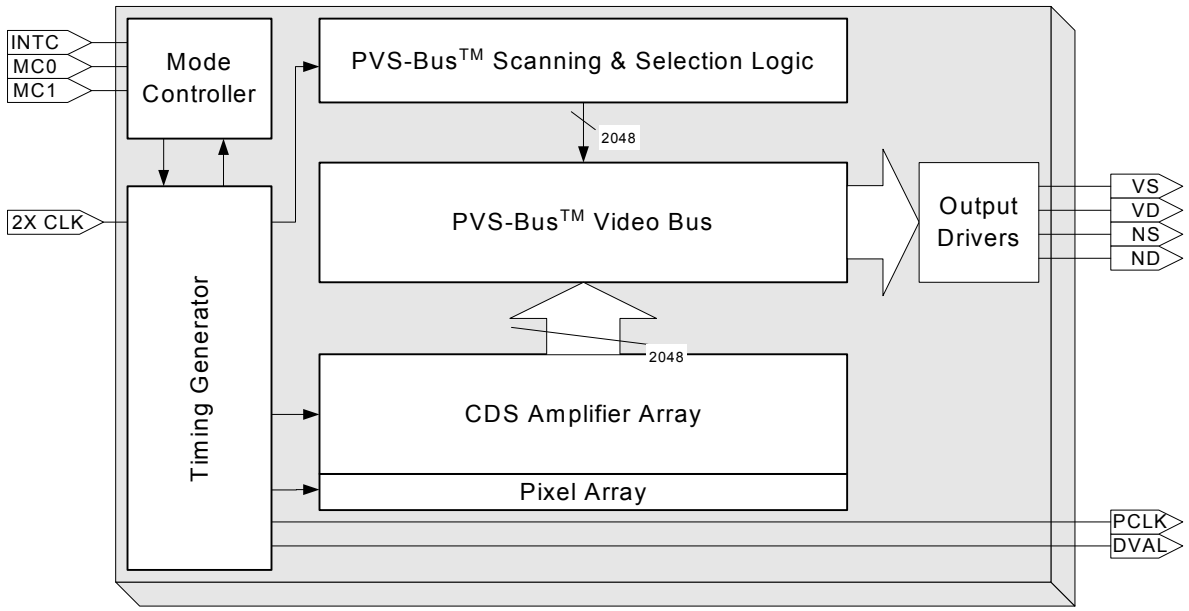

Figure 1 - Top level block diagram of SLIS-2048

Functional Pixel Diagram

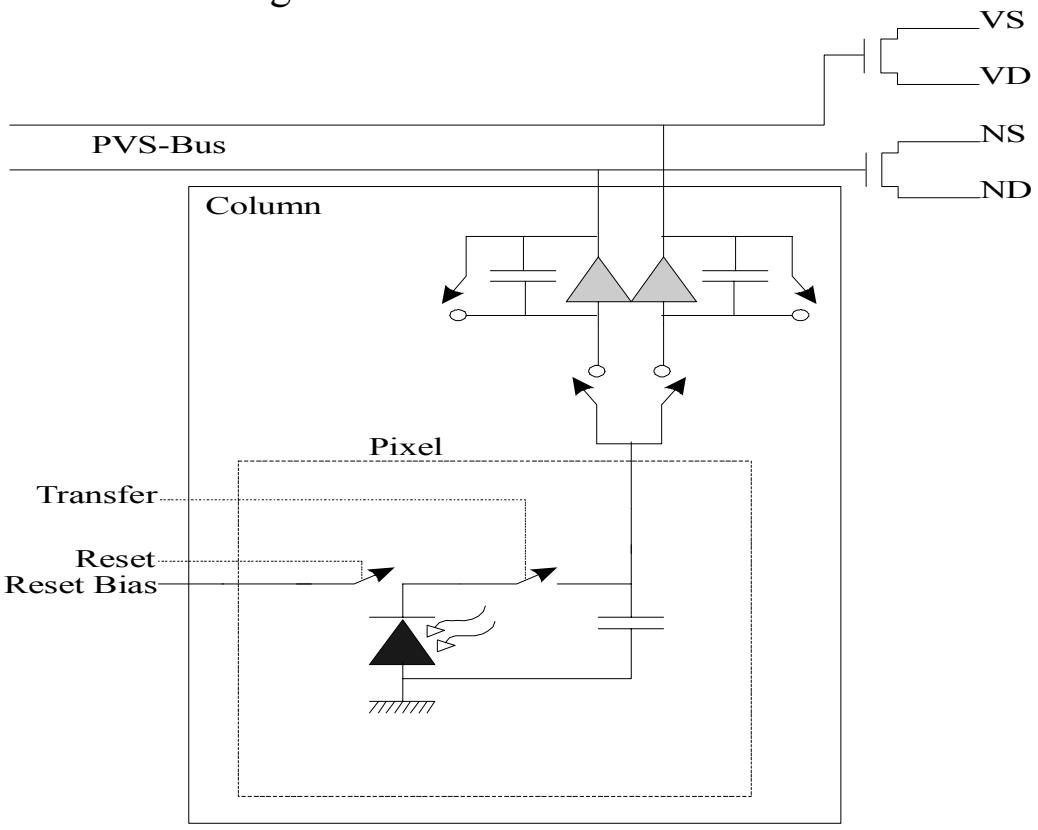

Figure 2 - Functional equivalent of pixel and signal chain.

SLIS-2048 Specifications (@T_A = 25°C, DVDD=AVDD=I/OLEVEL = 5.0VDC, CLK_{IN} = 120 MHz, unless otherwise specified)

Parameter	Conditions	Min	Typical	Max	Units
Digital Signals					
Input High Logic Level (V_{iH})		2.4			V
Input Low Logic Level (V_{iL})				0.6	V
Digital Output load current (I_{out})				1.0	mA
Input Clock Frequency (CLK_{IN})			120	180	MHz
DC					
Supply Voltage, AVDD		4.8	5.0	5.15	V
Supply Voltage, DVDD		4.8	5.0	5.15	V
Supply Voltage, I/O LEVEL	3.3V or 5.0 V interface, see note 1	3.15		5.15	V
Power Consumption, per segment	For each segment of 2048 pixels, see note 2		1.0		W
Video Output					
Analog output external Load (VOUT or NOUT)			1//2		kΩ//pF
Output Voltage at Saturation			4.8		V
Output Voltage at Dark			3.0		V
Electro-optical					
Pixel FPN per segment	Within a segment of 2048 pixels		6.0		% Total
Segment to Segment deviation	Between segments (e.g. SLIS-4096 or higher)		8.0		% Total
Photodiode Output Linearity	Pixel average from 5% - 75% Saturation		2.5		% SAT
MTF @ 60M-Pixel/sec	600nm		50		%
Dynamic Range	Note 3		55		dB
Well Capacity			500		Ke^-
Sensitivity	from 5% - 75% Saturation		3		$\mu V/e^-$
Quantum Efficiency	600nm		65		%
Output due to Dark Current	10mSec Integration		25		rms e^-
Read Noise	Note 3		250		rms e^-
Spectral Response Range		350		1100	nm
Environmental					
Relative Humidity Range		0		90	%
Operating Temperature Range		0		50	°C

Notes

1. Device digital I/O is capable of interfacing with 5.0 or 3.3 Volt logic via pin 20.
2. Power consumption per 2048 pixel segment at 60MHz and 1 kΩ load between VOUT and NOUT. For total power consumption, multiply the number of 2K segments by this number. For example – SLIS-6144 has 3 segments; therefore total power consumption is 1.50 watts.
3. Temporal Noise at 60M-pixel/sec rate and 30MHz bandwidth filter applied to output.

Absolute Maximum Ratings, T_A = 25°C unless otherwise noted. †

Supply voltage range, V_{DD} ---------- 0 V to 5.25 V
Digital input current range, I ---------- –20 mA to 20 mA
Operating case temperature range, T_C (see Note 2)---------- –10°C to 70°
Operating free-air temperature range, T_A ---------- 0°C to 50°C
Storage temperature range ---------- –20°C to 85°C
Humidity range, R_H ---------- 0-100%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 10 seconds------ 255°C

† Exceeding the ranges specified under "absolute maximum ratings" can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated under "recommended operating conditions" is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.

Notes
1. Voltage values are with respect to the device GND terminal.
2. Case temperature is defined as the surface temperature of the package measured directly over the integrated circuit.

Signal Description

Table 2 - Signal Descriptions

Signal Name	Signal Type	Description (1)
PVDD	Bias	Analog guard ring bias (+5V)
PGND		Analog guard ring return
AVDD		Analog Vdd (+5V)
AGND		Analog ground
DVDD		Digital Vdd (+5V)
DGND		Digital ground
I/O LEVEL		I/O Logic level (+3.3V ≤ $V_{I/O}$ ≤ +5.0V)
VD	Video Output	Drain of video channel output PFET
VS		Source of video channel output PFET
ND		Drain of reference channel output PFET
NS		Source of reference channel output PFET
INTC	Digital Input	Integration and read-out control
MC1		Read-out mode select bit '1'
MC0		Read-out mode select bit '0'
CLK		Master clock (2X pixel clock)
PCLK	Digital Output	Pixel clock output – used to synchronize data read out
DVAL		Data valid flag – remains high while data is read out

Notes
1. The signals described above are repeated for each segment of a multi-segmented device, i.e. two sets for SLIS-4096, three sets for SLIS-6144, etc.

Application Information

Power and I/O Considerations

Internally, the imager runs from three separate power supplies with a common reference node. The internal analog circuitry derives power from the AVDD supply, which should always be operated at 5.0 VDC nominal. The internal digital circuitry derives power from the DVDD supply, which should also be operated at 5.0 VDC. The digital I/O operates from the I/O LEVEL supply and can operate at 5.0 or 3.3 VDC nominal supply so that the device can interface with 5.0 or 3.3 volt external logic as desired.

Device Operation and Timing

Photo-site integration and readout timing is controlled by the Integration Control (INTC) signal. When INTC is taken high, the charge that has integrated in the photo-sites since INTC last went low is transferred to the photo-site storage capacitors for sampling by the correlated double sampling (CDS) circuits. At this point the photo-sites may or may not be reset depending on the mode (See operational modes section for more detail). After the CDS functions have finished, the 'data valid' (DVAL) output is set high indicating that pixel data is available at a rate of one pixel per 'pixel clock' (PCLK) period. At any time after the CDS function is complete, the INTC signal can be pulled low again to initiate integration of the photo-sites for the next frame. The photo-sites will be held in reset and thus no charge will integrate while INTC is held high. Pixel data is valid on the falling edge of PCLK. At the end of the frame, DVAL goes low again, and the system is ready for another INTC rising edge to initiate the output of the next frame.

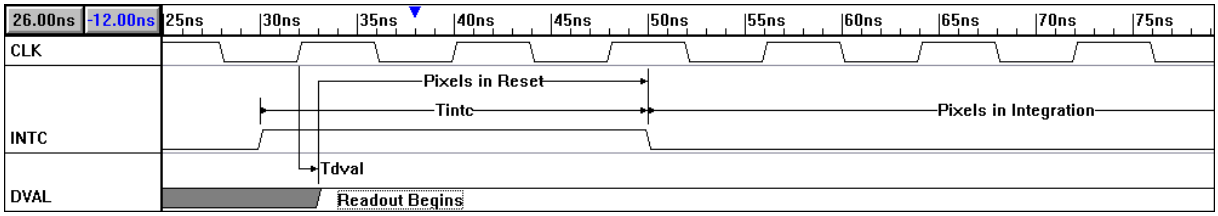

Figure 3 - Timing Diagram, Frame Timing with INTC

Symbol	Parameter	Conditions	Min (µs)	Typ (µs)	Max (µs)
t_{intc}	INTC pulse width high	Figure 3	2		
T_{dval}	CLK ↑ to DVAL ↑	Figure 3		2	3
T_{pd1}	CLK ↑ to PCLK ↑	Figure 4		2	3
T_{pd2}	CLK ↑ to PCLK ↓	Figure 4		2	3
T_{pd3}	Valid Pixel Hold Time after PCLK ↓	Figure 4	5	6	
T_{pd4}	CLK ↑ to Valid Pixel Transition	Figure 4	1	3	6

Table 3 - Waveform Timing Parameters

Operational Modes

The imager can be placed in four different operational modes using the Mode Select inputs, MC0 and MC1. These inputs are asynchronous and will place the imager in an undefined state for one frame after the mode is changed. Table 4 shows the different modes and their names. Mode descriptions follow.

Table 4 - Mode Descriptions

Mode	Mode Controls		Description
	MC0	MC1	
0	0	0	Segment disabled
1	0	1	Full CDS
2	1	0	Non-destructive read-out
3	1	1	Adaptive Exposure

Mode 0: Disable Mode

The master clock signal is internally ignored, and all digital outputs go to a high impedance state. The NOUT and VOUT signals are open ended and left floating. (Note: analog output disable may not be implemented in pre-production beta units)

Mode 1: Full Correlated Double Sampling (CDS) Mode

This is the normal operational mode where charge integrates in the photo-sites while INTC is low. When INTC is pulled high, the CDS function takes place, followed by the DVAL signal going high to indicate the beginning of valid pixel output. When all pixels have been clocked out, the DVAL signal goes low again. At any time after the CDS function is complete, the INTC signal can be pulled low again to initiate integration of the photo-sites for the next frame. By manipulating the pulse width of INTC, the user controls imager exposure time on a frame-by-frame basis. Exposure time is determined by the low time of INTC.

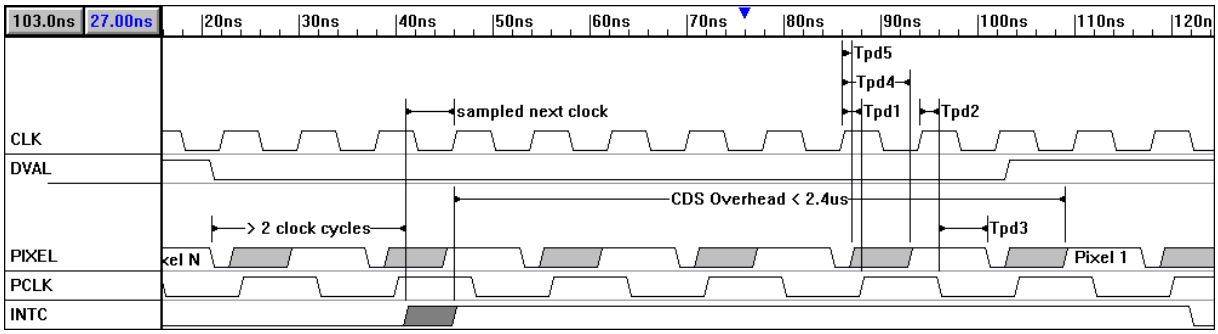

Figure 4 - Pixel Timing Diagram

Mode 2: Nondestructive Read-out (NDRO) Mode

Operation is identical to Full CDS Mode, except that the photo-sites are never switched out to the photo-site storage capacitors, so the charge stored in the hold capacitor remains intact for readout. For successive frame reads, the readout of data only differs by temporal noise content. This mode permits the user to capture a frame once and then read it out multiple times to average out the temporal noise content.

Mode 3: Adaptive Exposure (AE) Mode

Operation differs from Full CDS Mode only in the reset of the photo-sites. In AE mode, the photo-site charge is never reset, allowing the photo-site charge to continue integrating across multiple frames. Transition to a reset state must take place by changing back to Full CDS Mode. The AE mode permits the user to extend the total exposure time beyond the limits of a single frame time without modulating the sampling clock. Further, by permitting read-out of each intermediate frame, the user can be assured of capturing the desired exposure level.

Analog Output Signals

Each imager in the family has four video output pins per segment. The NS and ND outputs provide the reference voltage of the sensor including any common-mode switching noise coupled from the device's internal operation. The VS and VD outputs provide the gray value of the pixel also including any common-mode noise from the internal operation of the sensor. By subtracting the reference signal from the video signal with an external differential amplifier, the common-mode noise can be removed resulting in a video signal free from common-mode noise and representing the true gray level relative to the internal reference level. A typical video output connection is shown in Figure 5 below. Note that to achieve maximum signal at 60 M-Pixel/sec data rate, the output load impedance must be low. The output FETs are P-channel and are designed to handle loads as low as 1 KΩ. Since, the load impedance dominates the rise-time of the output circuit, stray capacitance at the VS and NS nodes must be kept as low as possible. A differential amplifier with low input capacitance must be used. It is also recommended that the output traces on the PCB be kept as short as possible. If it is not feasible to keep the output traces short, then buffer amplifiers should be inserted in the VS and NS outputs lines with the buffers as close to the imager pins as possible.

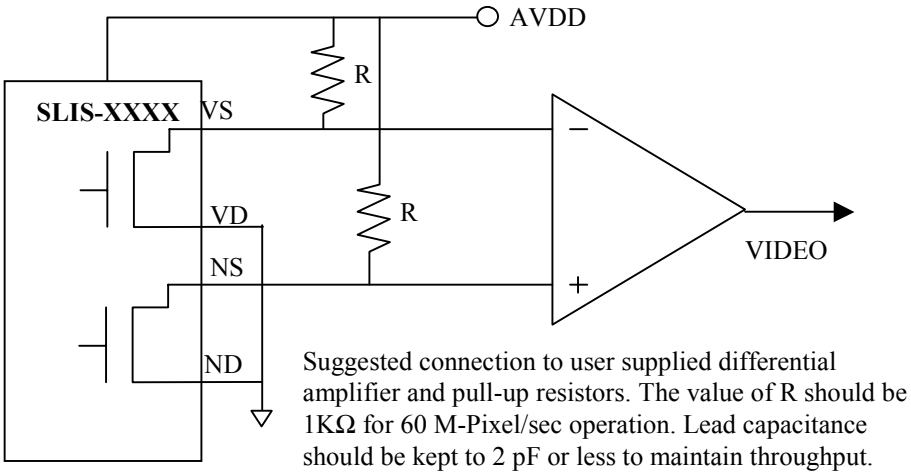

Figure 5 – Suggested Video Output Connections

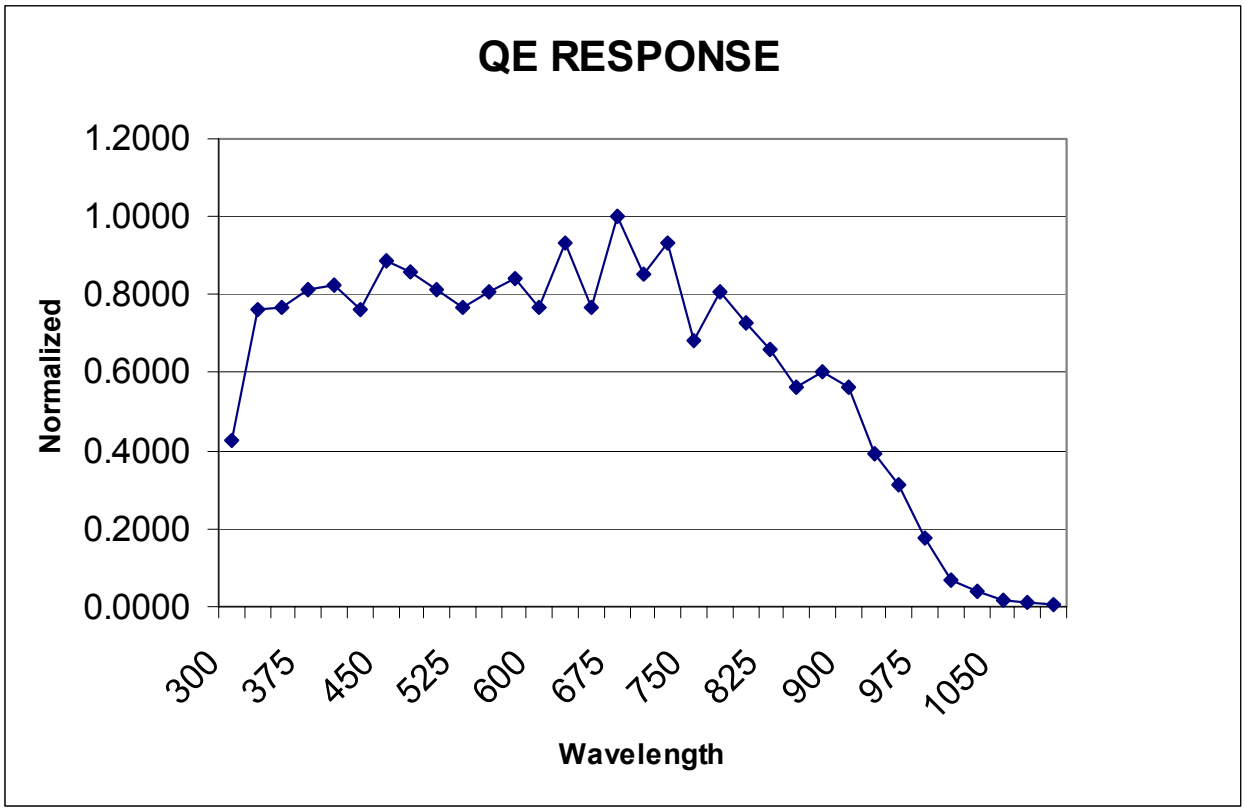

Figure 6 - Normalized Quantum Efficiency Response. Absolute value at peak (1.0) is 70%.

Chip Scale Package (CSP) Data

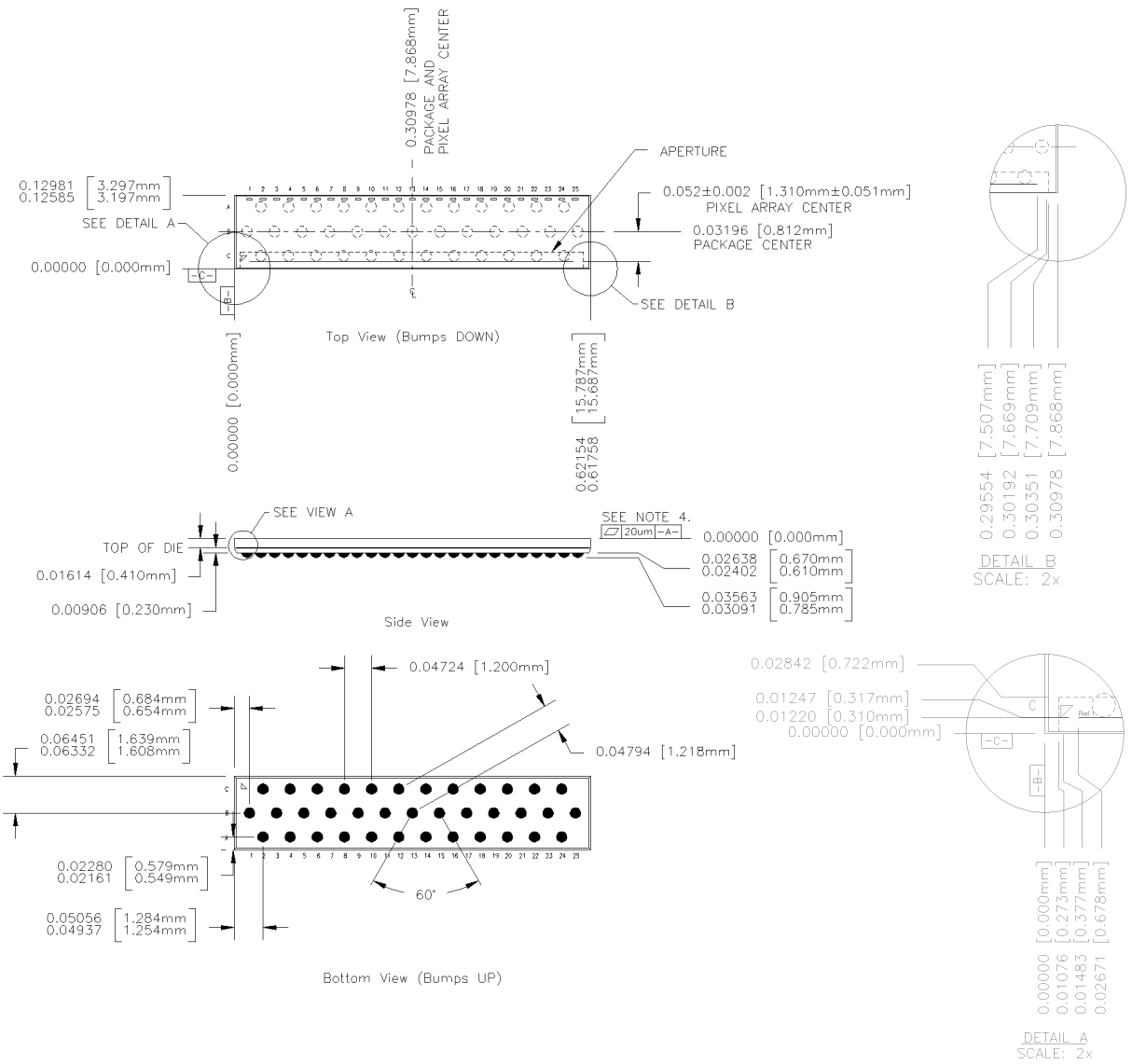

Figure 7 - Outline, Chip Scale Package (Preliminary Dimensions)

Table 5 – Chip Scale Package Pin-out

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	AGND	A8	AGND	A14	PCLK	A20	VS
A2	AVDD	B9	AVDD	B15	INTC	B21	VD
B3	DGND	A10	CLK (in)	A16	AGND	A22	AGND
A4	DVDD	B11	DVAL	B17	AVDD	B23	AVDD
B5	MC1	A12	AGND	A18	NS	A24	PGND
A6	I/O LEVEL	B13	AVDD	B19	ND	B25	PVDD
B7	MC0						

Ceramic Leadless Chip Carrier (CLCC) Package Data

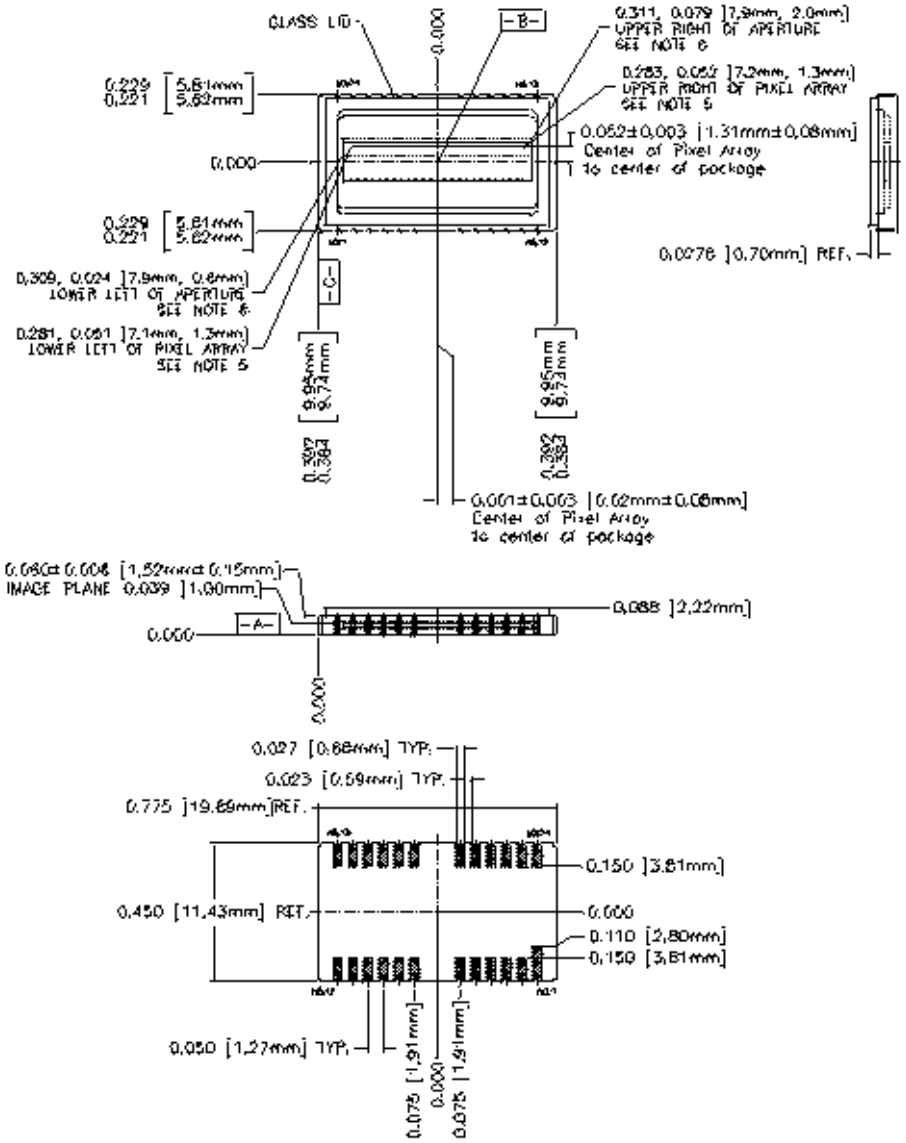

Figure 8 – Outline, Ceramic Leadless Chip Carrier (Preliminary Dimensions)

Table 6 – Ceramic LCC Pin-out

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VD	6	PCLK	11	MC1	19	PVDD
2	VS	7	DVAL	12	DVDD	20	PGND
3	ND	8	CLK (input)	13	DGND	21-24	AVDD
4	NS	9	MC0	14-17	AGND		
5	INTC	10	I/O LEVEL	18	N/C		

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