

Single-Ended Bus Transceiver

Features

- Single-Ended Transceiver
- Survives Shorts and Transients on Automotive Bus
- Wide Power Supply Voltage Range
- ISO 9141 Compatible
- Open Drain Fault Output

Benefits

- Single-Wire Multiplexer Interface
- ISO Diagnosis Bus

Applications

- Automobiles
- Trucks
- Tractors

Description

The Si9241EY is a monolithic bus transceiver designed to provide bidirectional serial communication in automotive diagnostic applications.

The device incorporates protection against overvoltages and short circuits to GND or V_B . The transceiver pin is protected and can be driven beyond the V_B voltage.

A fault output provides an active low in case of a short circuit or an open load. In the event of an over temperature condition, the output is immediately switched off and a fault indicated. This condition can only be reset once the over temperature condition is removed, and $\overline{CS}$ is toggled high.

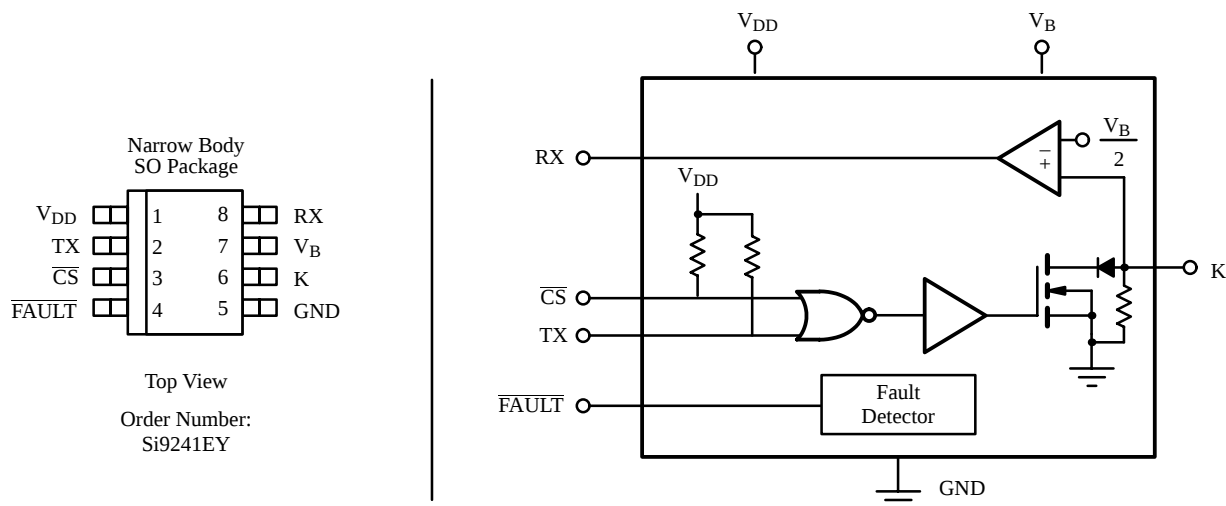
For bi-directional communication, $\overline{CS}$ must be High for “receive” and Low for “transmit”. If $\overline{CS}$ is Low, while IC is receiving data, an incorrect fault signal will occur. To inhibit the open load and short detect, tie $\overline{CS}$ and T_X together.

The Si9241EY is built on the Siliconix BiC/DMOS process. An epitaxial layer prevents latchup.

The RX output is capable of driving CMOS or $1 \times$ LSTTL load.

The Si9241EY is available in a space efficient 8-pin SO package. It operates reliably over the automotive temperature range (-40 to 125°C).

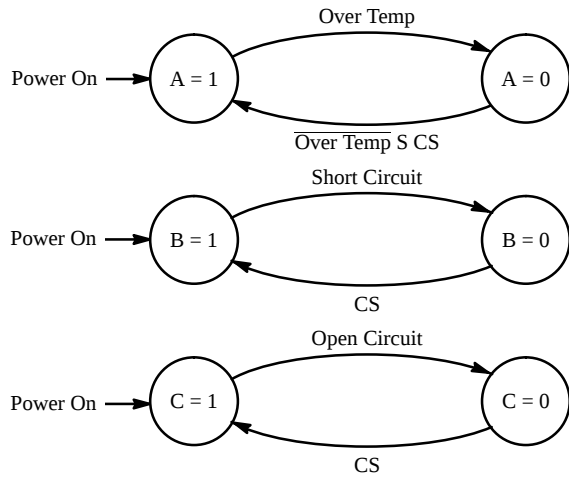
Pin Configuration and Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70013. Application Note AN602 may also be obtained via FaxBack, request document #70573.

Si9241EY

Output Table and State Diagrams



Inputs		State Variable			Output Table			Comments
$\overline{CS}$	TX	A	B	C	RX	K	$\overline{FAULT}$	
0	0	1	1	1	0	0	1	Over Temp Short Circuit Open Circuit
0	1	1	1	1	1	1	1	
X	X	0	1	1	K	HiZ	0	
0	X	1	0	1	K	HiZ	0	
0	X	1	1	0	K	HiZ	0	Receive Mode
1	X	1	1	1	0	0	1	
1	X	1	1	1	1	1	1	

X = "1" or "0"
HiZ = High Impedance State

Note: Over Temp is a condition and not meant to be a logic signal.

Absolute Maximum Ratings

Voltage Referenced to Ground

Voltage On V_{BAT} 45 V

Voltage K -16 V to ($V_B + 1$ V)

Voltage or Max. Current On Any Pin

(Except V_{BAT} , K) -0.3 V to $V_{DD} + 0.3$ V or 10 mA

Voltage on V_{DD} 7 V

Short Circuit Duration (to V_{BAT} or GND) Continuous

Operating Temperature (T_A) -40 to 125°C

Junction and Storage Temperature -55 to 150°C

Thermal Resistance Θ_{JA} 125°C/W

Specifications

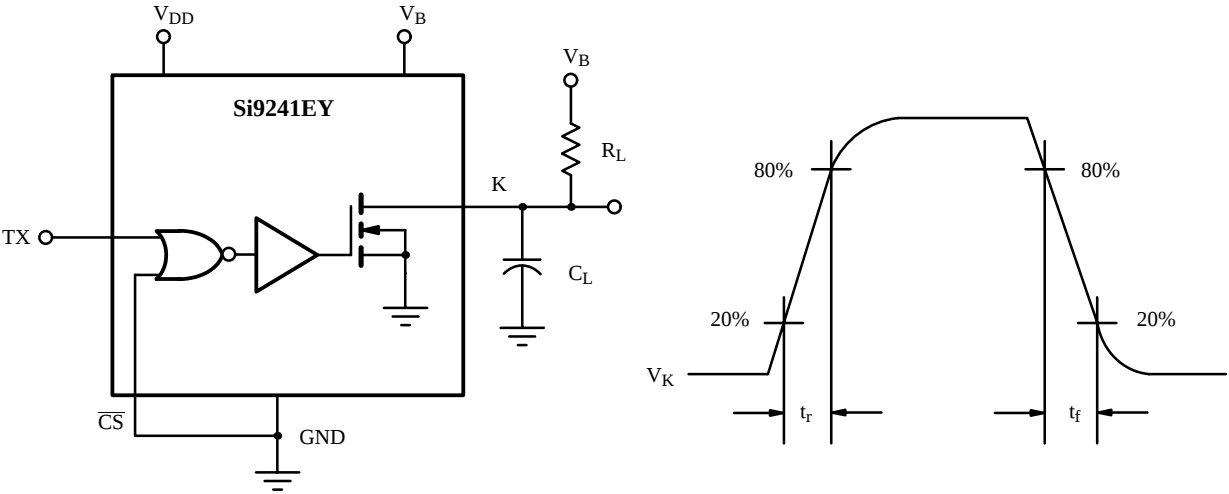
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.5 to 5.5 V, V_{BAT} = 7.25 to 35 V	Temp ^a	Limits E Suffix: −40 to 125°C			Unit
				Min ^b	Typ ^c	Max ^b	
Transmitter and Logic Levels							
$\overline{CS}$, TX Input Low Voltage	V_{ILT}		Full			1.5	V
$\overline{CS}$, TX Input High Voltage	V_{IHT}		Full	3.5			
K Output Low Voltage	V_{OLK}	R_L = 510 Ω , C_L = 10 nF V_{BAT} = 35 V, V_{DD} = 4.5 V	Full			4.9	
		R_L = 510 Ω , C_L = 10 nF See Test Circuit	Full			0.2 V_{BAT}	
K Output High Voltage	V_{OHK}		Full	0.91 V_{BAT}			
K Rise, Fall Times	t_r , t_f		Full			9.6	μs
K Output Sink Resistance	R_{si}	$\overline{CS}$ = 0 V, TX = 0 V	Full			110	Ω
K Output Capacitance ^d	C_O	$\overline{CS}$ = 0 V	Full			20	pF
TX Input Capacitance ^d	C_{INT}		Full			10	
$\overline{CS}$, TX Input Current	I_{INT}	V_{DD} = 5.5 V, V_{INT} = 1.5 V, 3.5 V	Full	−60		−4	μA

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V _{DD} = 4.5 to 5.5 V, V _B = 7.25 to 35 V		Temp ^a	Limits E Suffix: −40 to 125°C			Unit
					Min ^b	Typ ^c	Max ^b	
Receiver								
K Input Low Voltage	V _{ILK}			Full		0.4 V _{BAT}	0.33 V _{BAT}	V
K Input High Voltage	V _{IHK}			Full	0.7 V _{BAT}	0.6 V _{BAT}		
K Input Hysteresis ^d	V _{HYS}			Full	0.1 V _{BAT}			
RX Output Low Voltage	V _{OLR}	$\overline{CS}$ = 4 V	V _{ILK} = 0.33 V _{BAT} I _{OLR} = 1 mA	Full			0.4	
RX High Voltage	V _{OHR}		V _{IHK} = 0.70 V _{BAT} I _{OHR} = −40 μA	Full	4			
K Input Currents	I _{IHK}		V _{IHK} = V _{BAT}	Full	1.5		20	μA
Supplies								
Bat Supply Current	I _{BAT}	$\overline{CS}$, TX = 1.5 V, K Open		Full		2.7	5.0	mA
Logic Supply Current	I _{DD}			Full		1	3.0	
Miscellaneous								
Baud Rate	BR	R _L = 510 Ω, C _L = 10 nF		Full	10.4			kBaud
Fault Output Low Voltage	V _{OLF}	$\overline{CS}$ = T _X = 0V, K = V _B , I _{OLF} = 1 mA		Full			0.4	V
$\overline{CS}$ Minimum Pulse Width ^{d, e}	t _{cs}			Full	1			μs

- Notes
- a. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
 - b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
 - c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
 - d. Guaranteed by design, not subject to production test.
 - e. Minimum pulse width to reset a fault condition.

Test Circuit (Transmit Only)



Si9241EY

Application Circuit

