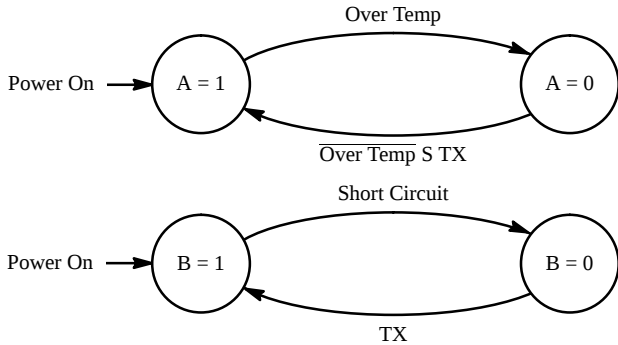


Si9243EY

Output Table and State Diagrams



Note: Over Temp is a condition and not meant to be a logic signal.

Inputs	State Variable		Output Table				Comments
	TX	A	B	K	RXK	L	
0	1	1	1	0	0	0	Over Temp Short Circuit
1	1	1	1	1	1	1	
0	1	1	1	0	0	1	
1	1	1	1	1	1	0	
X	0	1		HiZ	K	L	
0	1	0		HiZ	1	L	
1	1	1	1	1	1	1	Receive Mode
1	1	1	1	0	0	0	

X = "1" or "0"
HiZ = High Impedance State

Absolute Maximum Ratings

Voltage Referenced to Ground

Voltage On V_{BAT} 45 V

Voltage K, L -16 V to $V_{BAT} + 1$ V

Voltage On Any Pin (Except V_{BAT} , K, L)

or Max. Current -0.3 V to $V_{DD} + 0.3$ V or 10 mA

Voltage on V_{DD} 7 V

Short Circuit Duration (to V_{BAT} or GND) Continuous

Operating Temperature (T_A) -40 to 125°C

Junction and Storage Temperature -55 to 150°C

Thermal Resistance Θ_{JA} 125°C/W

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{DD} = 4.5$ to 5.5 V, $V_{BAT} = 7.25$ to 35 V	Temp ^a	Limits E Suffix: -40 to 125°C			Unit
				Min ^b	Typ ^c	Max ^b	
Transmitter and Logic Levels							
TX Input Low Voltage	V_{ILT}		Full			1.5	V
TX Input High Voltage	V_{IHT}		Full	3.5			
K Output Low Voltage	V_{OLK}	$R_L = 510\ \Omega$, $C_L = 10\ \text{nF}$ $V_{BAT} = 35\ \text{V}$, $V_{DD} = 4.5\ \text{V}$	Full			4.9	
		$R_L = 510\ \Omega$, $C_L = 10\ \text{nF}$ See Test Circuit	Full			$0.2\ V_{BAT}$	
K Output High Voltage	V_{OHK}		Full	$0.91\ V_{BAT}$			
K Rise, Fall Times	t_r , t_f		Full			9.6	μs
K Output Sink Resistance	R_{si}	TX = 0 V	Full			110	Ω
K Output Capacitance ^d	C_O		Full			20	pF
TX Input Capacitance ^d	C_{INT}		Full			10	
TX Input Current	I_{INT}	$V_{DD} = 5.5\ \text{V}$, TX = 1.5 V, 3.5 V	Full	-60		-4	μA

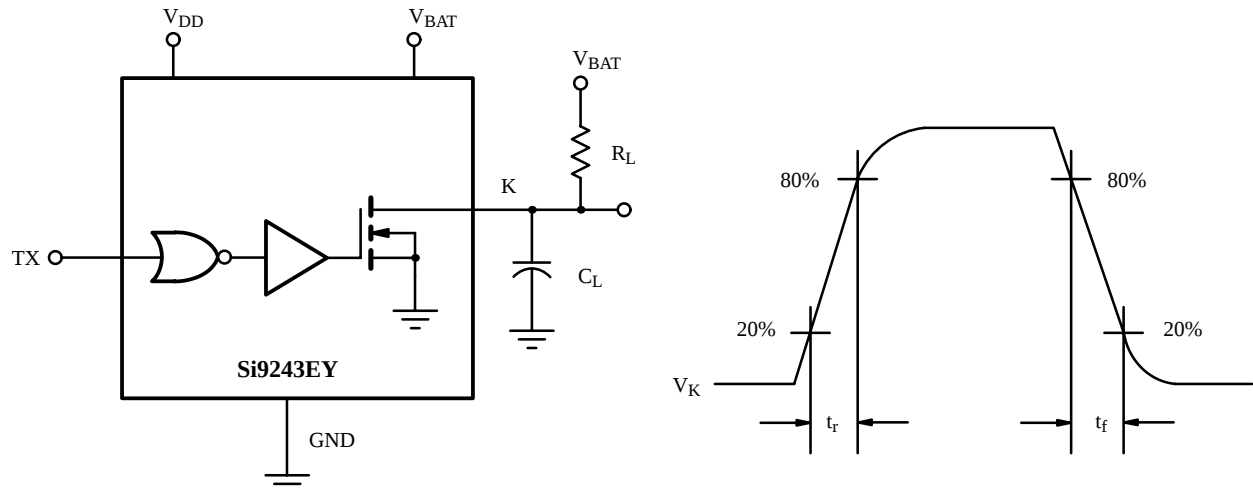
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{DD} = 4.5$ to 5.5 V, $V_B = 7.25$ to 35 V		Temp ^a	Limits E Suffix: -40 to 125°C			Unit
					Min ^b	Typ ^c	Max ^b	
Receiver								
L and K Input Low Voltage	V_{ILK}			Full		$0.4 V_{BAT}$	$0.33 V_{BAT}$	V
L and K Input High Voltage	V_{IHK}			Full	$0.7 V_{BAT}$	$0.6 V_{BAT}$		
L and K Input Hysteresis ^d	V_{HYS}			Full	$0.1 V_{BAT}$			
RXL and RXK Output Low Voltage	V_{OLR}	TX = 4 V	$V_{ILK}, V_{ILL} = 0.33 V_{BAT}$ $I_{OLR} = 1 \text{ mA}$	Full			0.4	
RXL and RXK High Voltage	V_{OHR}		$V_{IHK}, V_{IHL} = 0.70 V_{BAT}$ $I_{OHR} = -40 \mu\text{A}$	Full	4			
L and K Input Currents	I_{IHK}		$V_{IHK} = V_B$	Full	1.5		20	μA
Supplies								
Bat Supply Current	I_{BAT}	TX = 1.5 V, K, L Open		Full		2.7	5.0	mA
Logic Supply Current	I_{DD}	TX = 1.5 V, K, L Open		Full		1	3.0	
Miscellaneous								
Baud Rate	BR	$R_L = 510 \Omega$, $C_L = 10 \text{ nF}$		Full	10.4			kBaud
TX Minimum Pulse Width ^{d, e}	t_{TX}			Full	1			μs

Notes

- Room = 25°C , Cold and Hot = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- Minimum pulse width to reset a fault condition.

Test Circuit



Si9243EY

Application Circuit

