Multi-Output Power-Supply Controller

FEATURES

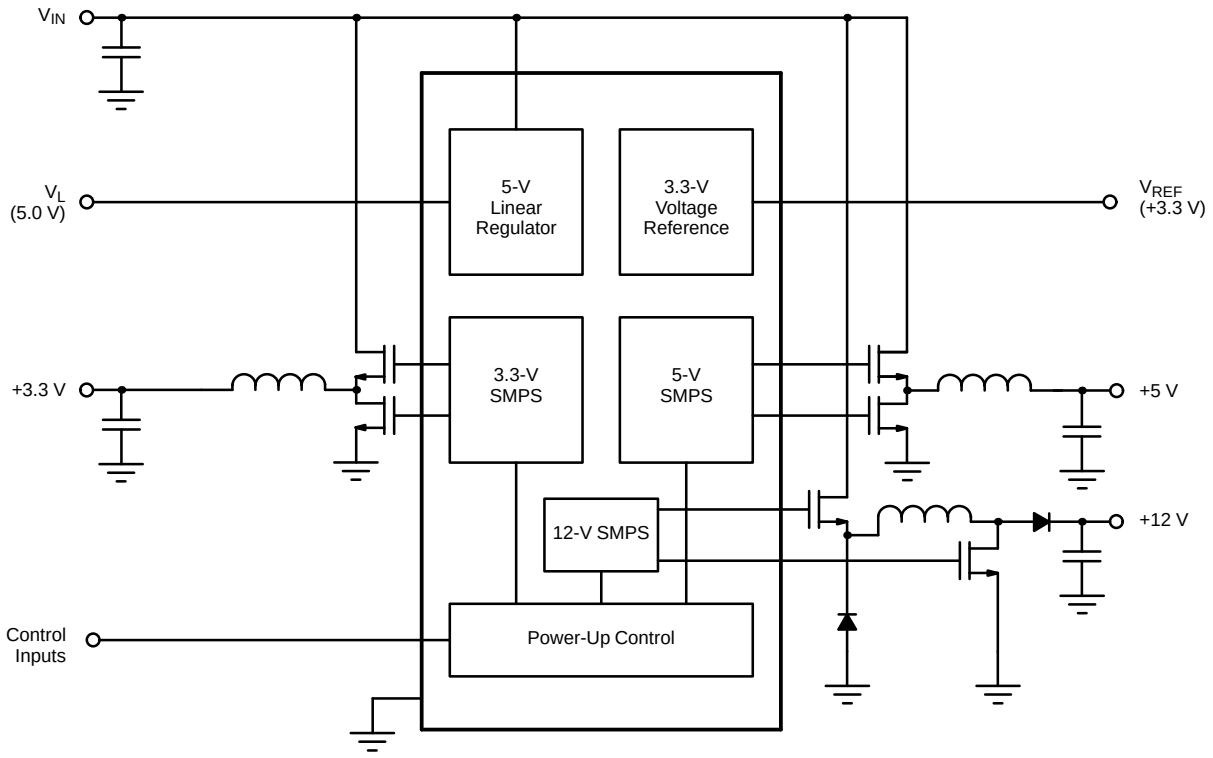
- Up to 95% Efficiency
- 3% Total Regulation (Each Controller)
- 5.5-V to 30-V Input Voltage Range
- 3.3-V, 5-V, and 12-V Outputs
- 200-kHz Low-Noise Fixed Frequency Operation
- Precision 3.3-V Reference Output
- 30 mA Linear Regulator Output
- High Efficiency Pulse Skipping Mode Operation at Light Load
- Only Three Inductors Required—No Transformer
- LITTLE FOOT® Optimized Output Drivers
- Internal Soft-Start
- Minimal External Control Components
- 28-Pin SSOP Package

DESCRIPTION

The Si9136 is a current-mode PWM and PSM converter controller, with two synchronous buck converters (3.3 V and 5 V) and a flyback (non-isolated buck-boost) converter (12 V). Designed for portable devices, it offers a total five power outputs (three tightly regulated dc/dc converter outputs, a precision 3.3-V reference and a 5-V LDO output). It requires minimum external components and is capable of achieving conversion efficiencies approaching 95%.

The Si9136 is available in a 28-pin SSOP package and specified to operate over the extended commercial (0°C to 90°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND ..... –0.3 to +36 V
P_{GND} to GND ..... ±2 V
V_L to GND ..... –0.3 to +6.5 V
BST_3, BST_5, BSTFY to GND ..... –0.3 V to +36 V
V_L Short to GND ..... Continuous
LX_3 to BST_3; LX_5 to BST_5; LXFY to BST ..... –6.5 V to 0.3 V
Inputs/Outputs to GND
(CS_3, CS_5, CSP, CSN) ..... –0.3 V to (V_L +0.3 V)
5 ON/$\overline{OFF}$, 3 ON/$\overline{OFF}$, 12 ON/$\overline{OFF}$ ..... –0.3 V to +5.5 V
DL3, DL5 to PGND ..... –0.3 V to (V_L +0.3 V)
DLFY to PGND ..... Input of Flyback
DH3 to LX_3, DH5 to LX_5,
DHFY to LXFY ..... –0.3 V to (BSTX +0.3 V)
Continuous Power Dissipation (T_A = 90°C)[a]
28-Pin SSOP[b] ..... 572 mW
Operating Temperature Range ..... 0°C to 90°C
Storage Temperature Range ..... –40°C to 125°C
Lead Temperature (Soldering, 10 Sec.) ..... 300°C

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 9.52 mW/°C above 90°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS

Parameter	Specific Test Conditions V_{IN} = 15 V , I_{VL} = I_{REF} = 0 mA T_A = 0°C to 90°C, All Converters ON	Limits Min[a]	Limits Typ[b]	Limits Max[a]	Unit
3.3-V Buck Controller					
Total Regulation (Line, Load, and Temperature)	V_{IN} = 6 to 30 V, 0 < V_{CS3} – V_{FB3} < 90 mV	3.23	3.33	3.43	V
Line Regulation	V_{IN} = 6 to 30 V			±0.5	%
Load Regulation	0 < V_{CS3} – V_{FB3} < 90 mV			±0.5	
Current Limit	V_{CS3} – V_{FB3}	90	125	160	mV
Bandwidth	L = 10 µH, C = 330 µF		50		kHz
Phase Margin	R_{SENSE} = 20 mΩ		65		°
5-V Buck Controller					
Total Regulation (Line, Load, and Temperature)	V_{IN} = 6 to 30 V, 0 < V_{CS5} – V_{FB5} < 90 mV	4.88	5.03	5.18	V
Line Regulation	V_{IN} = 6 to 30 V			±0.5	%
Load Regulation	0 < V_{CS5} – V_{FB5} < 90 mV			±0.5	
Current Limit	V_{CS5} – V_{FB5}	90	125	160	mV
Bandwidth	L = 10 µH, C = 330 µF		50		kHz
Phase Margin	R_{SENSE} = 20 mΩ		65		°
12-V Flyback Controller					
Total Regulation (Line, Load, and Temperature)	V_{IN} = 6 to 30 V, 0 < V_{CSP} – V_{CSN} < 300 mV	11.4	12.0	12.6	V
Line Regulation	V_{IN} = 6 to 30 V			±0.5	%
Load Regulation	0 < V_{CSP} – V_{FBN} < 300 mV			±0.5	
Current Limit	V_{CSP} – V_{CSN}	330	410	500	mV
Bandwidth	L = 10 µH, C = 100 µF		10		kHz
Phase Margin	R_{SENSE} = 100 mΩ, C_{comp} = 120 pF		65		°
Internal Regulator					
V_L Output	All Converters OFF, V_{IN} >5.5 V, 0 <I_L <30 mA	4.7		5.5	V
V_L Fault Lockout Voltage		3.6		4.2	
V_L Fault Lockout Hysteresis			75		mV
V_L /FB5 Switchover Voltage		4.2		4.7	V
V_L /FB5 Switchover Hysteresis			75		mV

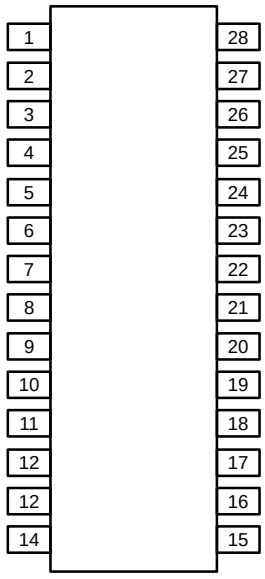
SPECIFICATIONS

Parameter	Specific Test Conditions V_{IN} = 15 V , I_{VL} = I_{REF} = 0 mA T_A = 0°C to 90°C, All Converters ON	Limits			Unit
		Min[a]	Typ[b]	Max[a]	
Reference					
REF Output	No External Load	3.24	3.30	3.36	V
REF Load Regulation	0 to 1 mA		30	75	mV
Supply Current					
Supply Current – Shutdown	All Converters OFF, No Load		35	60	µA
Supply Current – Operation	All Converters ON, No Load, F_{OCS} = 200 kHz		1100	1800	
Oscillator					
Oscillator Frequency		180	200	220	kHz
Maximum Duty Cycle		92	95		%
Outputs					
Gate Driver Sink/Source Current (Buck)	DL3, DH3, DL5, DH5 Forced to 2 V		1		A
Gate Driver On-Resistance (Buck)	High or Low		2	7	Ω
Gate Driver Sink/Source Current (Flyback)	DHFY, DLFY Forced to 2 V		0.2		A
Gate Driver On-Resistance (Flyback)	High or Low			15	Ω
5 ON/$\overline{\text{OFF}}$, 3 ON/$\overline{\text{OFF}}$, and 12 ON/$\overline{\text{OFF}}$					
V_{IL}				0.8	V
V_{IH}		2.4			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

PIN CONFIGURATION

SSOP-28



Top View

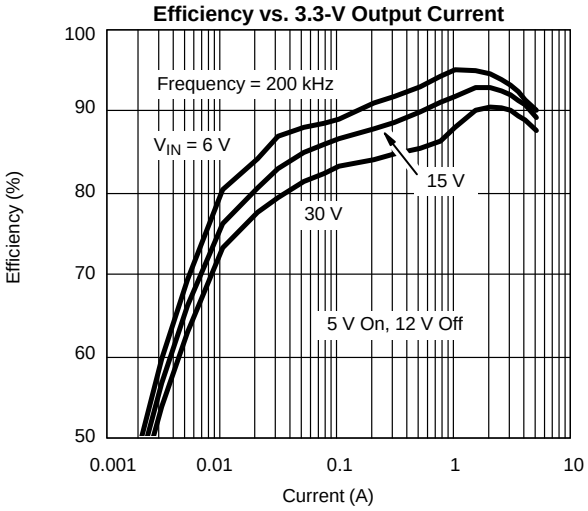
ORDERING INFORMATION

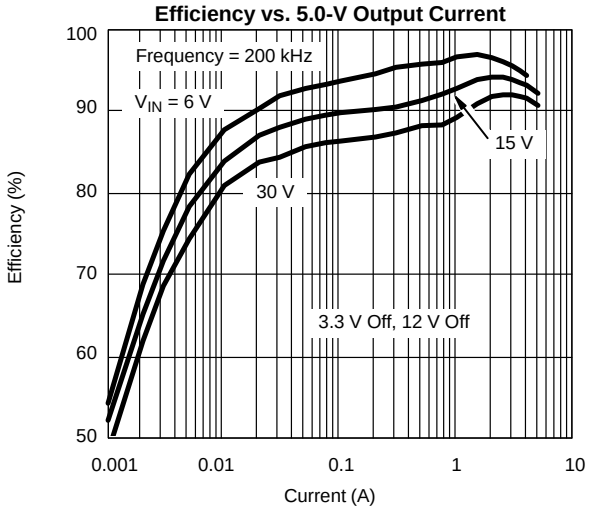
Part Number	Temperature Range	V_{OUT}
Si9136LG	0 to 90°C	3.3 V, 5 V, 12 V
Evaluation Board	**Temperature Range**	**Board Type**
Si9136DB	0 to 90°C	Surface Mount

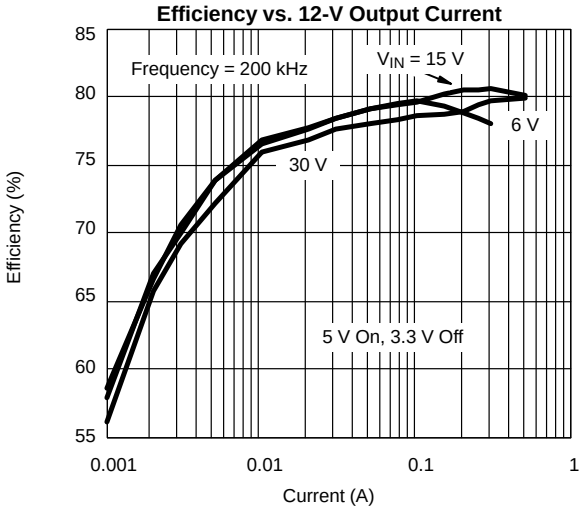
PIN DESCRIPTION

Pin Number	Symbol	Description
1	CS_3	Current sense input for 3.3-V buck.
2	FBFY	Feedback for flyback.
3	BSTFY	Boost capacitor connection for flyback converter.
4	DHFY	Gate-drive output for flyback high-side MOSFET.
5	LXFY	Inductor connection for flyback converter.
6	DLFY	Gate-drive output for flyback low-side MOSFET.
7	CSP	Current sense positive input for flyback converter.
8	CSN	Current sense negative input for flyback converter.
9	GND	Analog ground.
10	COMP	Flyback compensation connection, if required.
11	REF	3.3-V internal reference.
12	12 ON/$\overline{OFF}$	ON and OFF control input for 12-V flyback controller.
13	3.3 ON/$\overline{OFF}$	ON and OFF control input for 3.3-V buck controller.
14	5 ON/$\overline{OFF}$	ON and OFF control input for 5-V buck controller.
15	CS_5	Current sense input for 5-V buck controller.
16	DH5	Inductor connection for buck 5-V.
17	LX_5	Gate-drive output for 5-V buck high-side MOSFET.
18	BST_5	Boost capacitor connection for 5-V buck converter.
19	DL5	Gate-drive output for 5-V buck low-side MOSFET.
20	PGND	Power ground.
21	FB_5	Feedback for 5-V buck.
22	V_L	5-V logic supply voltage for internal circuitry.
23	V_{IN}	Input voltage
24	DL3	Gate-drive output for 3.3-V buck low-side MOSFET.
25	BST_3	Boost capacitor connection for 3.3-V buck converter.
26	LX_3	Inductor connection for 3.3-V buck low-side MOSFET.
27	DH3	Gate-drive output for 3.3-V buck high-side MOSFET.
28	FB_3	Feedback for 3.3-V buck.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

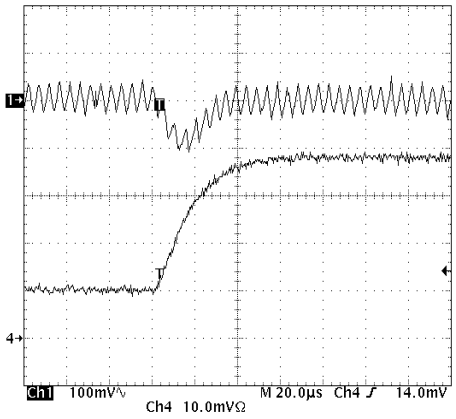






TYPICAL WAVEFORMS

5-V Converter (V_{IN} = 10 V)

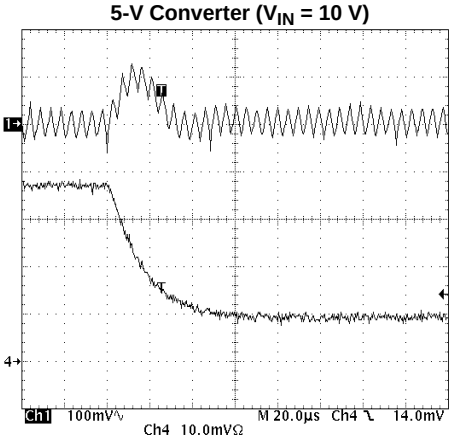


Ch1: V_{OUT}

Ch2: Load Current (1 A/div)

PWM Loading

5-V Converter (V_{IN} = 10 V)

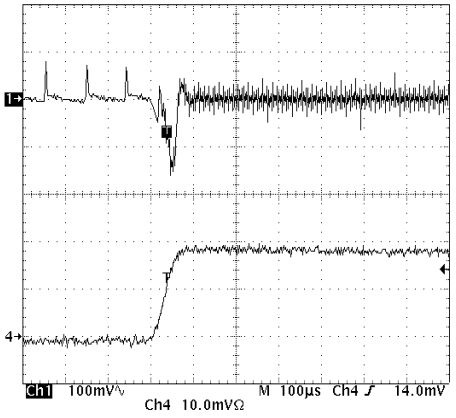


Ch1: V_{OUT}

Ch2: Load Current (1 A/div)

PWM Unloading

5-V Converter (V_{IN} = 10 V)

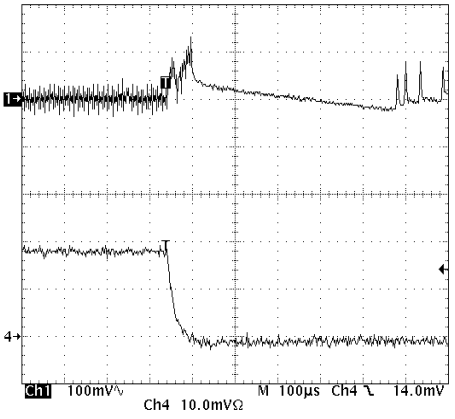


Ch1: V_{OUT}

Ch2: Load Current (1 A/div)

PSM Õ PWM

5-V Converter (V_{IN} = 10 V)

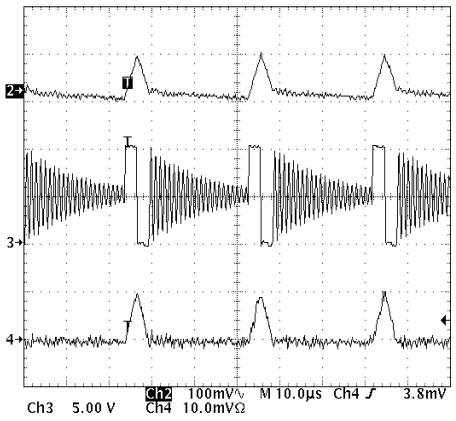


Ch1: V_{OUT}

Ch2: Load Current (1 A/div)

PWM Õ PSM

5-V Converter (V_{IN} = 10 V)



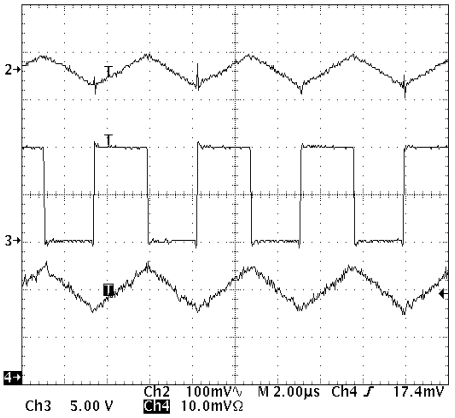
Ch2: V_{OUT}

Ch3: Inductor Node (L X5)

Ch4: Inductor Current (1A/div)

PSM Operation

5-V Converter (V_{IN} = 10 V)



Ch2: V_{OUT}

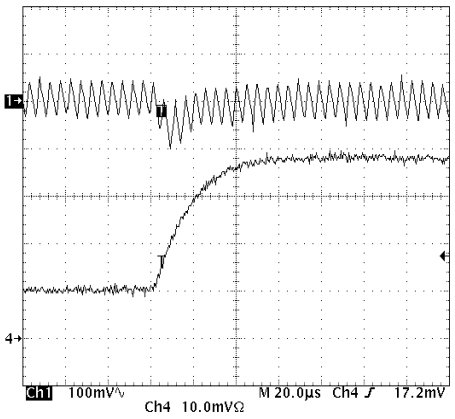
Ch3: Inductor Node (L X5)

Ch4: Inductor Current (1A/div)

PWM Operation

TYPICAL WAVEFORMS

3-V Converter (V_{IN} = 10 V)

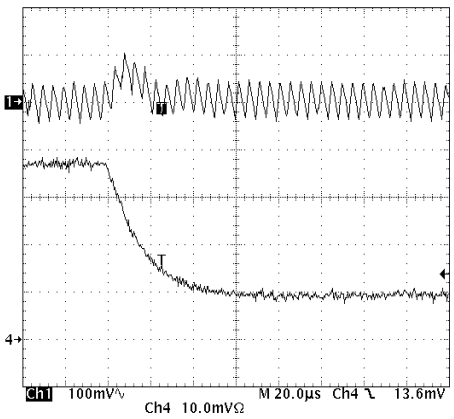


ɔUT

ad
(1 A/div)

PWM, Loading

3-V Converter (V_{IN} = 10 V)

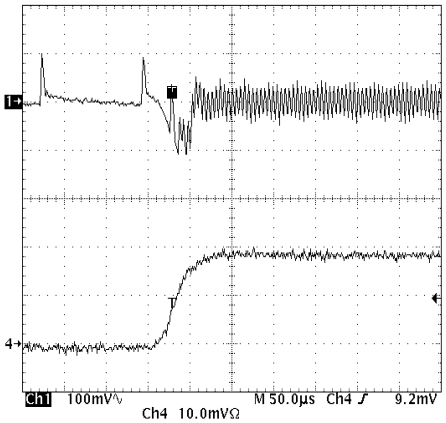


Ch1: V_{OUT}

Ch2: Load
Current (1 A/div)

PWM, Unloading

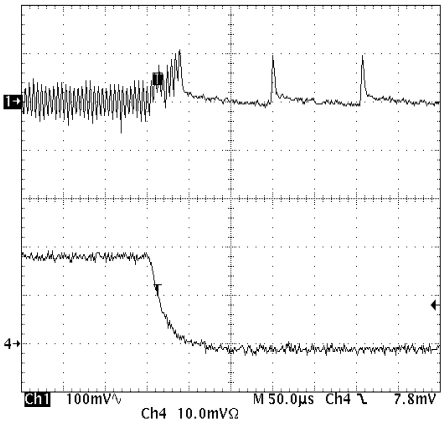
3-V Converter (V_{IN} = 10 V)



ɔad
(1 A/div)

PSM Õ PWM

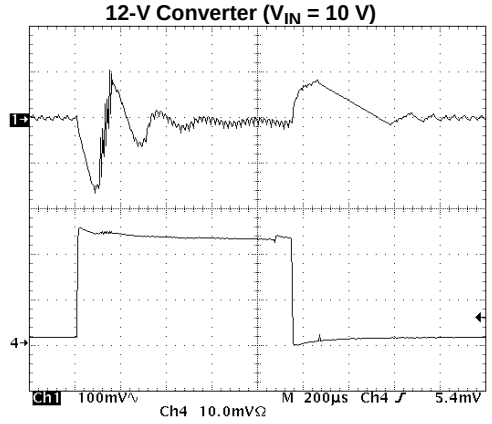
3-V Converter (V_{IN} = 10 V)



ad
(1 A/div)

PWM O PSM

12-V Converter (V_{IN} = 10 V)

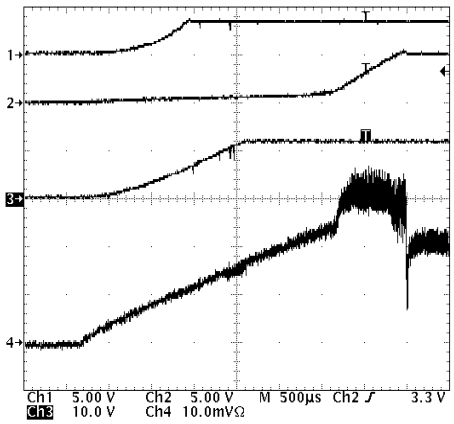


Ch1: V_{OUT}

Ch4: Load
Current
(100 mA/div)

250-mA Transient

Start-Up



3.3-V Output

5-V Output

12-V Output

Inductor Current,
5-V Converter
(2 A/div)

STANDARD APPLICATION CIRCUIT

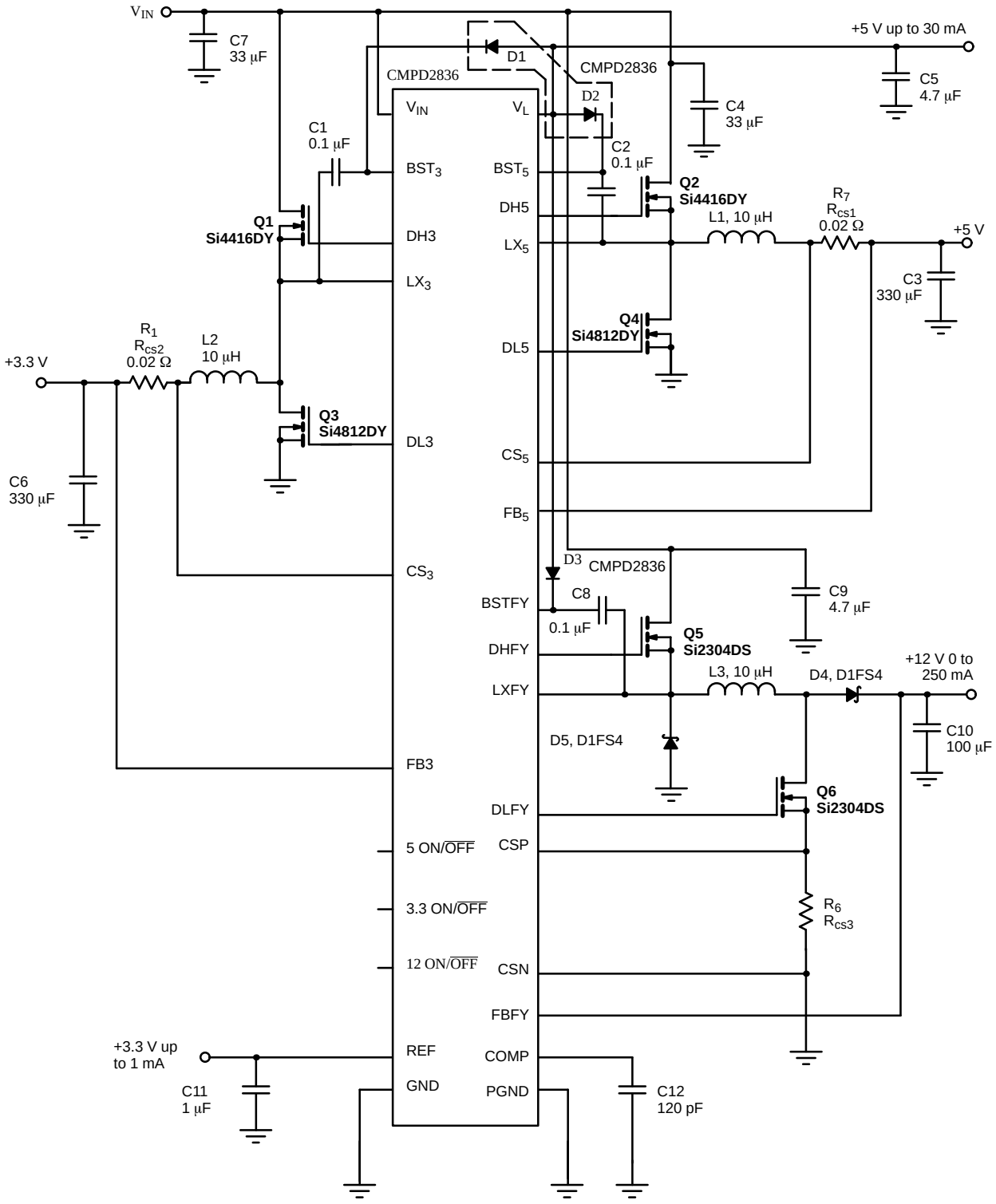


FIGURE 1.

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S-00583—Rev. C, 03-Apr-00

TIMING DIAGRAMS

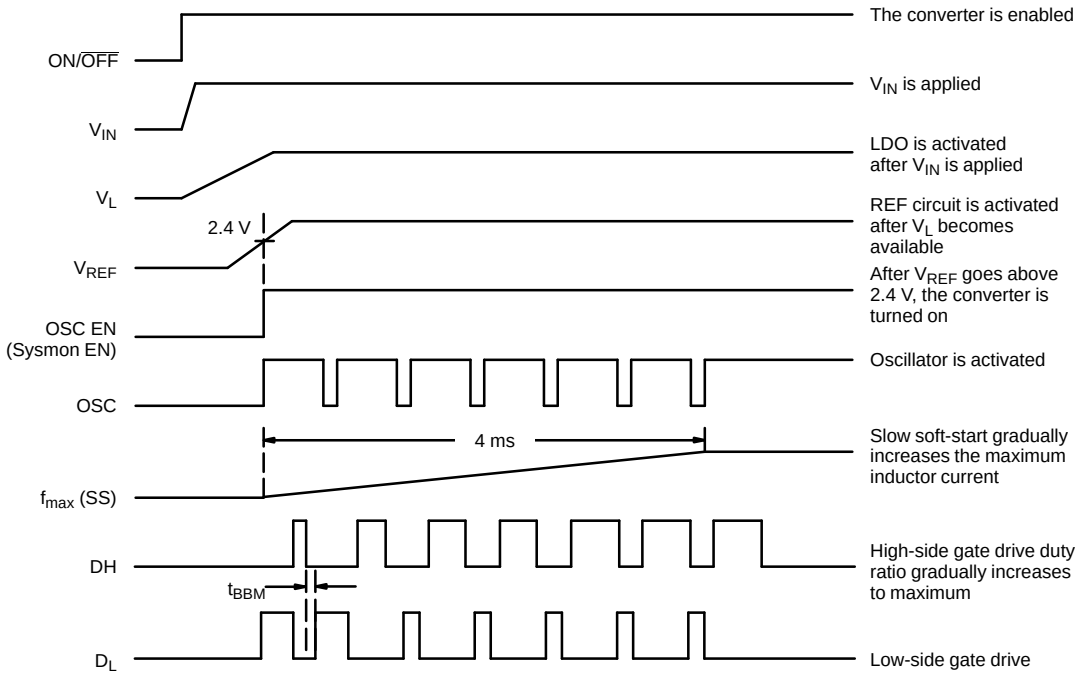

FIGURE 2. Converter is Enabled Before V_{IN} is Applied

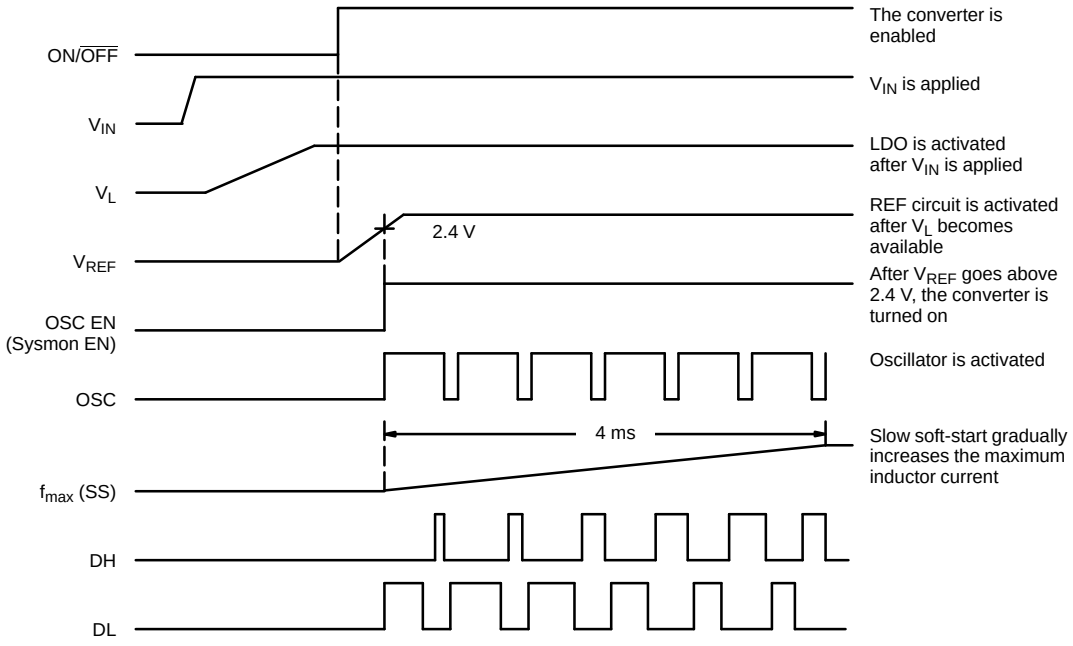

FIGURE 3. Converter is Enabled After V_{IN} is Applied

TIMING DIAGRAMS

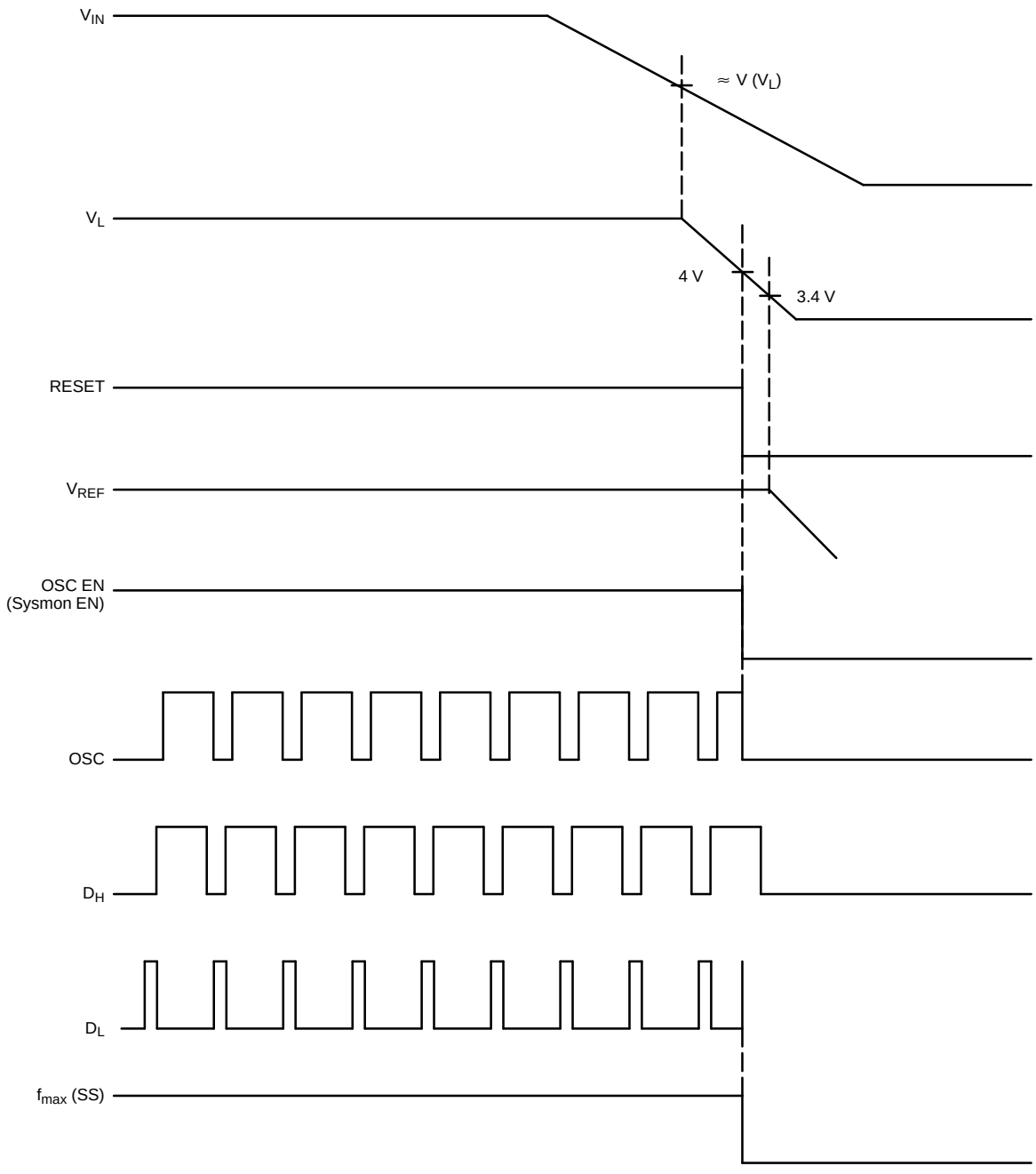

FIGURE 4. Power Off Sequence

DETAIL FUNCTIONAL BLOCK DIAGRAM

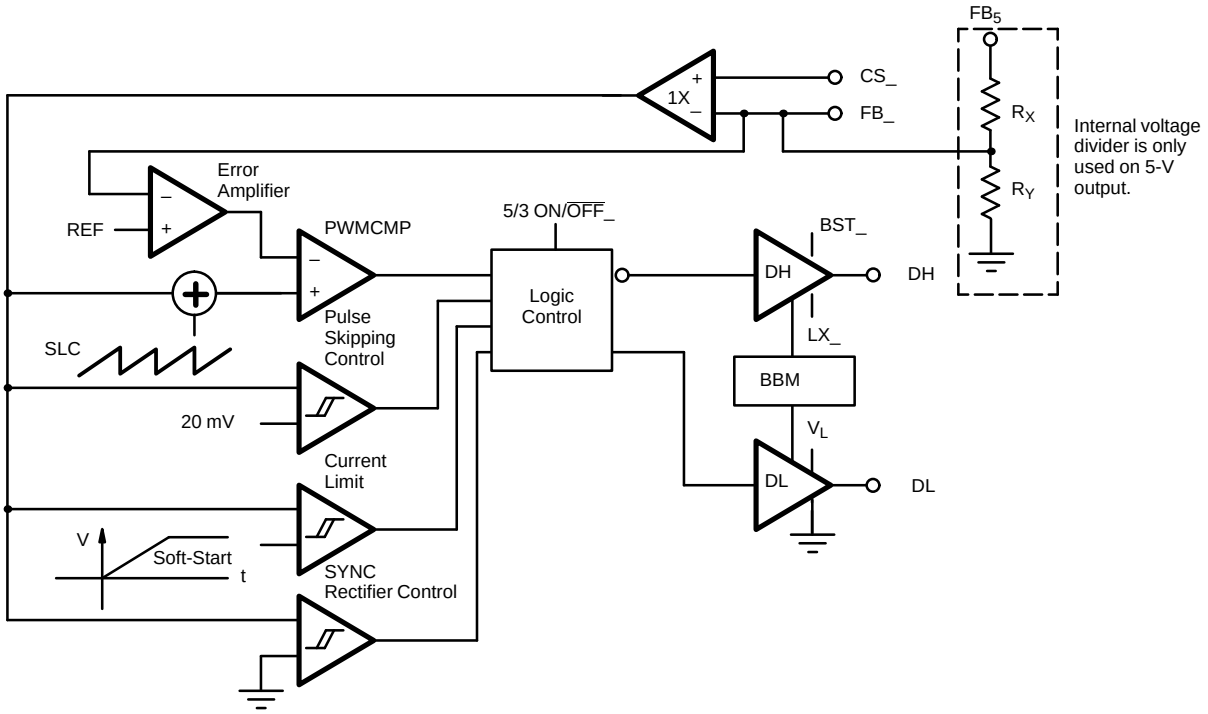

FIGURE 5. Buck Block Diagram

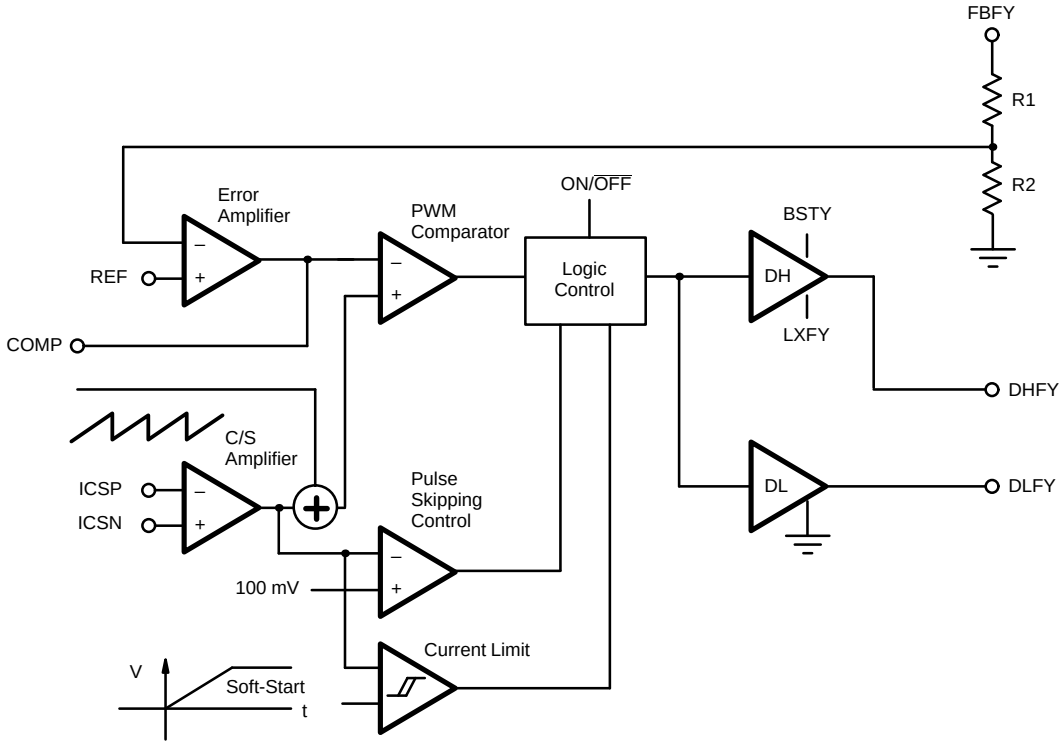

FIGURE 6. PWM Flyback Block Diagram

DETAIL FUNCTIONAL BLOCK DIAGRAM

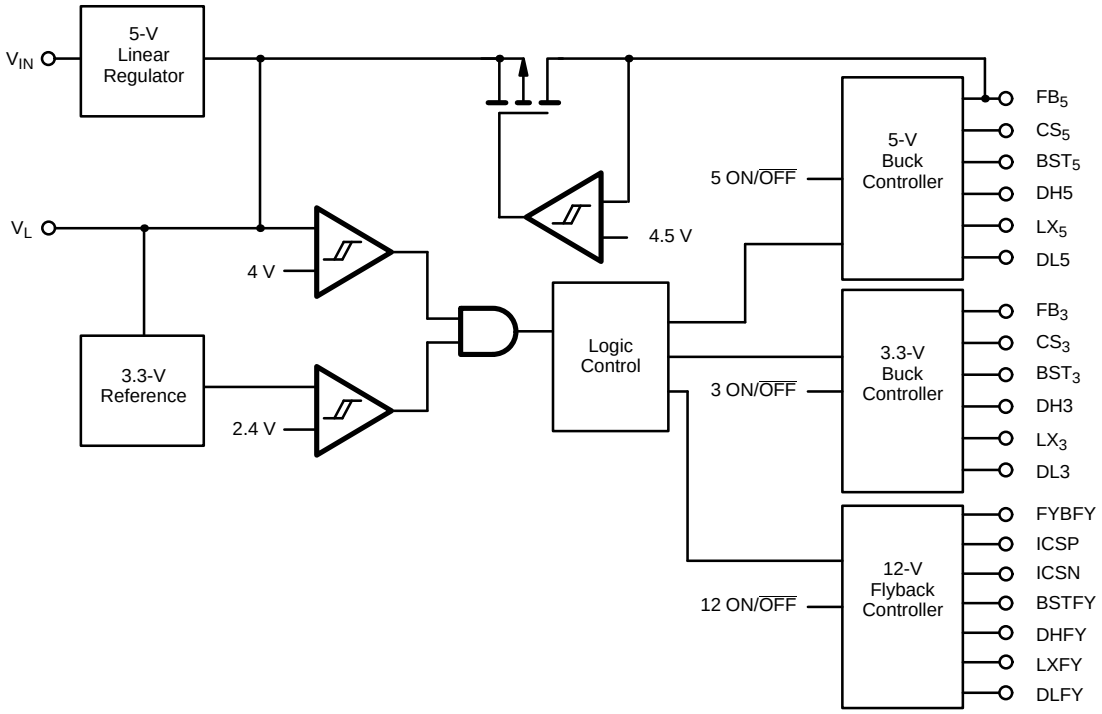

FIGURE 7. Complete Si9136 Block Diagram

DESCRIPTION OF OPERATION

Start-up Sequence

Si9136's outputs are controlled by three specific input control lines; 3.3 ON/$\overline{\text{OFF}}$, 5 ON/$\overline{\text{OFF}}$, and 12 ON/$\overline{\text{OFF}}$. Once V_{IN} is applied, the V_L, the 5-V LDO will come up within its tolerance. When any one of these control lines becomes logic high, the precision 3.3-V reference will also come up. Immediately afterwards, the oscillator will begin and the corresponding converter will come up with its own tolerance. In the event of all three converters are turned off, the oscillator and the reference output will be turned off, and the total system will only draw 35-μA of supply current.

Each converter can soft-start independently. This internal soft-start circuitry for each converter will gradually increases the inductor maximum peak current during the soft-start period (approximately 4 ms), preventing excessive currents from being drawn from the input.

Si9136 converts a 5.5-V to 30-V input voltage to five different output voltages; two buck (step-down) high current, PWM, switch-mode supplies of 3.3-V and 5-V, one "flyback" PWM switch-mode supply of 12-V, one precision 3.3-V reference and one 5-V low drop out (LDO) linear regulator output. Switch-mode supply output current capabilities depend on external components (can be selected to exceed 10 A). In the standard application circuit illustrated in Figure 1, each buck converter is capable of delivering 5 A, with the flyback converter delivering 250 mA. The recommended load currents for the precision 3.3-V reference output is less than 1 mA, and the 5-V LDO output is less than 30 mA. In order to maximize power efficiency of the converter, when the 5-V buck converter output (FB5) voltage is above 4.5-V, the internal 5-V LDO is turned off and V_L is supplied by the 5-V converter output.

Buck Converter Operation:

The 3.3-V and 5-V buck converters are both current-mode PWM and PSM (during light load operation) regulators using high-side bootstrap n-channel and low-side n-channel MOSFETs. At light load conditions, the converters switch at a lower frequency than the clock frequency, seen like some clock pulses between the actual switching are skipped, this operating condition is defined as pulse-skipping. The operation of the converter(s) switching at clock frequency is defined as normal operation.

DESCRIPTION OF OPERATION (CONT'D)

Normal Operation: Buck Converters

In normal operation, the buck converter high-side MOSFET is turned on with a delay (known as break-before-make time - t_{BBM}), after the rising edge of the clock. After a certain on time, the high-side MOSFET is turned off and then after a delay (t_{BBM}), the low-side MOSFET is turned on until the next rising edge of the clock, or the inductor current reaches zero. The t_{BBM} (approximately 25 ns to 60 ns), has been optimized to guarantee the efficiency is not adversely affected at the high switching frequency and a specified minimum to account for variations of possible MOSFET gate capacitances.

During the normal operation, the high-side MOSFET switch on-time is controlled internally to provide excellent line and load regulation over temperature. Both buck converters should have load, line, regulation to within 0.5% tolerance.

Pulse Skipping: Buck Converters

When the buck converter switching frequency is less than the internal clock frequency, its operation mode is defined as pulse skipping mode. During this mode, the high-side MOSFET is turned on until V_{CS}-V_{FB} reaches 20 mV, or the on time reaches its maximum duty ratio. After the high-side MOSFET is turned off, the low-side MOSFET is turned on after the t_{BBM} delay, which will remain on until the inductor current reaches zero. The output voltage will rise slightly above the regulation voltage after this sequence, causing the controller to stay idle for the next one, or several clock cycles. When the output voltage falls slightly below the regulation level, the high-side MOSFET will be turned on again at the next clock cycle. With the converter remaining idle during some clock cycles, the switching losses are reduced in order to preserve conversion efficiency during the light output current condition.

Current Limit: Buck Converters

When the buck converter inductor current is too high, the voltage across pin CS3(5) and pin FB3(5) exceeds approximately 120 mV, the high-side MOSFET would be turned off instantaneously regardless of the input, or output condition. The Si9136 features clock cycle by clock cycle current limiting capability.

Flyback Converter Operation:

Designed mainly for PCMCIA or EEPROM programming, the Si9136 has a 12-V output non-isolated buck boost converter, called for brevity a flyback. It consists of two n-channel MOSFET switches that are turned on and off in phase, and two diodes. Similar to the buck converter, during the light load conditions, the flyback converter will switch at a frequency lower than the internal clock frequency, which can be defined as pulse skipping mode (PSM); otherwise, it is operating in normal PWM mode.

Normal Operation: Flyback Converter

In normal operation mode, the two MOSFETs are turned on at the rising edge of the clock, and then turned off. The on time is controlled internally to provide excellent load, line, and temperature regulation. The flyback converter has load, line and temperature regulation well within 0.5%.

Pulse Skipping: Flyback Converter

Under the light load conditions, similar to the buck converter, the flyback converter will enter pulse skipping mode. The MOSFETs will be turned on until the inductor current increases to such a level that the voltage across the pin CSP and pin CSN reaches 100 mV, or the on time reaches the maximum duty cycle. After the MOSFETs are turned off, the inductor current will conduct through two diodes until it reaches zero. At this point, the flyback converter output will rise slightly above the regulation level, and the converter will stay idle for one or several clock cycle(s) until the output falls back slightly below the regulation level. The switching losses are reduced by skipping pulses and so the efficiency during light load is preserved.

Current Limit: Flyback Converter

Similar to the buck converter; when the voltage across pin CSP and pin CSN exceeds 410-mV typical, the two MOSFETs will be turned off regardless of the input and output conditions.

Flyback Lowside Drive

Unlike the gate drive for the two buck converters, the flyback lowside gate drive DLFY is powered by a voltage that can be as high as 15 V with 20-V input for the flyback converter. If this poses concerns on the MOSFET V_{GS} rating, a simple resistor-zener circuit can be used: a resistor series with gate and zener diode across the gate and source to clamp its voltage. A 100-Ω, 10-V combination works well.

DESCRIPTION OF OPERATION (CONT'D)

Grounding:

There are two separate grounds on the Si9136, analog signal ground (GND) and power ground (PGND). The purpose of two separate grounds is to prevent the high currents on the power devices (both external and internal) from interfering with the analog signals. The internal components of Si9136 have their grounds tied (internally) together. These two grounds are then tied together (externally) at a single point, to ensure Si9136 noise immunity.

This separation of grounds should be maintained in the external circuitry, with the power ground of all power devices being returned directly to the input capacitors, and the small signal ground being returned to the GND pin of Si9136.

ON/$\overline{\text{OFF}}$ Function

Logic-low shuts off the appropriate section by disabling the gate drive stage. High-side and low-side gate drivers are turned off when ON/OFF pins are logic-low. Logic-high enables the DH and DL pins.

Stability:

Buck Converters:

In order to simplify designs, the Si9136 requires no specified external components except load capacitors for stability control. Meanwhile, it achieves excellent regulation and efficiency. The converters are current mode control, with a bandwidth substantially higher than the LC tank dominant pole frequency of the output filter. To ensure stability, the minimum capacitance and maximum ESR values are:

$$C_{LOAD} \geq \frac{V_{REF}}{2\pi \times V_{OUT} \times R_{CS} \times BW} \qquad ESR \leq \frac{V_{OUT} \times Rcs}{V_{REF}}$$

Where V_{REF} = 3.3 V, V_{OUT} is the output voltage (5 V or 3.3 V), Rcs is the current sensing resistor in ohms and BW = 50 khz

With the components specified in the application circuit (L = 10 μH, RCS = 0.02 Ω, C_{OUT} = 330 μF, ESR approximately 0.1 Ω), the converter should have a bandwidth at approximately 50 kHz, with minimum phase margin of 65°, and dc gain above 50 dB.

Other Outputs

The Si9136 also provides a 3.3-V reference which can be external loaded up to 1 mA, as well as, a 5-V LDO output which can be loaded 30 mA, or even more depending on the system application. When the 5-V buck converter is turned on, the 5-V LDO output is shorted with the 5-V buck converter output, so its loading capability is substantially increased. For stability, the 3.3-V reference output requires a 1-μF capacitor, and 5-V LDO output requires a 4.7-μF capacitor.