Features

- Advanced, Catalog Speech Processor for High-Quality Sound, Capable of Unlimited Speech Duration Using External Memory
- Operates up to 12.32 MIPS.
- Supports High-Quality Algorithms Such as MX (1.0 Kbps – 3.5 Kbps at 8 kHz), CX (3.0 Kbps – 11.2 kHz at 8 kHz Sampling Rate), ADPCM, Single Channel FM with CX or MX.
- Speed and Pitch Shifting in MX for Various Voice Effects.
- Six Level Digital Gain Control.
- 4 User Configurable I/O's.

- Very Low-Power Operation, Ideal for Hand-Held Devices.
- Low-Voltage Operation, Sustainable by Three (3) Batteries.
- Three Reduced Power Standby Modes, Less Than 10 μA in Deep-Sleep Mode.
- Resistor-Trimmed Oscillator or 32.768 kHz Crystal Reference Oscillator.
- Direct Speaker Drive, 32 Ω (PDM).
- Interrupt Driven, 4 or 8-Bit Parallel Data Transfer Protocol.
- Available in Die Form or 64-Pin LQFP Package

Description

The SC-691 is a standard slave synthesizer from Sensory, Inc. that accepts compressed speech data from other microprocessors or microcontrollers and converts it to speech.

This allows the SC-691 to be used with a master microprocessor/microcontroller in various speech-related products such as security systems, learning aids, games, and toys. High quality, low bit-rate coders, easy interface with the master microcontroller, digital gain control, low power sleep mode, and low voltage operation makes this device ideal for products requiring long duration speech, less development cycle times, and peripheral device control through the slave device.

SC-691 Block Diagram
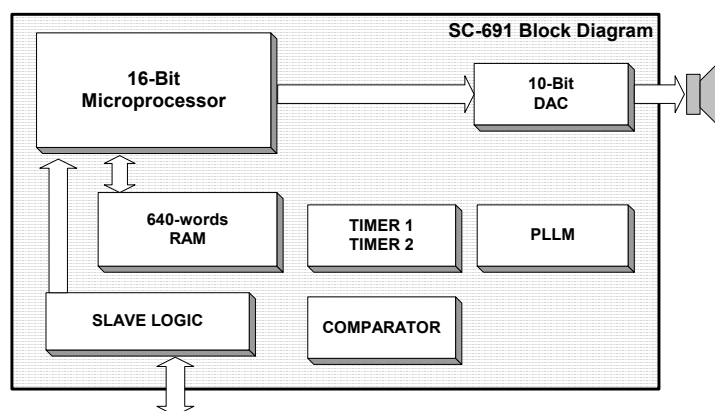
This device supports several speech synthesis algorithms that permit tradeoffs to meet the price performance requirements of various markets.
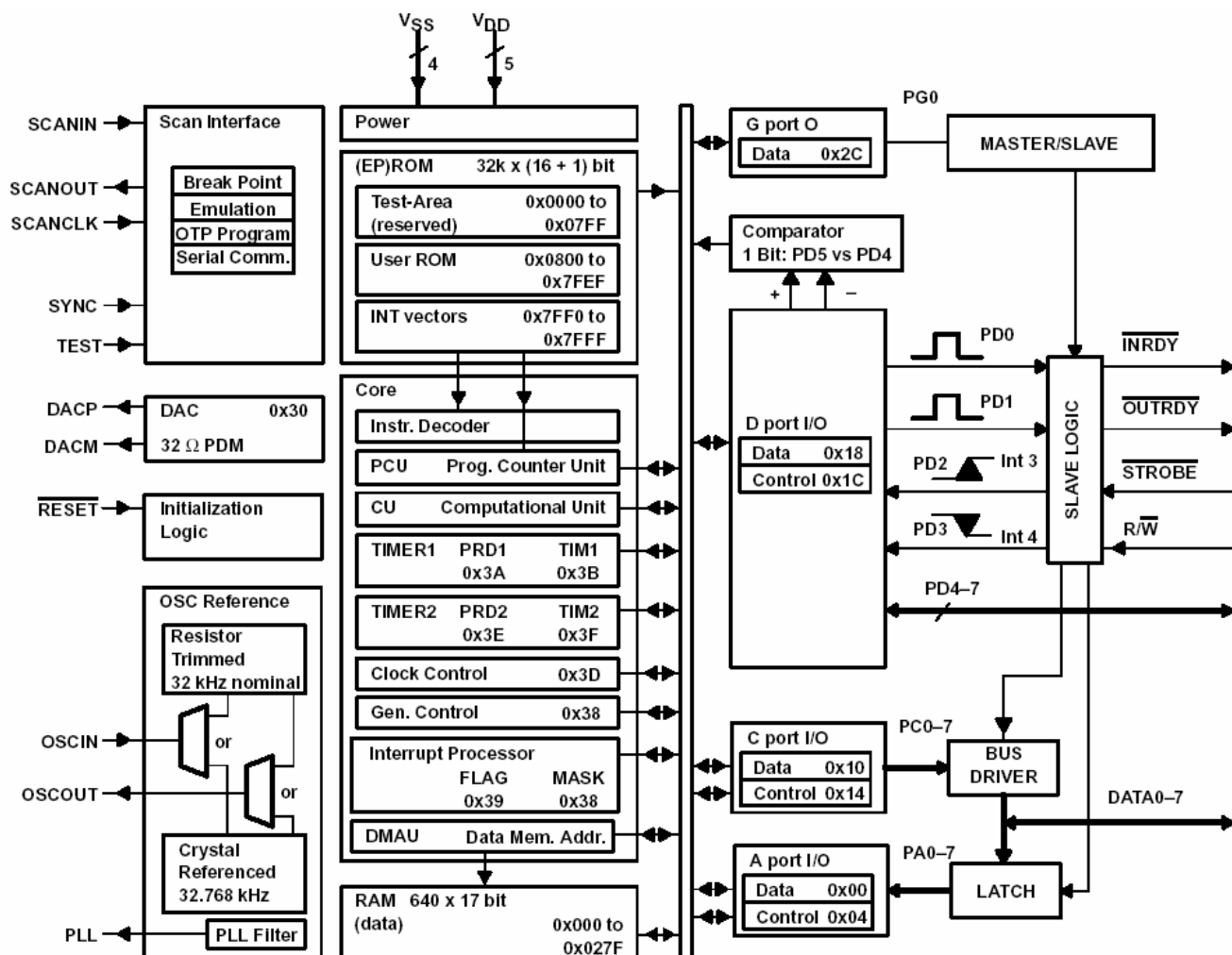
The SC-691 implements a unique feature of playing a single channel FM music along with CX or MX speech data concurrently. This feature allows the user to speak a certain phrase in MX or CX with single channel music in the background.

The SC-691 is optimized to support a 4-bit wide data transfer protocol. The device has two status bits and three control bits that control the communication protocol between the master and the slave.
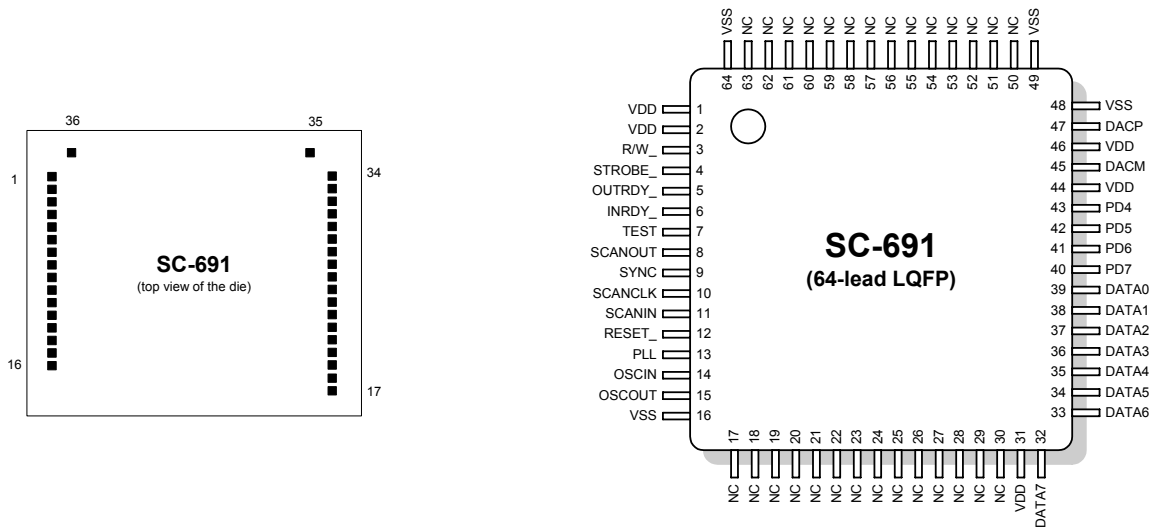
The SC-691 also has 1 bit (command/data) which differentiates between a command and speech data feeding into the slave. In 4-bit mode, various commands are sent to the slave during speech to perform various tasks.

The SC-691 also supports the 8-bit wide data transfer but the support for commands is disabled during speaking-a-phrase. When speaking-a-phrase in 8-bit mode is complete, the SC-691 switches back to the 4-bit mode to receive the next command. Switching between 4 bit mode and 8 bit mode is permitted between speech data files.

Functional Block Diagram

Pin/Pad Assignments

SC-691
(top view of the die)

SC-691
(64-lead LQFP)

NAME	PIN NO.	PAD NO.	I/O	DESCRIPTION
DATA0–DATA3	39 → 36	25 → 22	I/O	Data bits 0 through 3 (in 4-bit or 8-bit mode)
DATA4 or DATA/COMMAND	35	21	I/O	Data bit 4 (in 8-bit mode) NOTE: Pin 35 is DATA4 in 8-bit mode, or DATA/COMMAND in 4-bit mode.
DATA5–DATA7	34 → 32	20 → 18	I/O	Data bits 5 through 7 (8-bit mode only)
INRDY_	6	6	O	An output signal from the slave to the microcontroller. A low signal indicates that the SC-691 is ready to accept data or command. A high signal indicates that the SC-691 is busy and the microcontroller must not write any data or command to it
OUTRDY_	5	5	O	An output signal from the slave to the microcontroller. A low signal indicates that the SC-691 is ready to send data or command to the microcontroller.
PD4–PD7	43 → 40	29 → 26	I/O	General-purpose I/O bus
R/W_	3	3	I	An input signal to the slave from the microcontroller. Read/write select signal which is set high for read operations or set low for write operations by the microcontroller.
STROBE_	4	4	I	An input signal to the slave from the microcontroller. STROBE_ sequences read or write operations in conjunction with the R/W_ signal. This signal is pulsed high-low-high for read or write operations sequencing.
Reference Oscillator Signals				
OSCOUT	15	15	O	Output of resistor/crystal oscillator
OSCIN	14	14	I	Input to resistor/crystal oscillator
PLL	13	13	O	Output of phase-lock-loop filter
Scan Port Control Signals				
SCANIN[†]	11	39	I	Scan port data input
SCANOUT	8	35	O	Scan port data output
SCANCLK	10	38	I	Scan port clock
SYNC[†]	9	37	I	Scan port synchronization
TEST[†]	7	36	I	Test modes
Digital-to-Analog Sound Output				
DACP	47	33	O	Digital-to-analog plus output (+)
DACM	45	31	O	Digital-to-analog minus output(–)
Initialization				
RESET_	12	12	I	Device initialization
Power Signals				
V_{DD}	1, 2, 31, 44, 46[‡]	1, 2, 17, 30, 32[‡]	-	Processor power, 5 V nominal supply voltage
V_{SS}	16, 48, 49[‡], 64	16, 34[‡], 35, 36	-	Ground pin

† All pins must be N.C.
‡ Marked pins are V_{DD} and V_{SS} connections which service the DAC circuitry. These pins tend to sustain a higher current draw. A dedicated decoupling capacitor across these pins is therefore required.

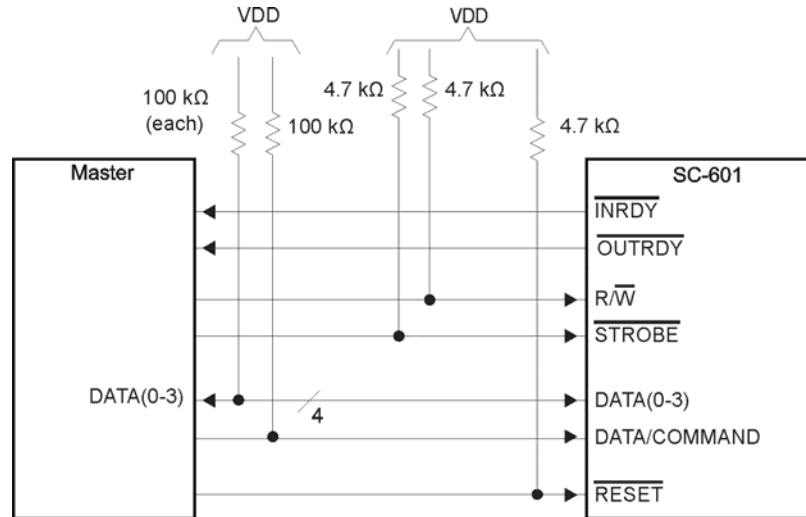|	SC-691 (4-bit mode)	SC-691 (8-bit mode)
Number of data lines	4	8
Number of control lines	3 (STROBE_, R/W_, data/command)	2 (STROBE_, R/W_)
Number of status lines	2 (INRDY_, OUTRDY_)	2 (INRDY_, OUTRDY_)
Number of general-purpose I/O lines	4	4
Support for commands (while speaking)	Yes	No

Figure 1: **Interfacing Diagram 4-Bit Mode**

Note:
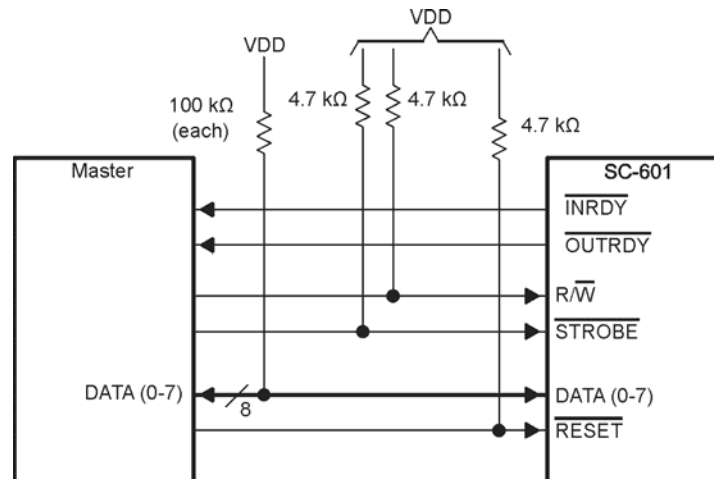|	
STROBE_	Active low STROBE_ signal from microcontroller
R/W_	Read/write signal from microcontroller
RESET_	Active low RESET_ signal from microcontroller
DATA0–	DATA3 Data bits 0 through 3
PD4–PD7	General-purpose I/O bus
DACP	Output to speaker/amplifier
DACM	Output to speaker/amplifier
DATA/COMMAND	This bit determines if the data sent by the microcontroller is data or command.

Figure 2: **Interfacing Diagram 8-Bit Mode**

Note:
|	
STROBE_	Active low STROBE_ signal from microcontroller
R/W_	Read/write signal from microcontroller
RESET_	Active low RESET_ signal from microcontroller.
INRDY_	Active low indicates that the SC-691 is ready to accept data.
OUTRDY_	Active low indicates that the SC-691 is ready to send data.
DATA0–DATA7	Data bits 0 through 7
PD4–PD7	General-purpose I/O bus
DACP	Output to speaker/amplifier
DACM	Output to speaker/amplifier

Read Operation By The Master

The process for the read operation by the master is the same in either 4-bit or 8-bit mode. The read operation by the master happens when the slave wants to send something to the master. The read process is initiated by the slave by pulling OUTRDY_ low when it is ready.

The following events take place during the read operation:

- ▸ The SC-691 puts the data to be sent to the master on the internal bus.
- ▸ The SC-691 sets OUTRDY_ low to indicate that it is ready to send data to the microcontroller.
- ▸ The microcontroller sets R/W_ high to indicate a read operation.
- ▸ The microcontroller sets STROBE_ low. The data is available on the external data-bus at this point.
- ▸ The microcontroller reads the data from the bus.
- ▸ The microcontroller sets STROBE_ high. The SC-691 also pulls OUTRDY_ high at the rising edge of STROBE_.
- ▸ The data is taken from the external data-bus after STROBE_ goes high.

The microcontroller should latch or read in the data while STROBE is low. When the microcontroller sets STROBE_ high, the SC-691 sets OUTRDY_ high to indicate that the data has been successfully transferred.

A) Sequence of events for a single read operation:
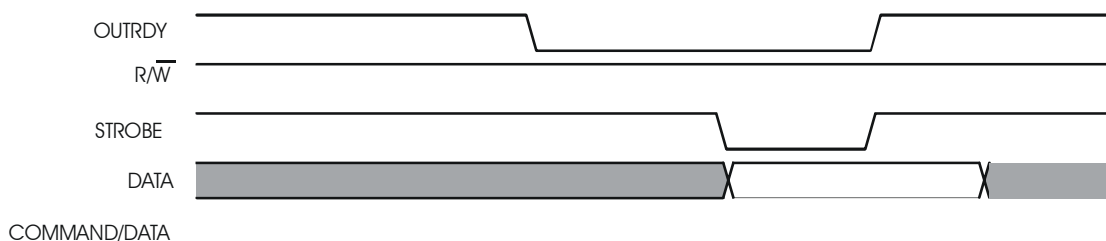
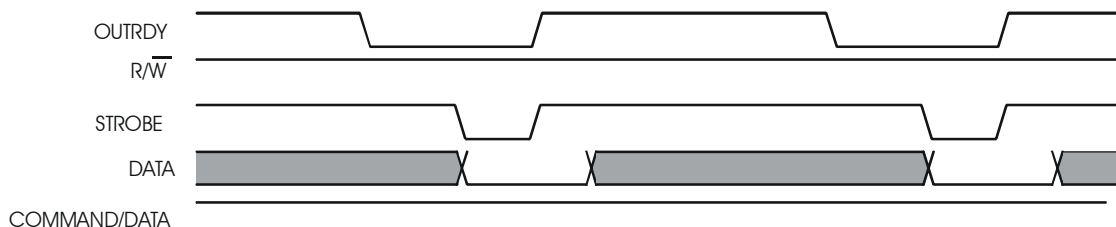B) Read-Two speech data transfer sequences:
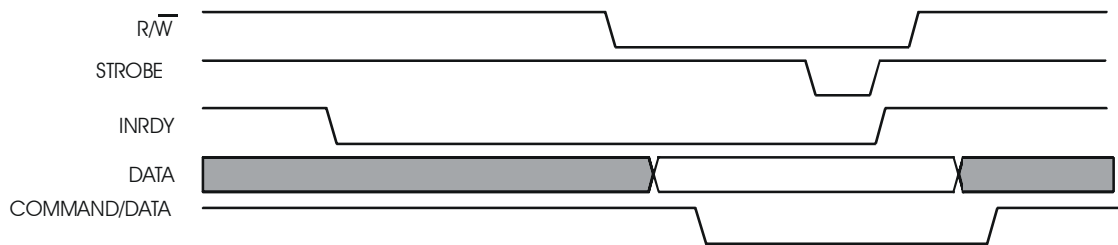

Figure 3: **Data Transfer – Read**

Write Operation By The Master

The process for the write operation by the master is the same in either 4-bit or 8-bit mode. The write operation by the master happens when the slave is ready to request data or command from the master. The write process is initiated by the slave by pulling INRDY_ low when the slave is ready to receive data. The following events take place during the write operation:

- ▸ The SC-691 sets INRDY_ low to indicate that it is ready to receive data from the microcontroller.
- ▸ The microcontroller sets R/W _low to indicate a write operation.
- ▸ The microcontroller puts the data in the external data-bus.
- ▸ The microcontroller sets STROBE_ low after the data is valid.
- ▸ The microcontroller sets STROBE_ high after a minimum of 300 ns. The SC-691 also pulls INRDY_ high at the rising edge of STROBE_.
- ▸ The data is latched in the SC-691 at the rising edge of STROBE_.

When the microcontroller sets STROBE_ high, the SC-691 sets INRDY__ high to indicate that the SC-691 is not ready to receive any more data.

A) Sequence of events for a single write operation:

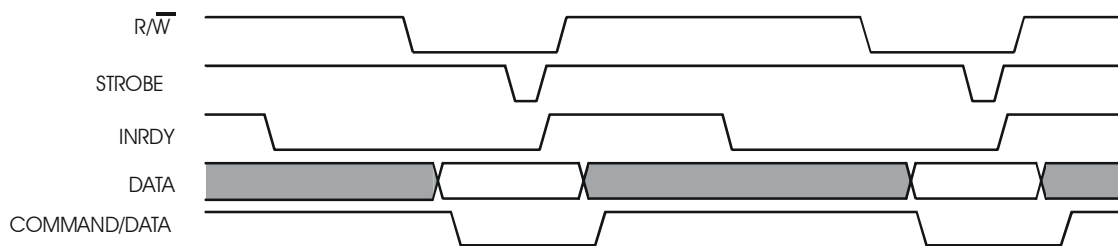B) Read-Two speech data transfer sequences:

Figure 4: **Data Transfer - Write**

Absolute Maximum Ratings

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	-0.3 to 7 V
Supply current, I_{DD} (see Note 2)	35 mA
Input voltage range, V_I (see Note 1)	-0.3 to V_{DD} + 0.3 V
Output voltage range, V_O (see Note 1)	-0.3 to V_{DD} + 0.3 V
Storage temperature range, T_A	-30°C to 125°C

WARNING:
Stressing the SC-691 beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltages are measured with respect to V_{SS}.
2. The total supply current includes the current out of all the I/O pins as well as the operating current of the device.

Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage (with respect to V_{SS}), V_{DD}		3	5.2	V
CPU clock rate (as programmed), $f_{(CPU)}$		64	12,320	kHz
Load resistance between DAC_P and DAC_M, $R_{(DAC)}$		32		Ω
Operating free-air temperature, T_A	Device functionality	0	70	°C

Timing Requirements

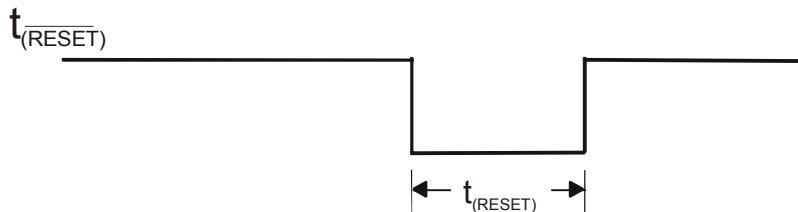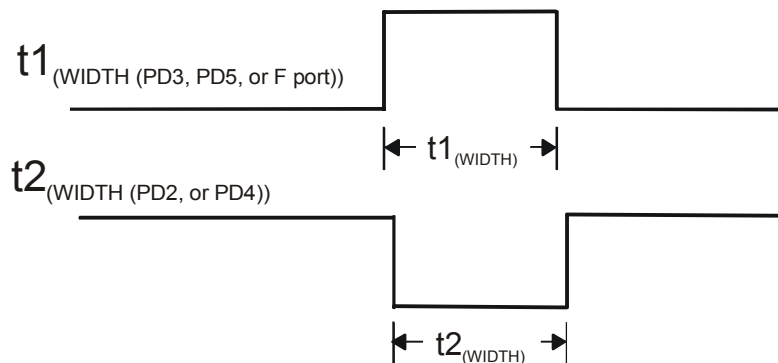|		MIN	MAX	UNIT
$t_{(RESET)}$	Reset_ low pulse width, while V_{DD} is within specified limits	100		ns
$t1_{(WIDTH)}$	Pulse width required prior to a negative transition at pin (PD3 or PD5 interrupt)	2		$1/F_{CPU}$
$t2_{(WIDTH)}$	Pulse width required prior to a positive transition at pin (PD2 or PD4 interrupt)	2		$1/F_{CPU}$

Figure 5: **Initialization Timing Diagram**

Figure 6: **SC-691 External Interrupt Pin Pulse Width Requirements $t1_{WIDTH}$ and $t2_{WIDTH}$**

DC Electrical Characteristics, TA = 0 to 70°C

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
RESET_	Threshold changes	V_{DD} = 3 V	Positive going threshold		2.4		V
			Negative going threshold		1.8		
			Hysteresis		0.6		
		V_{DD} = 5.2 V	Positive going threshold		3.3		V
			Negative going threshold		2.9		
			Hysteresis		0.4		
V_{IH}	High-level input voltage	V_{DD} = 3 V		2		3	V
		V_{DD} = 4.5 V		3		4.5	
		V_{DD} = 5.2 V		3.5		5.2	
V_{IL}	Low-level input voltage	V_{DD} = 3 V		0		1	V
		V_{DD} = 4.5 V		0		1.5	
		V_{DD} = 5.2 V		0		1.7	
I_{OH}¶	High-level output current per pin of I/O port	V_{DD} = 4.5 V	V_{OH} = 4 V			−2	mA
I_{OL}¶	Low-level output current per pin of I/O port		V_{OL} = 0.5 V			5	mA
$I_{OH (DAC)}$	High-level output DAC current		V_{OH} = 4 V			−10	mA
$I_{OL (DAC)}$	Low-level output DAC current		V_{OL} = 0.5 V			20	mA
I_{lkg}	Input leakage current	Excludes OSC_{IN}				1	µA
$I_{(STANDBY)}$	Standby current	RESET is low			0.05	10	µA
I_{DD}†	Operating current	V_{DD} = 4.5 V, F_{CLOCK} = 12.32 MHz			15		mA
$I_{(SLEEP-deep)}$	Supply current	V_{DD} = 4.5 V, DAC off, ARM set, OSC disabled			0.05	10	µA
$I_{(SLEEP-mid)}$		V_{DD} = 4.5 V, DAC off, ARM set, OSC enabled			40	60	
$I_{(SLEEP-light)}$		V_{DD} = 4.5 V, DAC off, ARM clear, OSC enabled			60	100	
V_{IO}	Input offset voltage	V_{DD} = 4.5 V, V_{ref} = 1 to 4.25 V			25	50	mV
$R_{(PULLUP)}$	F port pullup resistance	V_{DD} = 5 V		70	150		KΩ
$\Delta f_{(RTO-trim)}$	Trim deviation	R_{RTO} = 470 KΩ, V_{DD} = 4.5 V, T_A = 25°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±1%	±3%	
$\Delta f_{(RTO-volt)}$	Voltage deviation	R_{RTO} = 470 KΩ, V_{DD} = 3.5 to 5.2 V, T_A = 25°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡				±1.5%	
$\Delta f_{(RTO-temp)}$	Temperature deviation	R_{RTO} = 470 KΩ, V_{DD} = 4.5 V, T_A = 0 to 70°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±0.03		%/°C
$\Delta f_{(RTO-res)}$	Resistance deviation	V_{DD} = 4.5 V, T_A = 25°C, $R_{(OSC)}$ = 470 KΩ at ±1%, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±1%		

† Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.
‡ The best trim value is selected at nominal temperature and voltage but the deviation due to the trim error is ignored.
§ Typical voltage and current measurement taken at 25°C
¶ This parameter cannot exceed 15 mA total per internal V_{DD} pin. Port C and port D share 1 internal V_{DD}. Ports A and G0 are used internally.

External Component Absolute Values

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{(RTO)}$	RTO external resistance	T_A = 25°C, 1% tolerance		470	KΩ
$C_{(PLL)}$	PLL external capacitance	T_A = 25°C, 10% tolerance		3300	pF

Mechanical Data

LQFP 64 PLASTICQUAD FLATPACK (10x10x1.4 mm)
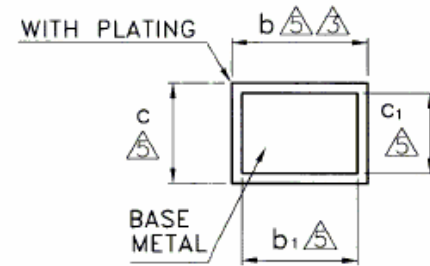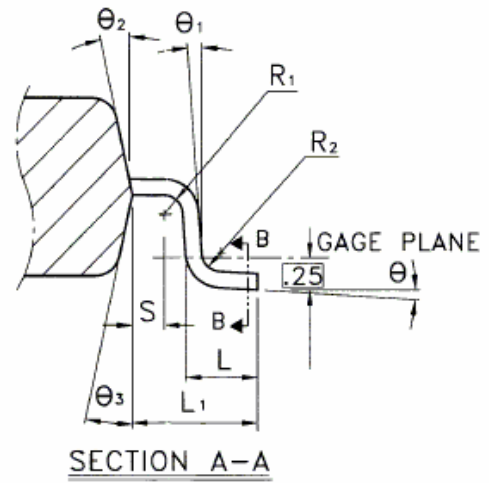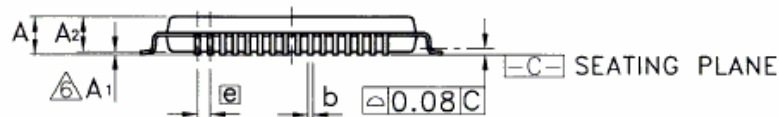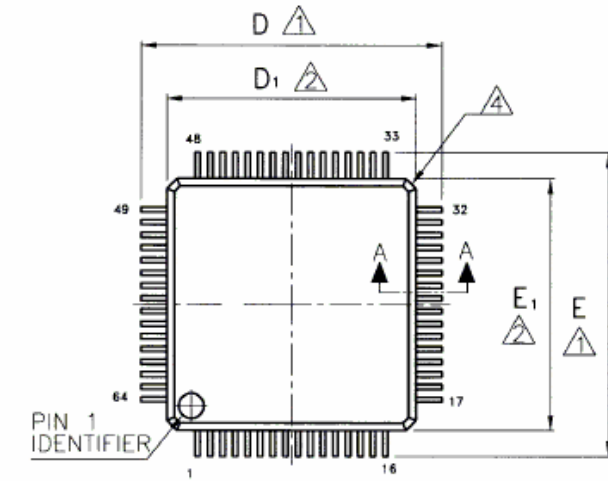
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	-	0.20	0.004	-	0.008
c1	0.09	-	0.16	0.004	-	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.50 BSC			0.20 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 BSC		
R1	0.08	-	-	0.003	-	-
R2	0.08	-	0.20	0.003	-	0.008
S	0.20	-	-	0.008	-	-
θ	0º	3.5º	7º	0º	3.5º	7º
$\theta1$	0º	-	-	0º	-	-
$\theta2$	12º TYP			12º TYP		
$\theta3$	12º TYP			12º TYP		

Notes:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022

Die Bond-out Coordinates

Die Size = **147.64 x 111.02 Mil**
Pad Size = **210 x 210 Mil**
Units = **Metric**

Pad	Pin	X-Axis Min	Y-Axis Min	X-Axis Max	Y- Axis Max
1	1	149.00	2122.80	235.00	2208.80
2	2	149.00	1961.45	235.00	2047.45
3	3	127.40	1805.45	213.40	1891.45
4	4	127.40	1651.45	213.40	1737.45
5	5	127.40	1497.45	213.40	1583.45
6	6	127.40	1343.45	213.40	1429.45
7	7	127.30	1191.05	213.30	1277.05
8	8	127.40	1077.95	213.40	1163.95
9	9	127.30	925.45	213.30	1011.45
10	10	127.30	814.15	213.30	900.15
11	11	127.30	702.85	213.30	788.85
12	12	127.45	555.50	213.45	641.50
13	13	127.30	435.50	213.30	521.50
14	14	127.30	324.20	213.30	410.20
15	15	127.30	212.90	213.30	298.90
16	16	148.00	108.10	234.00	194.10
17	31	3385.20	61.50	3471.20	147.50
18	32	3472.20	172.75	3558.20	258.75
19	33	3472.20	326.75	3558.20	412.75
20	34	3472.20	480.75	3558.20	566.75
21	35	3472.20	634.75	3558.20	720.75
22	36	3472.20	788.75	3558.20	874.75
23	37	3472.20	942.75	3558.20	1028.75
24	38	3472.20	1096.75	3558.20	1182.75
25	39	3472.20	1250.75	3558.20	1336.75
26	40	3472.20	1404.75	3558.20	1490.75
27	41	3472.20	1558.75	3558.20	1644.75
28	42	3472.20	1712.75	3558.20	1798.75
29	43	3472.20	1866.75	3558.20	1952.75
30	44	3450.60	2026.15	3536.60	2112.15
31	45	3517.01	2165.85	3603.01	2251.85
32	46	3517.01	2319.91	3603.01	2405.91
33	47	3517.01	2473.95	3603.01	2559.95
34	48	3516.80	2583.45	3602.80	2669.45
35	49	3149.35	2581.75	3235.35	2667.75
36	64	97.30	2533.65	183.30	2619.65

Ordering Information

Part	Ordering P/N	Shipping P/N	Description
SC-691 DIE	**SC691**	65-0140-A	Tested, Singulated SC-691 die in waffle pack.
SC-691 LQFP	**SC691-L1**	65-0139-A	SC-691 64 pin 10x10x1.4mm LQFP

The Interactive Speech™ Product Line

The Interactive Speech line of ICs and software was developed to "bring life to products" through advanced speech recognition and audio technology.

The Interactive Speech Product Line was designed for consumer telephony products and cost-sensitive consumer electronic applications such as home electronics, personal security, and personal communication.

The product line includes award-winning RSC series general-purpose microcontrollers and tools, SC series of speech microcontrollers, plus a line of easy-to-implement chips that can be pin-configured or controlled by an external host microcontroller. Sensory's software technologies run on a variety of microcontrollers and DSPs.

RSC Microcontrollers and Tools

The RSC product line contains low-cost 8-bit speech-optimized microcontrollers designed for use in consumer electronics. All members of the RSC family are fully integrated and include A/D, pre-amplifier, D/A, ROM, and RAM circuitry. The RSC family can perform a full range of speech/audio functions including speech recognition, speaker verification, speech and music synthesis, and voice record/playback. The family is supported by a complete suite of evaluation tools and development kits.

SC Microcontrollers and Tools

The SC-6x product line feature the highest quality speech synthesis ICs at the lowest data rate in the industry. The line includes a 12.32 MIPS processor for high-quality low data-rate speech compression and MIDI music synthesis, with plenty of power left over for other processor and control functions. Members of the SC-6x line can store as much as 37 minutes of speech on chip and include as much as 64 I/O pins for external interfacing. Integrating this broad range of features onto a single chip enables developers to create products with high quality, long duration speech at very competitive price points.

Application Specific Standard Products (ASSPs)

Voice Direct™ 364 provides inexpensive speaker-dependent speech recognition and speech synthesis. This easy-to-use, pin-configurable chip requires no custom programming and can recognize up to 60 trained words in slave mode, and 15 words in stand-alone mode. Ideal for speaker-dependent command and control of household consumer products, Voice Direct* 364 is part of a complete product line that includes the IC, module, and Voice Direct 364 Speech Recognition Kit.

Voice Extreme™ simplifies the creation of fully custom speech-enabled products by offering developers the capability of programming the chip in a high-level C-like language. Program code, speech data, and even record and playback information can be stored on a single off-chip Flash memory. Based on Sensory's RSC-364 speech processor, Voice Extreme includes a highly efficient on-chip code interpreter, and is supported by a comprehensive suite of low-cost development tools.

Software and Technology

Voice Activation™ micro footprint software provides advanced speech technology on a variety of microcontroller and DSP platforms. A flexible design with a broad range of technologies allows manufacturers to easily integrate speech functionality into consumer electronic products.

Fluent Speech™ small footprint software recognizes up to 50,000 words; offers Animated Speech with the ability to automate enunciation and articulation; performs text-to-speech synthesis in either male or female voices; provides noise and echo cancellation; performs Wordspotting for natural language usage; offers telephone barge-in; and provides continuous digit recognition.

Important notices

SENSORY®

1991 Russell Ave., Santa Clara, CA 95054
Tel: **(408) 327-9000** Fax: **(408) 727-4748**