PROTEK DEVICES®
.....Engineered solutions for the transient environment

SM8LC05 thru SM8LC24

HIGH SPEED TVS DIODE ARRAY

APPLICATIONS

- **Video-on-Demand**
- **ISDN Telecom Interface**
- **USB, ADSL & SCSI Interfaces**
- **Modems**
- **Portable Electronics**
- **LAN Interconnects**

FEATURES

- **IEC 1000-4-2, -4 & -5 Industry Requirements**
- **500 Watts Peak Pulse Power Dissipation per Line Pair (8/20 μs)**
- **ESD Protection > 40 kilovolts**
- **Low Capacitance: < 25 pF**
- **Available in 5 Voltage Types Ranging from 5.0V to 24V**
- **Standard SO-8 Package**
- **Two Line Pairs per Package**
- **Bidirectional Configurations**
- **UL 94V-0 Flammability Classification**

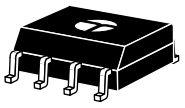
DESCRIPTION

The two (2) line pair SM8LC family is a series of low capacitance, silicon transient voltage suppressor (TVS) arrays designed for use in high-speed data rate applications. These devices provide board level ESD and EFT protection to sensitive I/O ports, TTL and MOS bus lines in accordance with IEC 1000-4-2, -4, -5 and European standard EN50082 and EN61000-4.

The SM8LC series has a peak pulse power rating (P_{PP}) of 500 Watts for an 8/20 μs waveshape. These devices can be used to protect combinations of two (2) bidirectional lines.

MAXIMUM RATINGS	
P_{PP} @ 25°C (See Figure 1)	500 Watts, 8/20 μs Waveshape
Operating & Storage Temperature	-55° to +150°C
Repetition Rate (Duty Cycle)	0.01%
$t_{Clamping}$ (0 Volts to $V_{(BR)}$ Min.)	Bidirectional: < 10 x 10^{-9} seconds
MECHANICAL CHARACTERISTICS	
Package	Molded SO-8 Surface Mount Package
Packaging	Tube or 12mm Tape per EIA 481
Approximate Weight	0.1 grams
Device Markings	Logo & Marking Code
Miscellaneous	Pin No. 1 Indicated by Dot on Top of Package

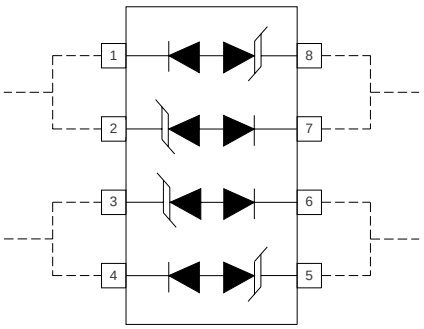
IEC 1000-4 COMPATIBLE



SO-8 PACKAGE

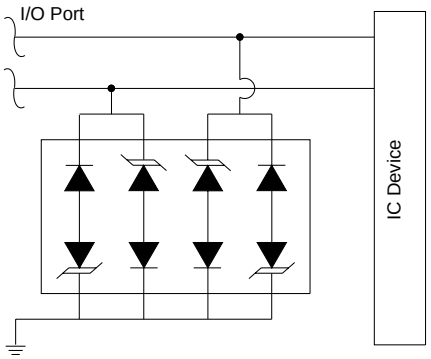
CIRCUIT DIAGRAM

SM8LC05
SM8LC08
SM8LC12
SM8LC15
SM8LC24



1. For Bidirectional applications, connect external pins 1 & 2, 3 & 4, 5 & 6, 7 & 8 as shown in the above circuit diagram.
2. Do not surge from pins 1 to 8, 7 to 2, 6 to 3 and 4 to 5. PIV typically greater than 100 Volts.

I/O PORT PROTECTION APPLICATION



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ELECTRICAL CHARACTERISTICS @ 25° C Ambient Temperature

PROTEK PART NUMBER	DEVICE MARKING CODE	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1 mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ I_P = 1 A V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ I_P = 10 A V_C VOLTS	MAXIMUM LEAKAGE CURRENT @ V_{WM} I_D µA	MAXIMUM CAPACITANCE @ 0V, 1 MHz C pF	TEMPERATURE COEFFICIENT OF $V_{(BR)}$ $\Theta V_{(BR)}$ mV/°C
SM8LC05	PGA	5.0	6.0	9.8	12.5	100	25	3
SM8LC08	PGB	8.0	8.5	13.3	16.6	10	25	6
SM8LC12	PGC	12.0	13.3	19.0	23.5	4	25	16
SM8LC15	PGD	15.0	16.7	25.5	29.5	4	25	17
SM8LC24	PGE	24.0	26.7	40.0	46.9	4	25	26

Note 1: Devices are designed to be used in parallel (See Circuit Diagram). For other applications, contact the factory. Do not surge in the "forward" direction of the TVS.
Note 2: Do not surge from pins 1 to 8, 7 to 2, 6 to 3 and 4 to 5. PIV typically greater than 100 Volts for each rectifier diode.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

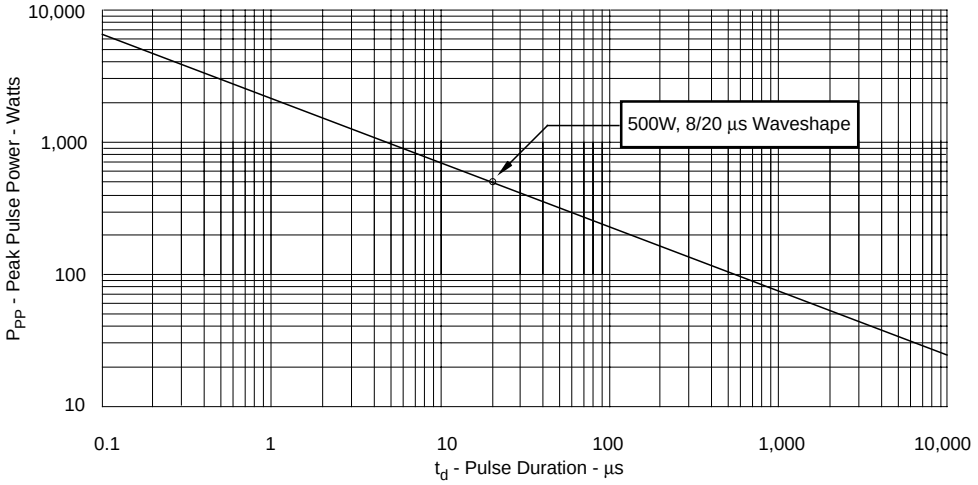


FIGURE 2
PULSE WAVE FORM

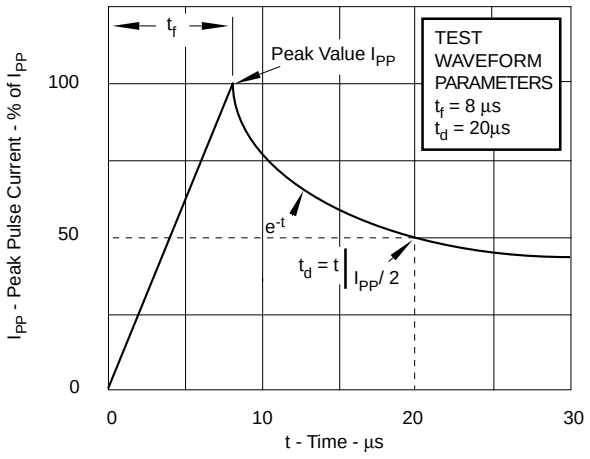
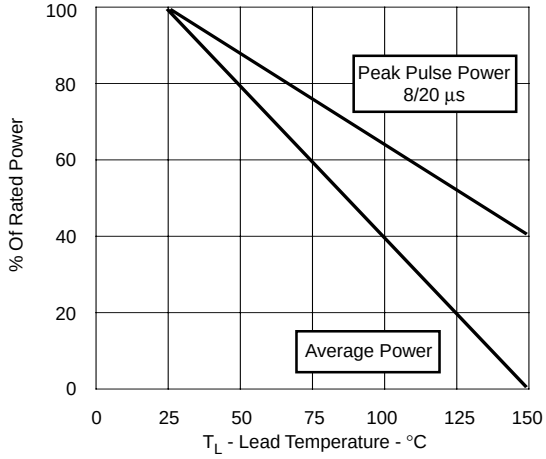
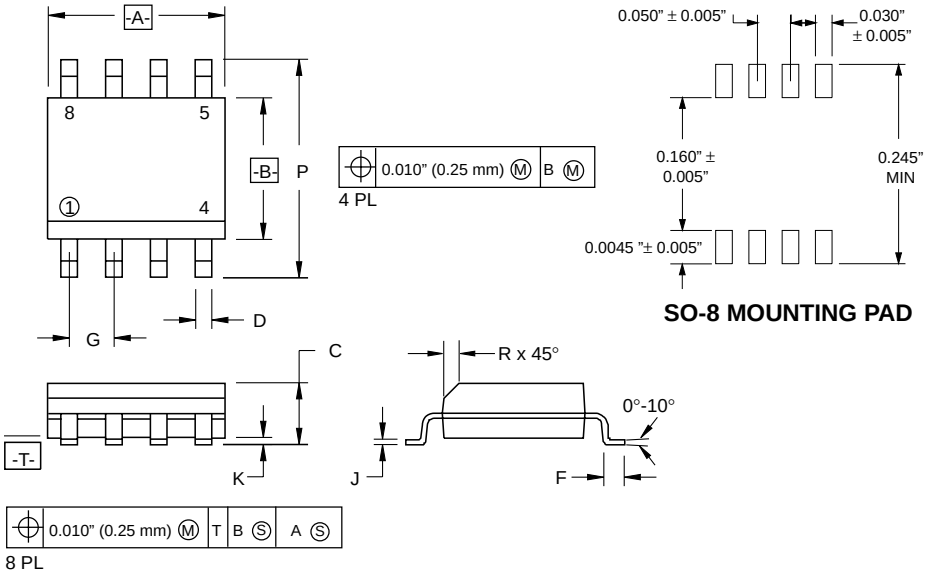


FIGURE 3
POWER DERATING CURVE



SO-8 PACKAGE OUTLINE



SO-8 MOUNTING PAD

SO-8 PACKAGE DIMENSIONS

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.250	0.016	0.049
G	1.27 BSC	1.27 BSC	0.05 BSC	0.05 BSC
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.008
P	5.78	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. - T - = Seating Plane
2. Dimension “A” is Datum.
3. Dimension “A” and “B” do not include mold protusion.
4. Maximum mold protusion is 0.15” (0.006 mm) per side.
5. Dimensioning and tolerances per ANSI Y14.5M, 1982.