SED1375 EMBEDDED MEMORY LCD CONTROLLER

September 1999

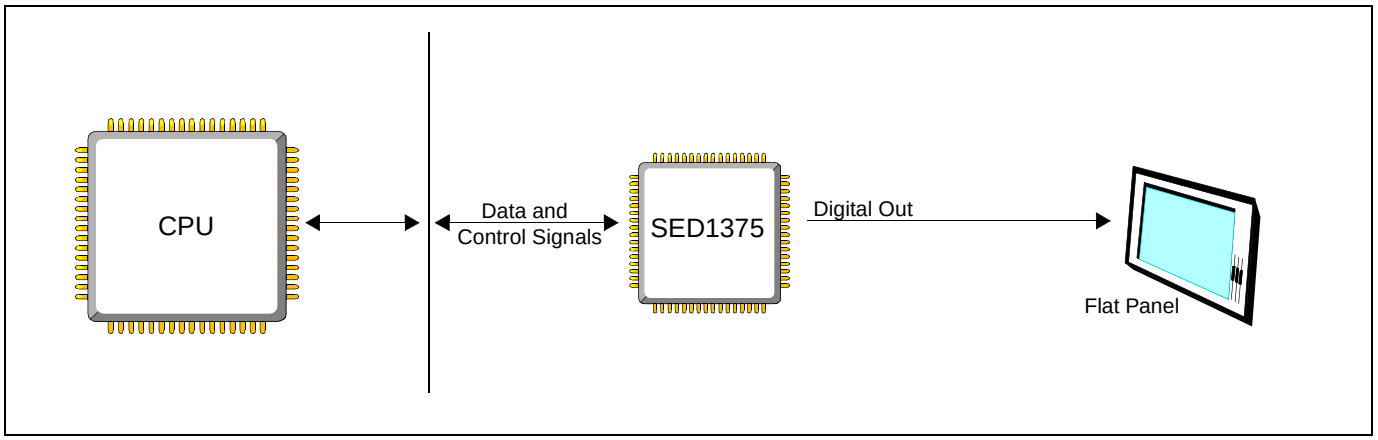
The SED1375 is a color/monochrome LCD graphics controller with an embedded 80K Byte SRAM display buffer. The high integration of the SED1375 provides a low cost, low power, single chip solution to meet the requirements of embedded markets such as Office Automation equipment, Mobile Communications devices, and Palm-size PCs where board size and battery life are major concerns.

Products requiring a “Portrait” display can take advantage of the Hardware Portrait Mode feature of the SED1375. Virtual and Split Screen are just some of the display modes supported. While focusing on devices targeted by the Microsoft Windows CE Operating System, the SED1375’s impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

■ FEATURES

- Embedded 80K byte SRAM display buffer.
- Direct support for the following CPU’s:
  - Hitachi SH-3.
  - Hitachi SH-4.
  - Motorola M68xxx.
  - MPU bus interface with programmable READY.
- Resolutions up to:
  - 640x480 at a color depth of 2 bpp.
  - 640x240 at a color depth of 4 bpp.
  - 320x240 at a color depth of 8 bpp.
- Up to 256 simultaneous colors from a possible 4096 colors on passive LCD panels and active matrix TFT/D-TFD LCD panels.
- Register level support for EL panels.
- Hardware Portrait Mode
- Split Screen Display
- Virtual Display Support
- LCD power-down sequencing.

■ SYSTEM BLOCK DIAGRAM



DESCRIPTION

Memory Interface

- Embedded 80K byte SRAM display buffer.

CPU Interface

- Direct support for:
  Hitachi SH-3.
  Hitachi SH-4.
  Motorola M68xxx.
  MPU bus interface with programmable READY.
- CPU write buffer.

Display Support

- 4/8-bit monochrome LCD interface.
- 4/8-bit color LCD interface.
- Single-panel, single-drive passive displays.
- Dual-panel, dual-drive passive displays.
- Active matrix TFT / D-TFD interface.
- Example resolutions:
  640x480 at a color depth of 2 bpp.
  640x240 at a color depth of 4 bpp.
  320x240 at a color depth of 8 bpp.

Clock Source

- Single clock input for both pixel and memory clocks.
- The SED1375 clock source can be internally divided down for a higher frequency clock input.

Display Modes

- 1/2/4/8 bit-per-pixel (bpp) support for LCD Panels.
- Up to 16 shades of gray using FRM on monochrome passive LCD panels.
- Up to 256 simultaneous colors from a possible 4096 colors on passive STN and active matrix TFT/D-TFD LCD panels.
- Split Screen Display: allows two different images to be simultaneously viewed on the same display.
- Virtual Display Support: displays images larger than the display size through the use of panning.
- Double Buffering/multi-pages: provides smooth animation and instantaneous screen update.
- Hardware Portrait Mode: direct hardware 90° rotation of display image for portrait mode display.

Power Down Modes

- Software Power Save mode.
- Hardware Power Save mode.
- LCD power-down sequencing.

Operating Voltage

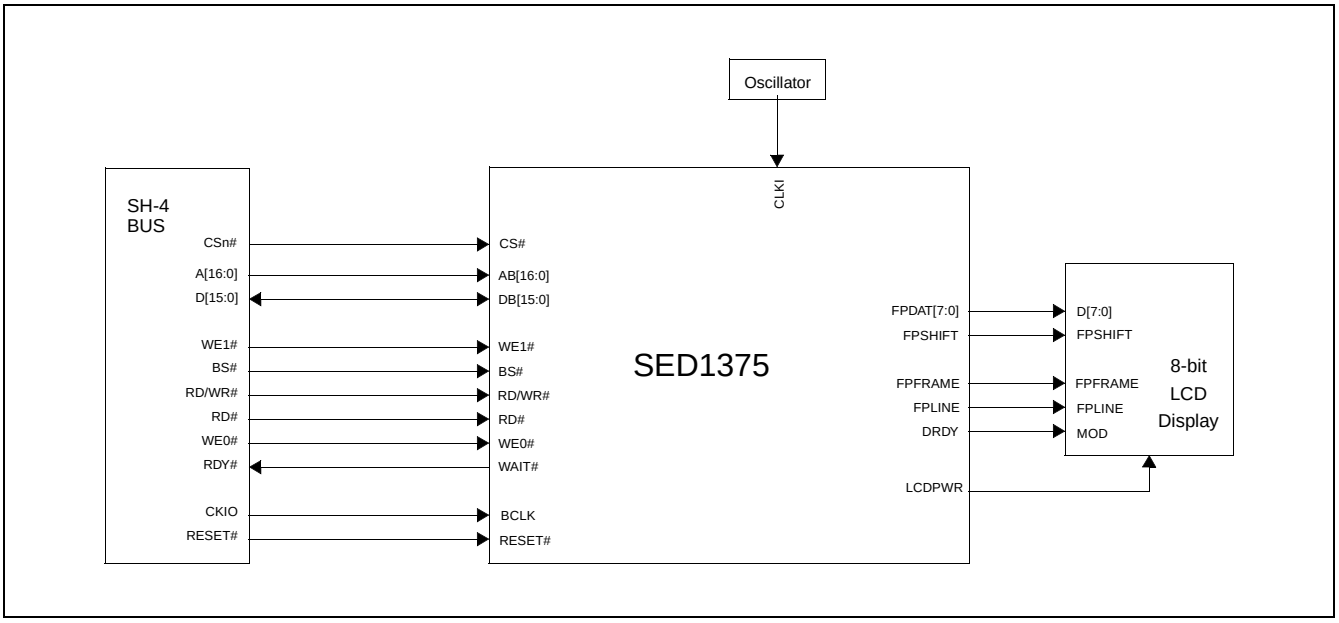
- $CORE_{VDD}$ 2.7 to 3.6 volts; IO_{VDD} 2.7 to 5.5 volts.

Package

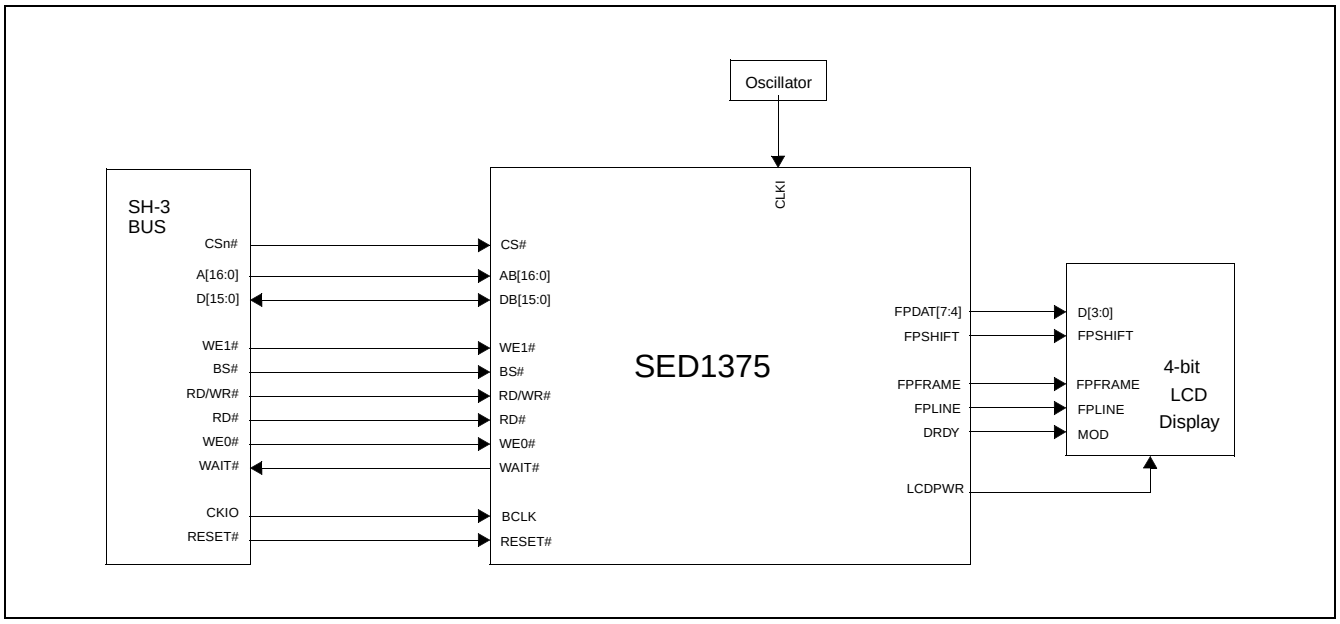
- 80-pin QFP14.

SYSTEM IMPLEMENTATION

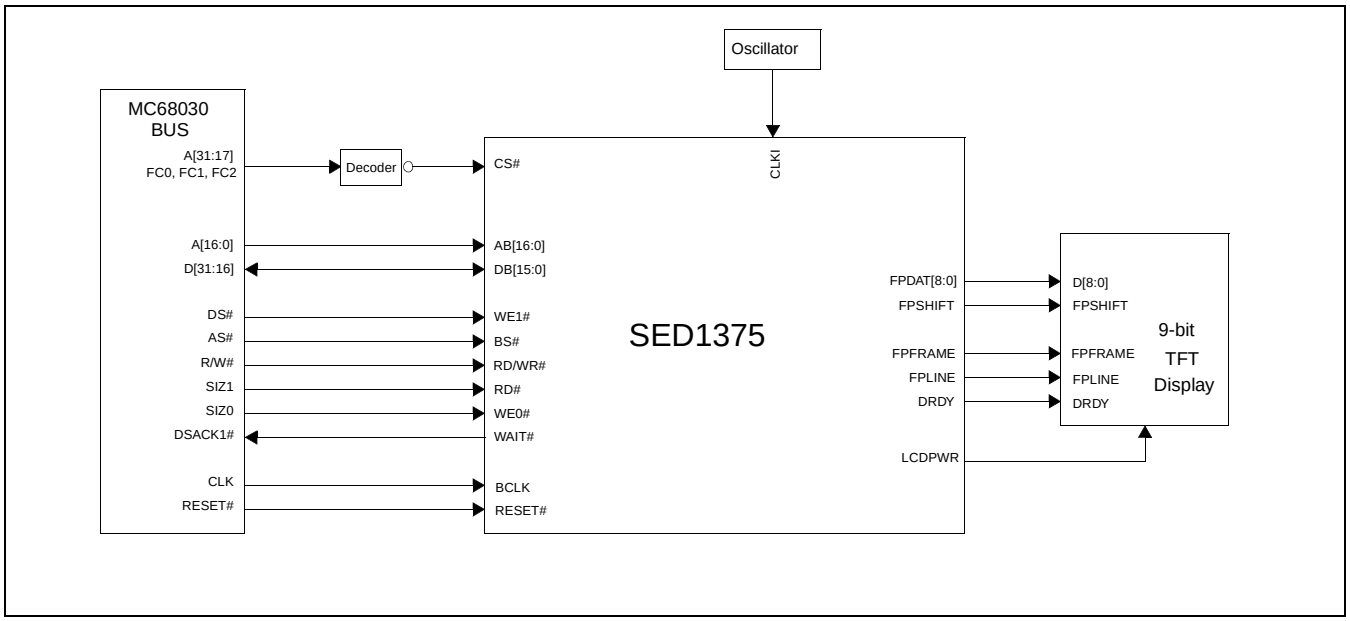
Example Implementation - SH-4 Bus, 8-Bit Passive LCD Panel



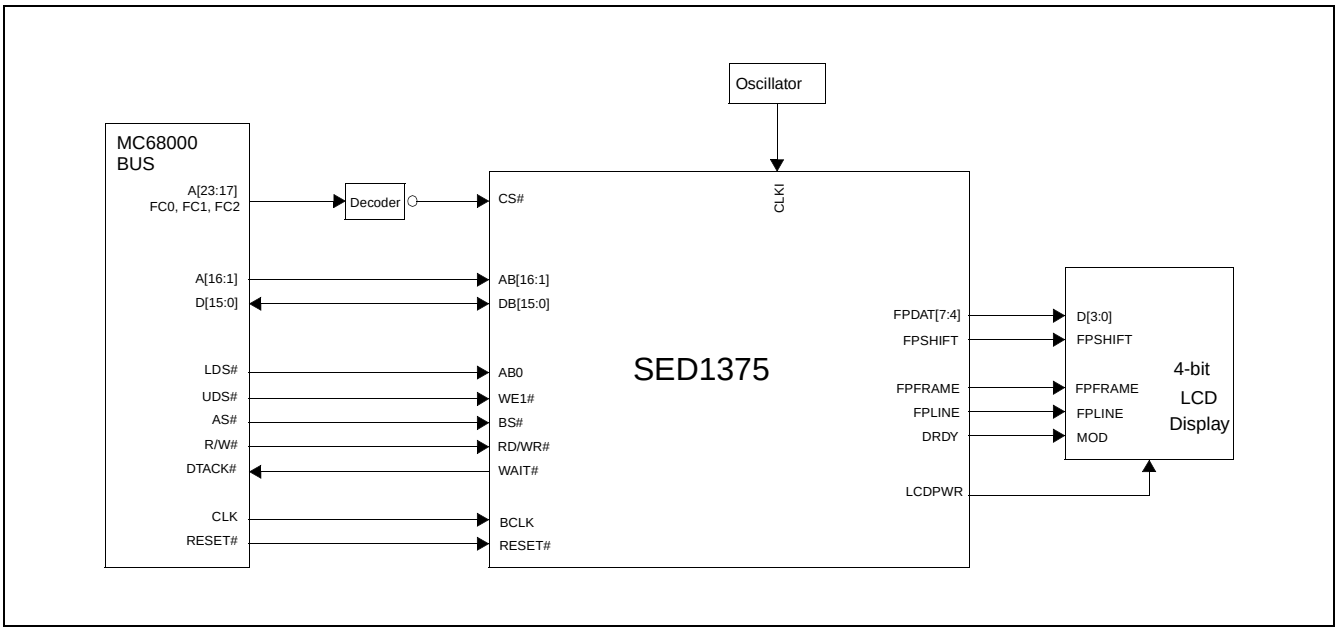
Example Implementation - SH-3 Bus, 4-Bit Passive LCD Panel



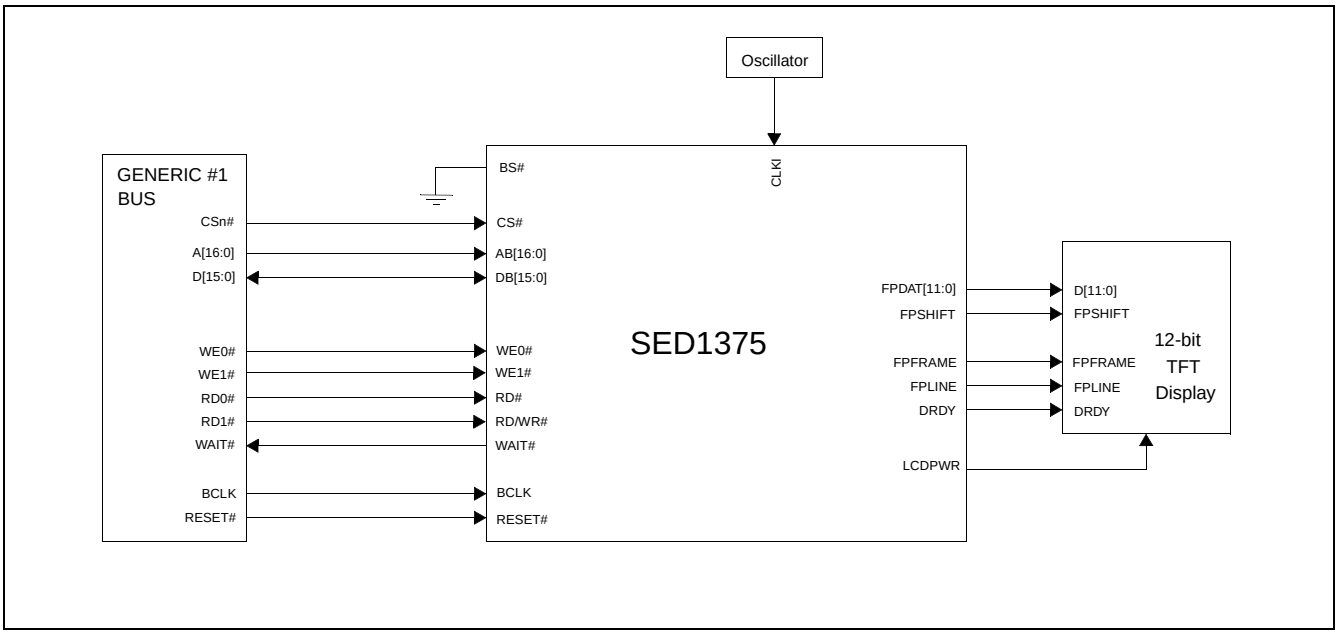
Example Implementation - 32-Bit 68030 Bus, 9-Bit Active TFT/D-TFD LCD Panel



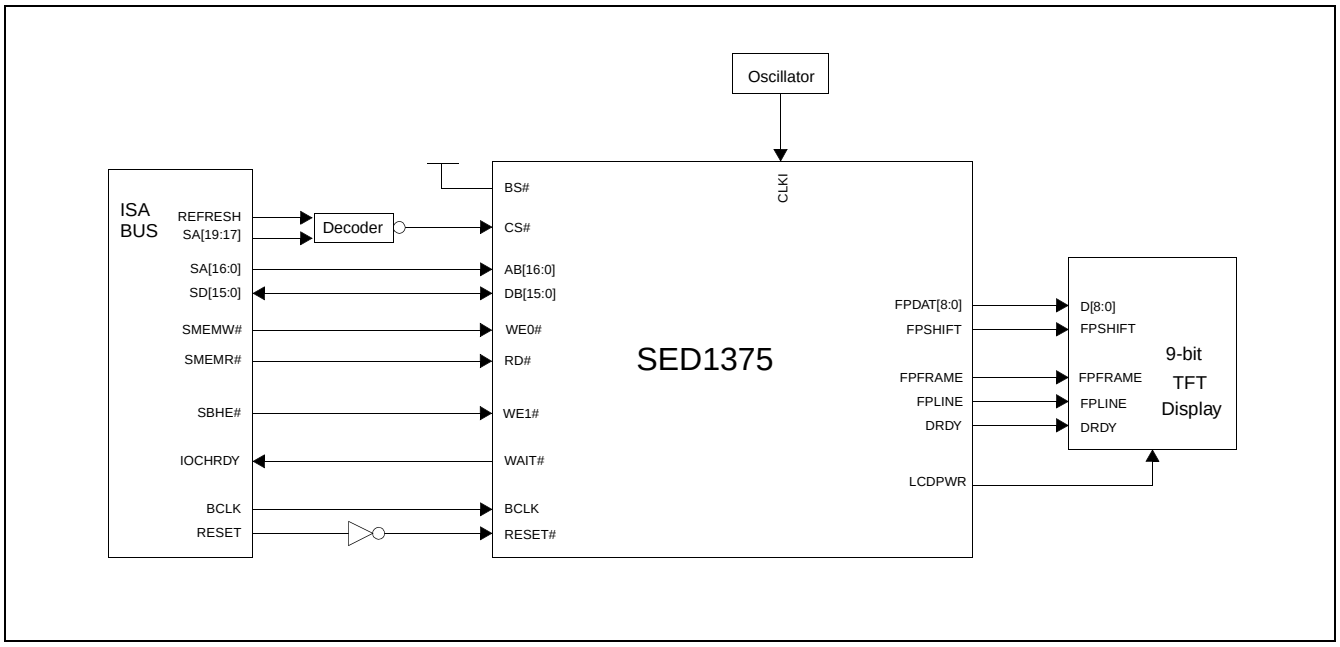
Example Implementation - 8-Bit 68000 Bus, 4-Bit Passive LCD Panel



Example Implementation - Generic #1 Bus, 12-Bit Active TFT/D-TFD LCD Panel



Example Implementation - Generic #2 Bus, 9-Bit Active TFT/D-TFD LCD Panel

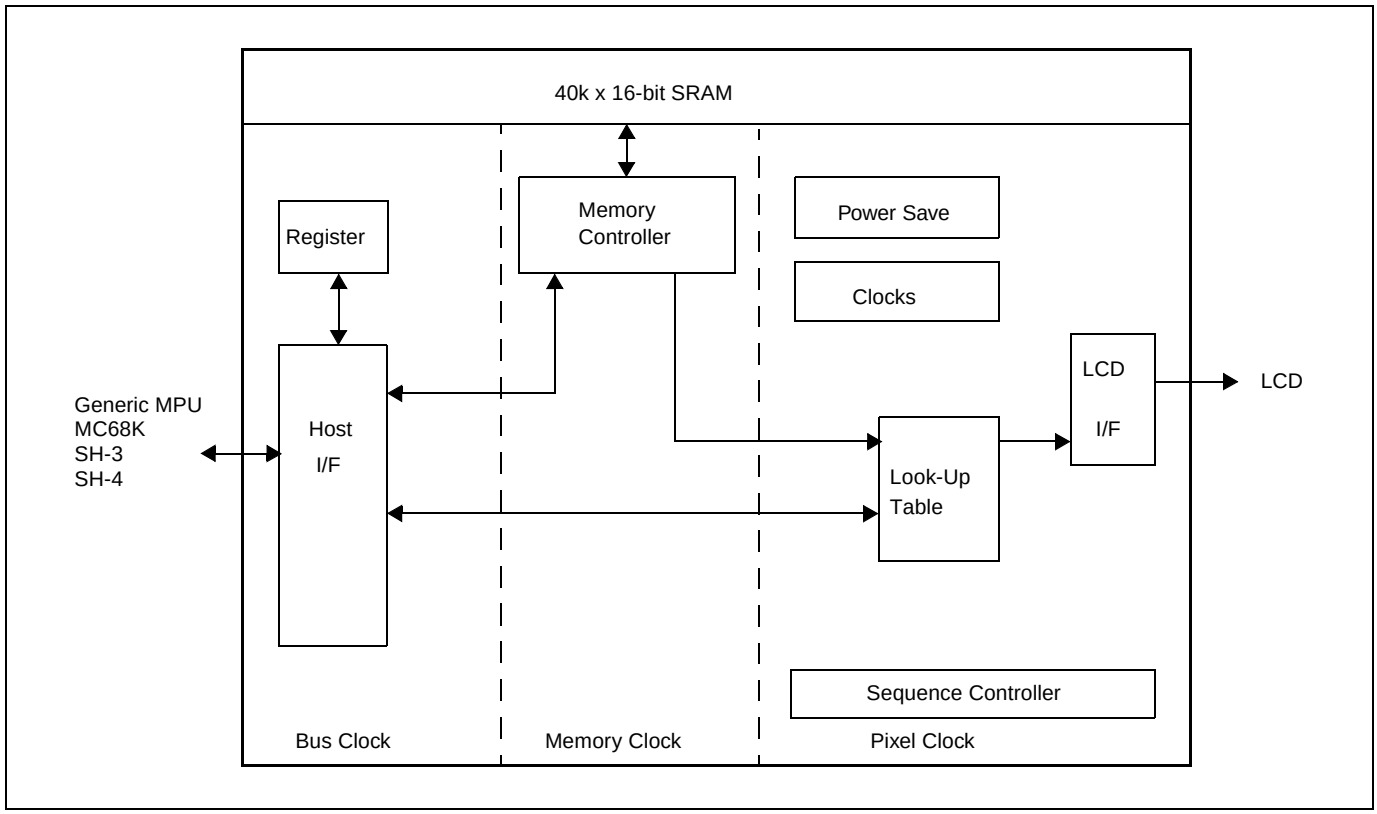


■ TYPICAL MODE SUPPORT

		Horizontal Pixels					
		100	**200**	**240**	**320**	**480**	**640**
Vertical Pixels	**100**	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4/8 bpp
	200	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4 bpp	1/2/4 bpp
	240	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4 bpp	1/2/4 bpp
	320	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4 bpp	1/2/4 bpp	1/2 bpp
	400	1/2/4/8 bpp	1/2/4/8 bpp	1/2/4 bpp	1/2/4 bpp	1/2 bpp	1/2 bpp
	480	1/2/4/8 bpp	1/2/4 bpp	1/2/4 bpp	1/2/4 bpp	1/2 bpp	1/2 bpp

Note
Color depth is limited by memory size.

■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

Host Interface

The Host Interface provides the means for the CPU/MPU to communicate with the display memory and internal registers.

Memory Controller

The Memory Controller arbitrates between CPU accesses and display refresh accesses. It also generates the necessary signals to control the SRAM frame buffer.

Sequence Controller

The Sequence Controller controls data flow from the Memory Controller through the Look-Up Table and to the LCD Interface. It also generates memory addresses for display refresh accesses.

Look-Up Table

The Look-Up Table contains three 256x4 look-up tables or palettes, one for each primary color. In monochrome mode only one of these look-up tables is used.

LCD Interface

The LCD Interface performs frame rate modulation for passive LCD panels. It also generates the correct data format and timing control signals for various LCD panels.

Power Save

Power Save contains the power save mode circuitry.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Supply Voltage	V_{SS} - 0.3 to 4.6	V
IO V_{DD}	Supply Voltage	V_{SS} - 0.3 to 6.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	° C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	° C

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Supply Voltage	V_{SS} = 0 V	2.7	3.0/3.3	3.6	V
IO V_{DD}	Supply Voltage	V_{SS} = 0 V	2.7	3.0/3.3/5.0	5.5	V
V_{IN}	Input Voltage		V_{SS}		IO V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	° C

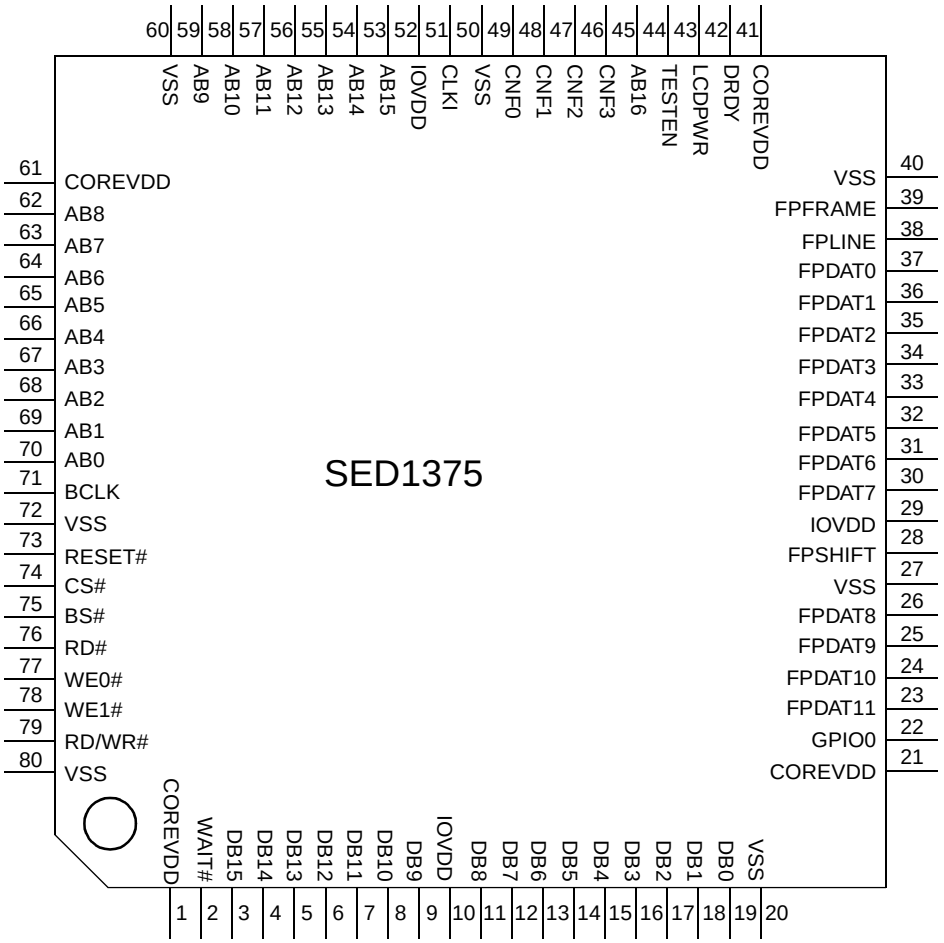
Input Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage CMOS inputs	IO V_{DD} = 3.0 3.3 5.0			0.8 0.8 1.0	V V V
V_{IH}	High Level Input Voltage CMOS inputs	IO V_{DD} = 3.0 3.3 5.0	1.9 2.0 3.5			V V V
V_{T+}	Positive-going Threshold CMOS Schmitt inputs	IO V_{DD} = 3.0 3.3 5.0	1.0 1.1 2.0		2.3 2.4 4.0	V V V
V_{T-}	Negative-going Threshold CMOS Schmitt inputs	IO V_{DD} = 3.0 3.3 5.0	0.5 0.6 0.8		1.7 1.8 3.1	V V V
I_{IZ}	Input Leakage Current	V_{DD} = Max V_{IH} = V_{DD} V_{IL} = V_{SS}	-1		1	µA
C_{IN}	Input Pin Capacitance				10	pF
HR_{PD}	Pull Down Resistance	V_I = V_{DD}	50	100	300	kΩ

Output Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Low Level Output Voltage Type 1 - TS1, CO1 Type 2 - TS2, CO2 Type 3 - TS3, CO3	 I_{OL} = 3mA I_{OL} = 6mA I_{OL} = 12mA			0.4	V
V_{OH}	High Level Output Voltage Type 1 - TS1, CO1 Type 2 - TS2, CO2 Type 3 - TS3, CO3	 I_{OL} = -1.5 mA I_{OL} = -3 mA I_{OL} = -6 mA	IO V_{DD} - 0.4			V
I_{OZ}	Output Leakage Current	V_{DD} = MAX V_{OH} = V_{DD} V_{OL} = V_{SS}	-1		1	µA
C_{OUT}	Output Pin Capacitance				10	pF
C_{BID}	Bidirectional Pin Capacitance				10	pF

■ SED1375 PIN OUT



Note
Package type: 80 pin surface mount QFP14

■ SED1375 PIN DESCRIPTION

Key:

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
C	=	CMOS level input
CD	=	CMOS level input with pull down resistor (typical values of 120KΩ/200KΩ at 5V/3.3V respectively)
CS	=	CMOS level Schmitt input
COx	=	CMOS output driver, x denotes driver type (1=3/-1.5mA, 2=6/-3mA, 3=12/-6mA)
TSx	=	Tri-state CMOS output driver, x denotes driver type (1=3/-1.5mA, 2=6/-3mA, 3=12/-6mA)
TSxD	=	Tri-state CMOS output driver with pull down resistor (typical values of 120KΩ/200KΩ at 5V/3.3V respectively), x denotes driver type (1=3/-1.5mA, 2=6/-3mA, 3=12/-6mA)
CNx	=	CMOS low-noise output driver, x denotes driver type (1=3/-1.5mA, 2=6/-3mA, 3=12/-6mA)

Host Interface

Pin Names	Type	Pin #	Cell	RESET# State	Description
AB0	I	70	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs system address bit 0 (A0). • For MC68K #1, this pin inputs the lower data strobe (LDS#). • For MC68K #2, this pin inputs system address bit 0 (A0). • For Generic #1, this pin inputs system address bit 0 (A0). • For Generic #2, this pin inputs system address bit 0 (A0). See “Host Bus Interface Pin Mapping” on page 14 for summary.
AB[16:1]	I	45, 53, 54, 55, 56, 57, 58, 59, 62, 63, 64, 65, 66, 67, 68, 69	C	Input	These pins input the system address bits 16 through 1 (A[16:1]).
DB[15:0]	IO	3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18, 19	C/TS2	Hi-Z	These pins have multiple functions. • For SH-3/SH-4 mode, these pins are connected to [D15:0]. • For MC68K #1, these pins are connected to D[15:0]. • For MC68K #2, these pins are connected to D[31:16] for a 32-bit device (e.g. MC68030) or D[15:0] for a 16-bit device (e.g. MC68340). • For Generic #1, these pins are connected to D[15:0]. • For Generic #2, these pins are connected to D[15:0]. See “Host Bus Interface Pin Mapping” on page 14 for summary.

Pin Names	Type	Pin #	Cell	RESET# State	Description
WE0#	I	77	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the write enable signal for the lower data byte (WE0#). • For MC68K #1, this pin must be tied to IO V_{DD} • For MC68K #2, this pin inputs the bus size bit 0 (SIZ0). • For Generic #1, this pin inputs the write enable signal for the lower data byte (WE0#). • For Generic #2, this pin inputs the write enable signal (WE#) See “Host Bus Interface Pin Mapping” on page 14 for summary.
WE1#	I	78	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the write enable signal for the upper data byte (WE1#). • For MC68K #1, this pin inputs the upper data strobe (UDS#). • For MC68K #2, this pin inputs the data strobe (DS#). • For Generic #1, this pin inputs the write enable signal for the upper data byte (WE1#). • For Generic #2, this pin inputs the byte enable signal for the high data byte (BHE#). See “Host Bus Interface Pin Mapping” on page 14 for summary.
CS#	I	74	C	Input	This pin inputs the chip select signal.
BCLK	I	71	C	Input	This pin inputs the system bus clock.
BS#	I	75	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the bus start signal (BS#). • For MC68K #1, this pin inputs the address strobe (AS#). • For MC68K #2, this pin inputs the address strobe (AS#). • For Generic #1, this pin must be tied to V_{SS}. • For Generic #2, this pin must be tied to IO V_{DD}. See “Host Bus Interface Pin Mapping” on page 14 for summary.
RD/WR#	I	79	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the RD/WR# signal. The SED1375 needs this signal for early decode of the bus cycle. • For MC68K #1, this pin inputs the R/W# signal. • For MC68K #2, this pin inputs the R/W# signal. • For Generic #1, this pin inputs the read command for the upper data byte (RD1#). • For Generic #2, this pin must be tied to IO V_{DD}. See “Host Bus Interface Pin Mapping” on page 14 for summary.

Pin Names	Type	Pin #	Cell	RESET# State	Description
RD#	I	76	CS	Input	This pin has multiple functions. • For SH-3/SH-4 mode, this pin inputs the read signal (RD#). • For MC68K #1, this pin must be tied to IO V_{DD}. • For MC68K #2, this pin inputs the bus size bit 1 (SIZ1). • For Generic #1, this pin inputs the read command for the lower data byte (RD0#). • For Generic #2, this pin inputs the read command (RD#). See “Host Bus Interface Pin Mapping” on page 14 for summary.
WAIT#	O	2	TS2	Hi-Z	This pin has multiple functions. • For SH-3 mode, this pin outputs the wait request signal (WAIT#). • For SH-4 mode, this pin outputs the device ready signal (RDY#). • For MC68K #1, this pin outputs the data transfer acknowledge signal (DTACK#). • For MC68K #2, this pin outputs the data transfer and size acknowledge bit 1 (DSACK1#). • For Generic #1, this pin outputs the wait signal (WAIT#). • For Generic #2, this pin outputs the wait signal (WAIT#). See “Host Bus Interface Pin Mapping” on page 14 for summary.
RESET#	I	73	CS	0	Active low input to set all internal registers to the default state and to force all signals to their inactive states.

LCD Interface

Pin Name	Type	Pin #	Cell	RESET# State	Description
FPDAT[7:0]	O	30, 31, 32, 33, 34, 35, 36, 37	CN3	0	Panel Data
FPDAT[10:8]	O, IO	24, 25, 26	CN3	Input	These pins have multiple functions. • Panel Data bits [10:8] for TFT/D-TFD panels. • General Purpose Input/Output pins GPIO[3:1]. These pins should be connected to IO V_{DD} when unused. See “LCD Interface Pin Mapping” on page 15 for summary.
FPDAT11	O, IO	23	CN3	Input	This pin has multiple functions. • Panel Data bit 11 for TFT/D-TFD panels. • General Purpose Input/Output pin GPIO4. • Inverse Video select pin. This pin should be connected to IO V_{DD} when unused. See “LCD Interface Pin Mapping” on page 15 for summary.
FPFRAME	O	39	CN3	0	Frame Pulse

Pin Name	Type	Pin #	Cell	RESET# State	Description
FPLINE	O	38	CN3	0	Line Pulse
FPSHIFT	O	28	CN3	0	Shift Clock
LCDPWR	O	43	CO1	0	Active high LCD Power Control
DRDY	O	42	CN3	0	This pin has multiple functions. • TFT/D-TFD Display Enable (DRDY). • LCD Backplane Bias (MOD). • Second Shift Clock (FPSHIFT2). See “LCD Interface Pin Mapping” on page 15 for summary.

Clock Input

Pin Name	Type	Pin #	Driver	Description
CLKI	I	51	C	Input Clock

Miscellaneous

Pin Name	Type	Pin #	Cell	RESET# State	Description
CNF[3:0]	I	46, 47, 48, 49	C	As set by hardware	These inputs are used to configure the SED1375 - see “Summary of Configuration Options” on page 14. Must be connected directly to IO V_{DD} or V_{SS}.
GPIO0	IO, I	22	CS/ TS1	Input	This pin has multiple functions. • General Purpose Input/Output pin. • Hardware Power Save.
TESTEN	I	44	CD	Hi-Z	Test Enable input. This input must be connected to V_{SS}.

Power Supply

Pin Name	Type	Pin #	Driver	Description
COREVDD	P	1, 21, 41, 61	P	Core V_{DD}
IOVDD	P	10, 29, 52	P	IO V_{DD}
VSS	P	20, 27, 40, 50, 60, 72, 80	P	Common V_{SS}

Summary of Configuration Options

Configuration Pin	Power On/Reset State	
	1	0
CNF3	Big Endian	Little Endian
CNF[2:0]	Select host bus interface as follows:	

CNF2	CNF1	CNF0	BS#	Host Bus
0	0	0	X	SH-4 interface
0	0	1	X	SH-3 interface
0	1	0	X	reserved
0	1	1	X	MC68K #1, 16-bit
1	0	0	X	reserved
1	0	1	X	MC68K #2, 16-bit
1	1	0	0	reserved
1	1	0	1	reserved
1	1	1	0	Generic #1, 16-bit
1	1	1	1	Generic #2, 16-bit

Host Bus Interface Pin Mapping

SED1375 Pin Names	SH-3	SH-4	MC68K #1	MC68K #2	Generic #1	Generic #2
AB[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]	A[16:1]
AB0	A0	A0	LDS#	A0	A0	A0
DB[15:0]	D[15:0]	D[15:0]	D[15:0]	D[31:16]	D[15:0]	D[15:0]
WE1#	WE1#	WE1#	UDS#	DS#	WE1#	BHE#
CS#	CSn#	CSn#	External Decode	External Decode	External Decode	External Decode
BCLK	CKIO	CKIO	CLK	CLK	BCLK	BCLK
BS#	BS#	BS#	AS#	AS#	connect to V_{SS}	connect to IO V_{DD}
RD/WR#	RD/WR#	RD/WR#	R/W#	R/W#	RD1#	connect to IO V_{DD}
RD#	RD#	RD#	connect to IO V_{DD}	SIZ1	RD0#	RD#
WE0#	WE0#	WE0#	connect to IO V_{DD}	SIZ0	WE0#	WE#
WAIT#	WAIT#	RDY#	DTACK#	DSACK1#	WAIT#	WAIT#
RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#

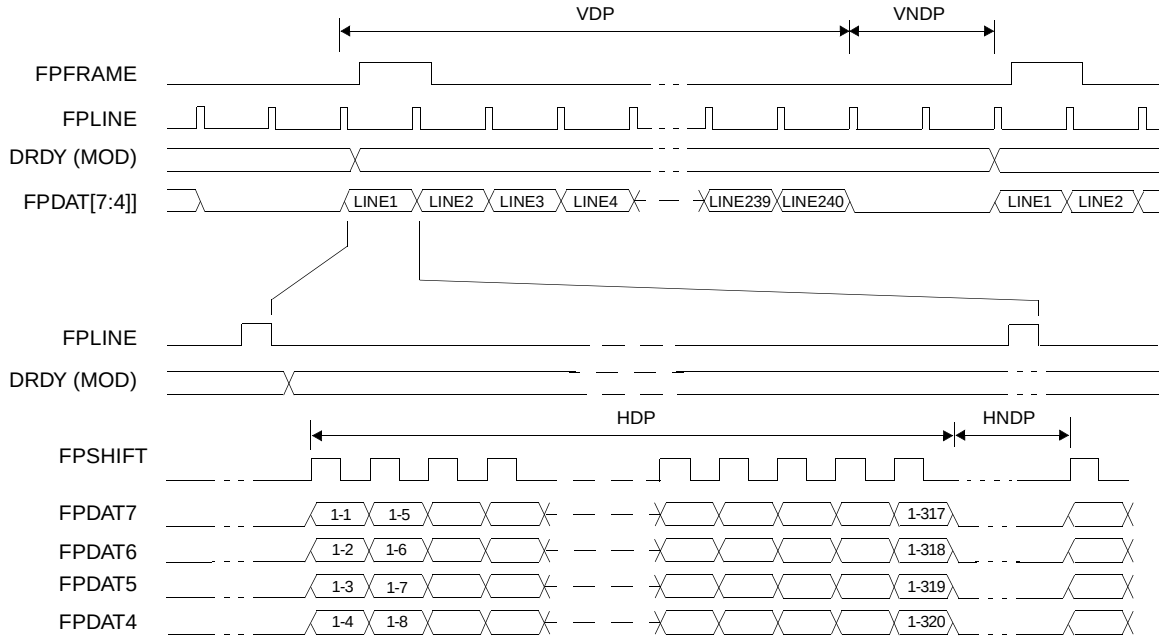
LCD Interface Pin Mapping

SED1375 Pin Name	Monochrome Passive Panel			Color Passive Panel				Color TFT/D-TFD	
	4-bit Single	8-bit Single	8-bit Dual	4-bit Single	8-bit Single Format 1	8-bit Single Format 2	8-bit Dual	9-bit	12-bit
FPFRAME	FPFRAME								
FPLINE	FPLINE								
FPSHIFT	FPSHIFT								
DRDY	MOD	MOD	MOD	MOD	FPSHIFT2	MOD	MOD	DRDY	
FPDAT0	driven 0	D0	LD0	driven 0	D0	D0	LD0	R2	R3
FPDAT1	driven 0	D1	LD1	driven 0	D1	D1	LD1	R1	R2
FPDAT2	driven 0	D2	LD2	driven 0	D2	D2	LD2	R0	R1
FPDAT3	driven 0	D3	LD3	driven 0	D3	D3	LD3	G2	G3
FPDAT4	D0	D4	UD0	D0	D4	D4	UD0	G1	G2
FPDAT5	D1	D5	UD1	D1	D5	D5	UD1	G0	G1
FPDAT6	D2	D6	UD2	D2	D6	D6	UD2	B2	B3
FPDAT7	D3	D7	UD3	D3	D7	D7	UD3	B1	B2
FPDAT8	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	GPIO1	B0	B1
FPDAT9	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	R0
FPDAT10	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	GPIO3	G0
FPDAT11	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4/ Hardware Video Invert	GPIO4	B0

Note

1. Unused GPIO pins must be connected to IO V_{DD}.

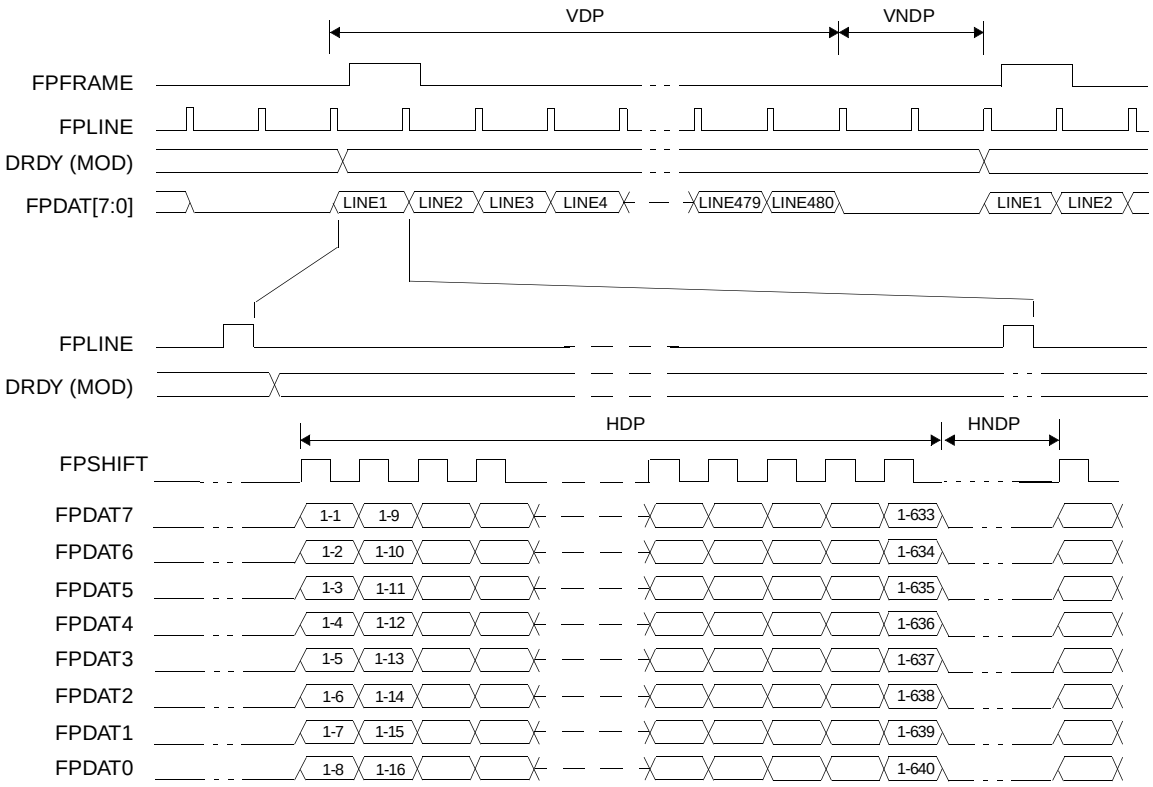
■ 4-BIT SINGLE MONOCHROME PASSIVE LCD PANEL INTERFACE



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 320x240 panel
For this timing diagram Mask FPSHIFT, REG[01h] bit 3, is set to 1

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

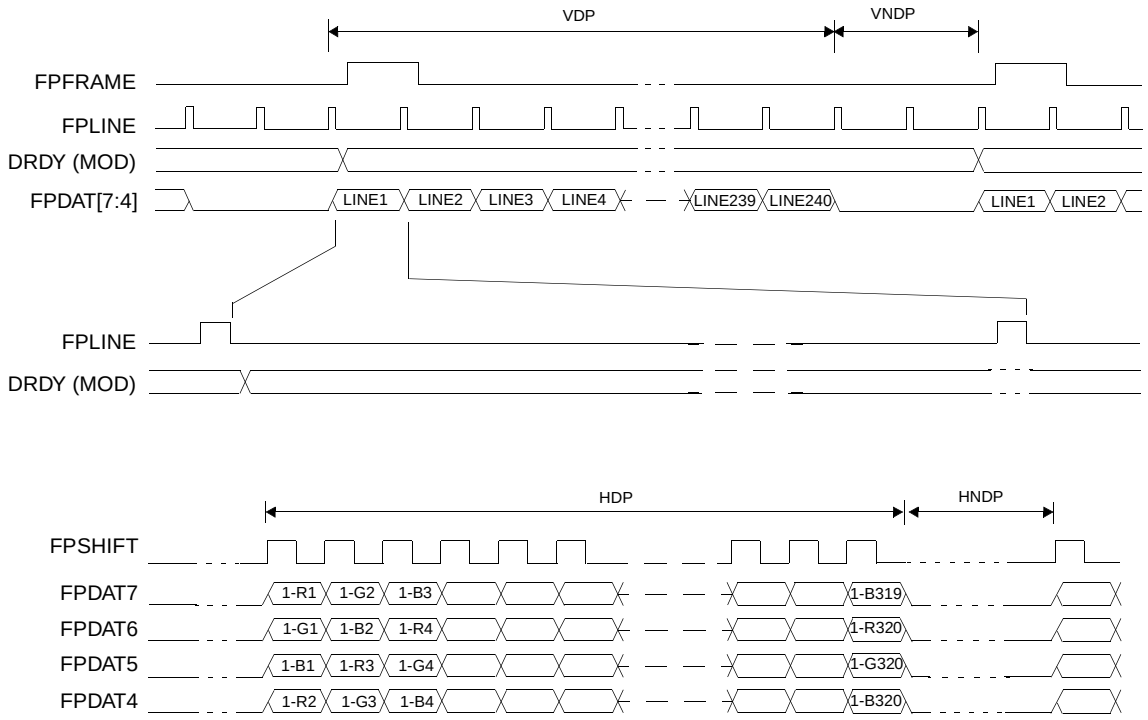
■ 8-BIT SINGLE MONOCHROME PASSIVE LCD PANEL INTERFACE



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640x480 panel
For this timing diagram Mask FPSHIFT, REG[01h] bit 3, is set to 1

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

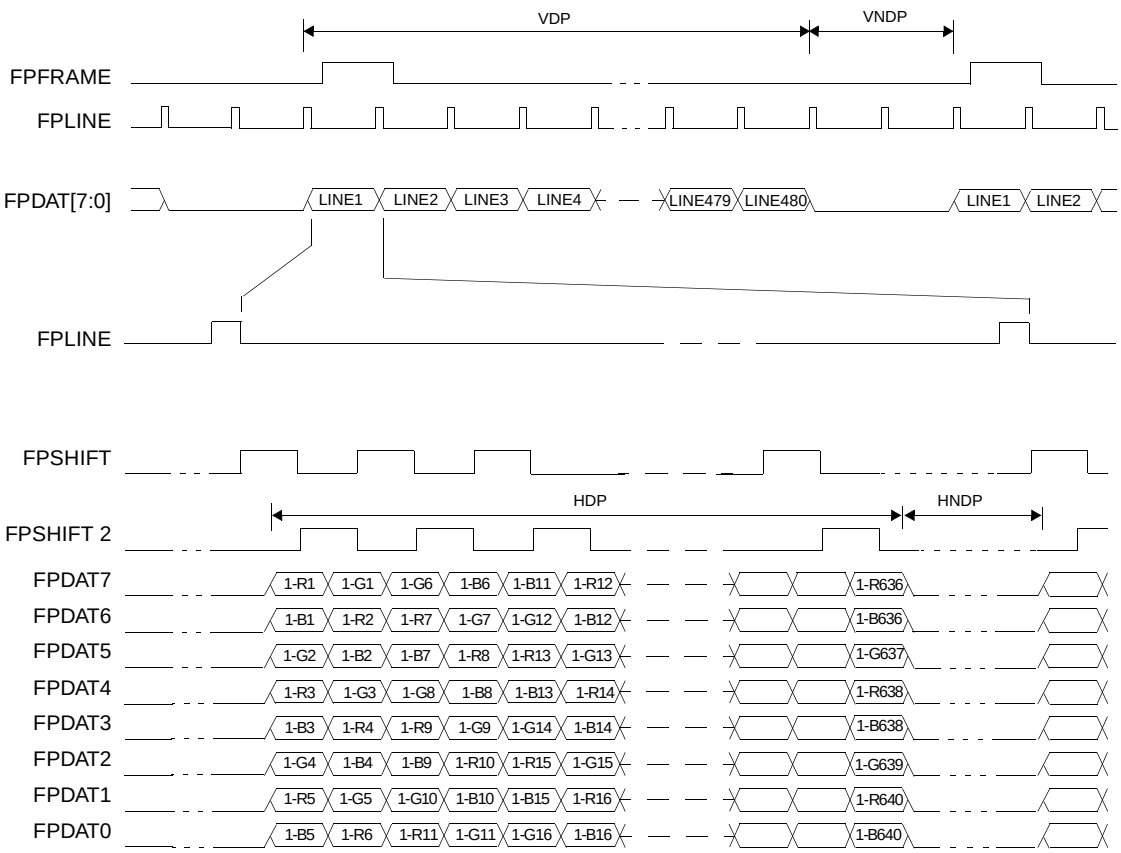
■ 4-BIT SINGLE COLOR LCD PANEL INTERFACE



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 320x240 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

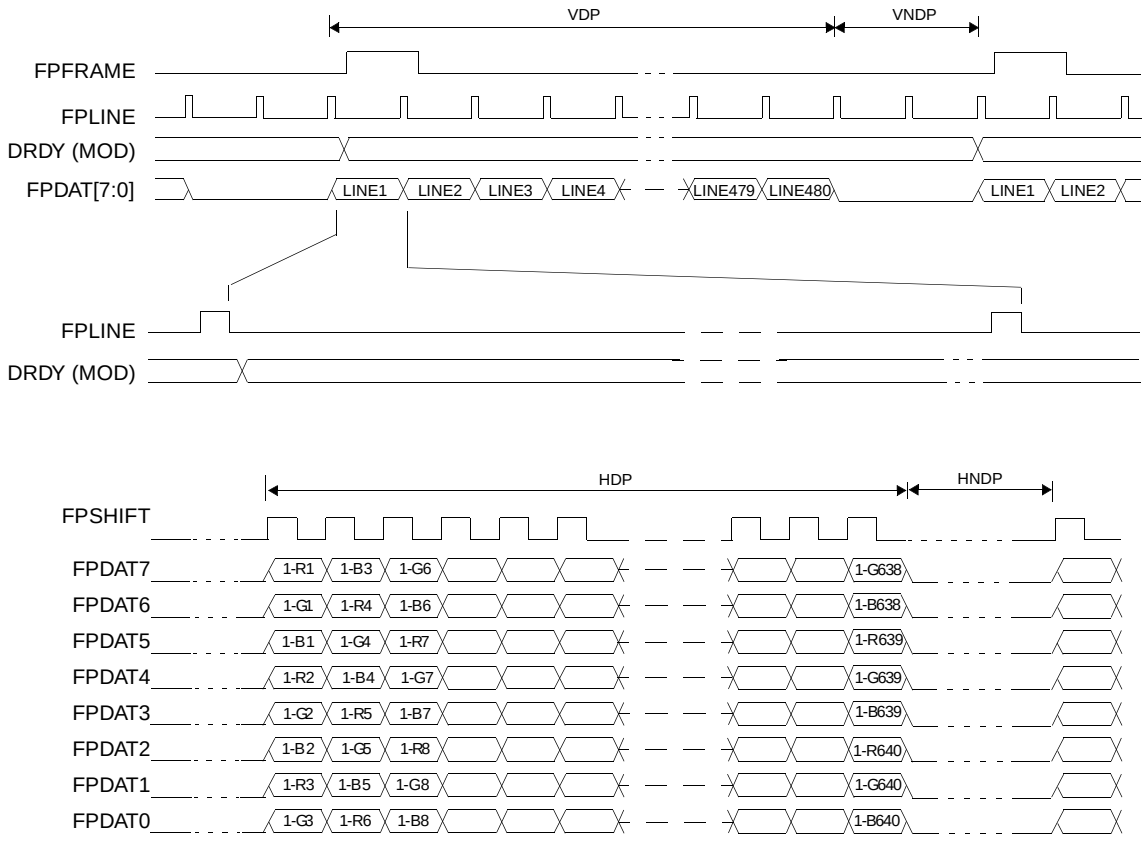
■ 8-BIT SINGLE COLOR PASSIVE LCD PANEL INTERFACE (FORMAT 1)



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

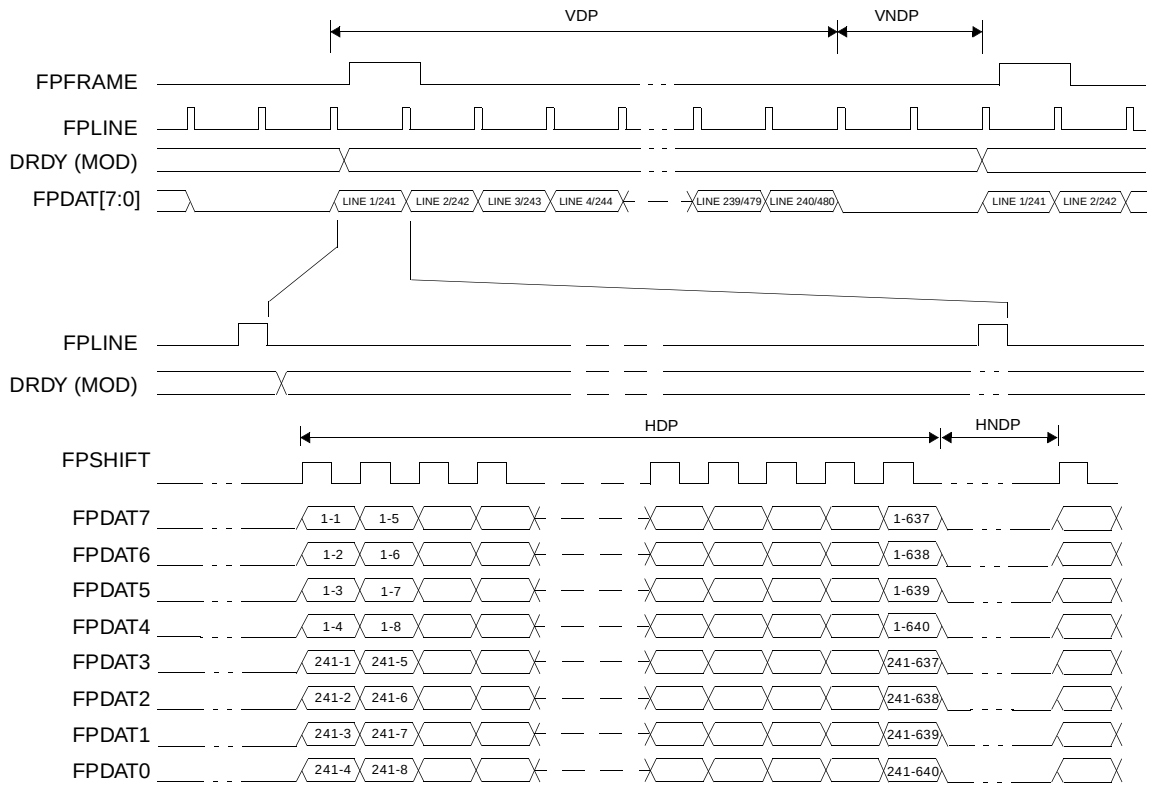
■ 8-BIT SINGLE COLOR PASSIVE LCD PANEL INTERFACE (FORMAT 2)



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

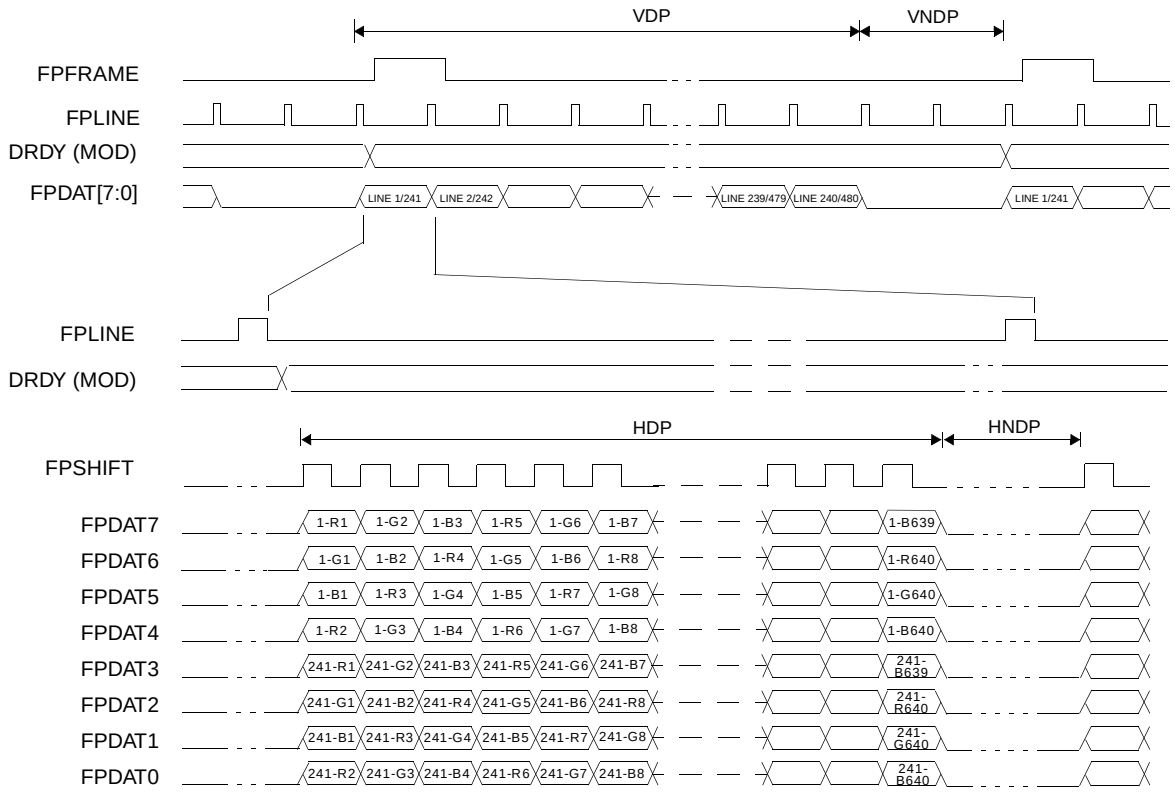
■ 8-BIT DUAL MONOCHROME PASSIVE LCD PANEL INTERFACE



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

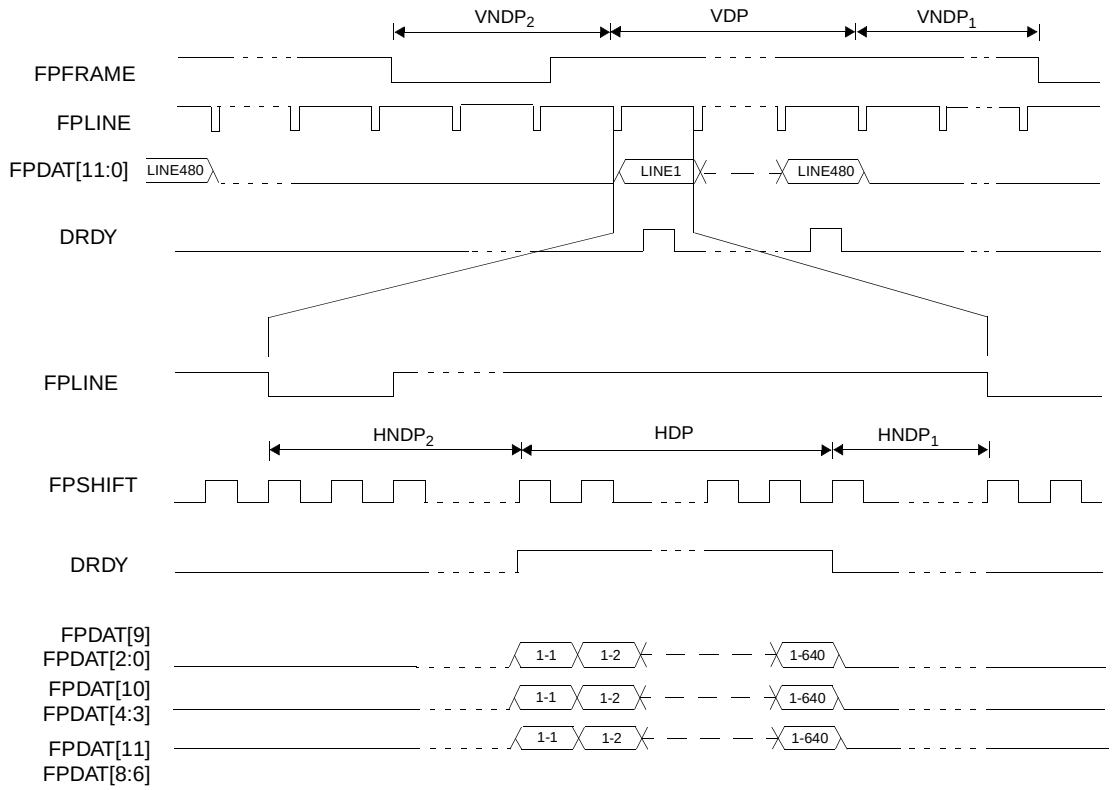
■ 8-BIT DUAL COLOR PASSIVE LCD PANEL INTERFACE



* Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period

■ 9/12-BIT ACTIVE TFT/D-TFD LCD PANEL INTERFACE

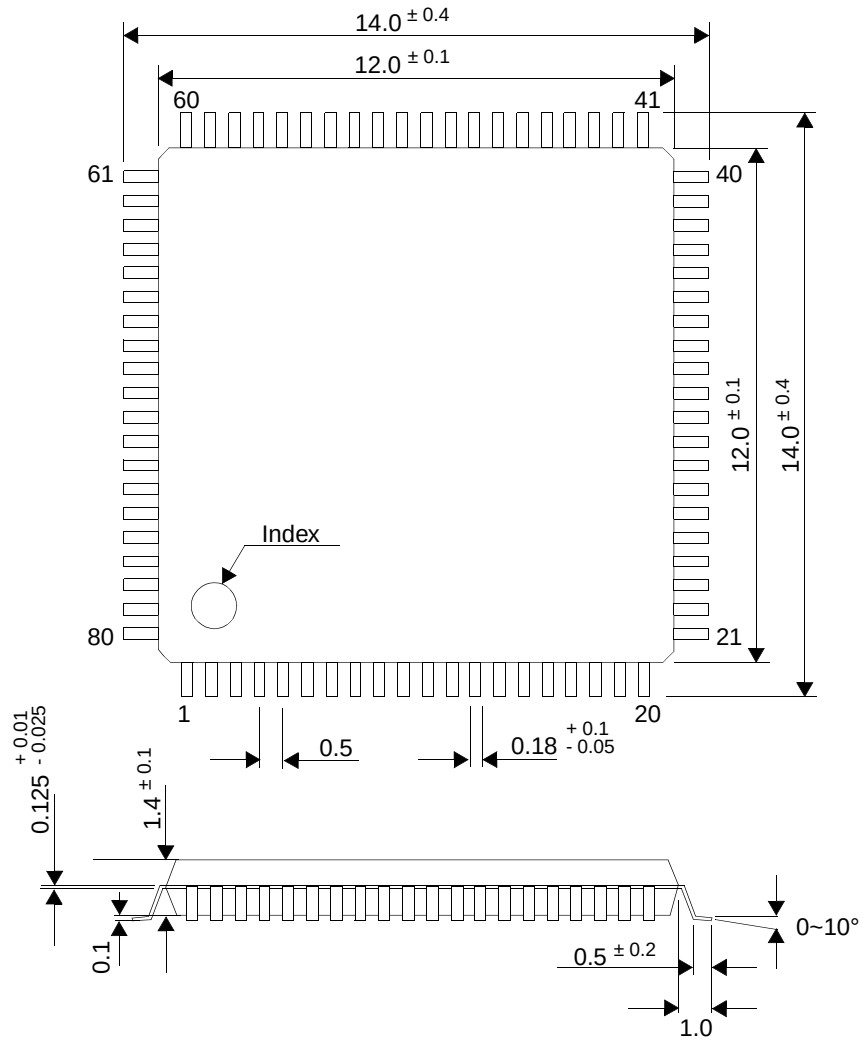


Note: DRDY is used to indicate the first pixel
Example Timing for 12-bit 640x480 panel

VDP = Vertical Display Period
VNDP = Vertical Non-Display Period = VNDP1 + VNDP2
VNDP1 = Vertical Non-Display Period 1
VNDP2 = Vertical Non-Display Period 2
HDP = Horizontal Display Period
HNDP = Horizontal Non-Display Period = HNDP1 + HNDP2
HNDP1= Horizontal Non-Display Period 1
HNDP2= Horizontal Non-Display Period 2

■ PACKAGE DIMENSIONS

QFP14 - 80 pin **Unit: mm**



■ COMPREHENSIVE SUPPORT TOOLS

Seiko Epson Corp. provides the designer and manufacturer a complete set of resources and tools for the development of LCD Graphics Systems.

Documentation

- Technical Manuals
- Evaluation/Demonstration Board Manuals

Evaluation/Demonstration Board

- Assembled and Fully Tested Graphics Evaluation/Demonstration Boards
- Schematic of Evaluation/Demonstration Boards
- Parts List
- Installation Guide
- CPU Independent Software Utilities
- Evaluation Software
- Windows CE Display Driver

■ Application Engineering Support

Seiko Epson Corp. offers the following services through their Sales and Marketing Network:

- Sales Technical Support
- Customer Training
- Design Assistance

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- SED1375 Technical Manual
- SDU1375 Evaluation Boards
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