EPSON®

## S5U13502 Dot Matrix Graphics LCD Controller

# ISA Bus Interface Considerations

**Document Number: X16-AN-003-06**

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# 1 INTRODUCTION

The S1D13502 is a general purpose LCD controller capable of interfacing to a variety of microprocessors. This interface is accomplished through the use of minimal external circuitry. This application note describes the interface between the S1D13502 and the ISA Bus.

## 1.1 Reference Material

Refer to the S1D13502 Hardware Functional Specification (X16-SP-001-xx) for complete AC timing details.

This document makes no attempts to describe the operation of the ISA Bus, please refer to the appropriate ISA Bus documentation for complete information.

# 2 16-BIT ISA BUS INTERFACE

For the purpose of the example shown below, the following conditions are set by default:

1. Indexing I/O with addresses 0310h and 0311h (see Configuration Options)
2. 128Kbytes of display memory occupying $C and $D segments (see Configuration Options)

**Note**
This memory configuration will conflict with a VGA card installed on the same bus, therefore either a serial terminal or monochrome display adapter is recommended as the primary console.

This section provides the necessary equations and settings to complete the interface between the S1D13502 and the 16-bit ISA Bus.

**Note**
A PAL was used instead of discrete logic to reduce external component count.

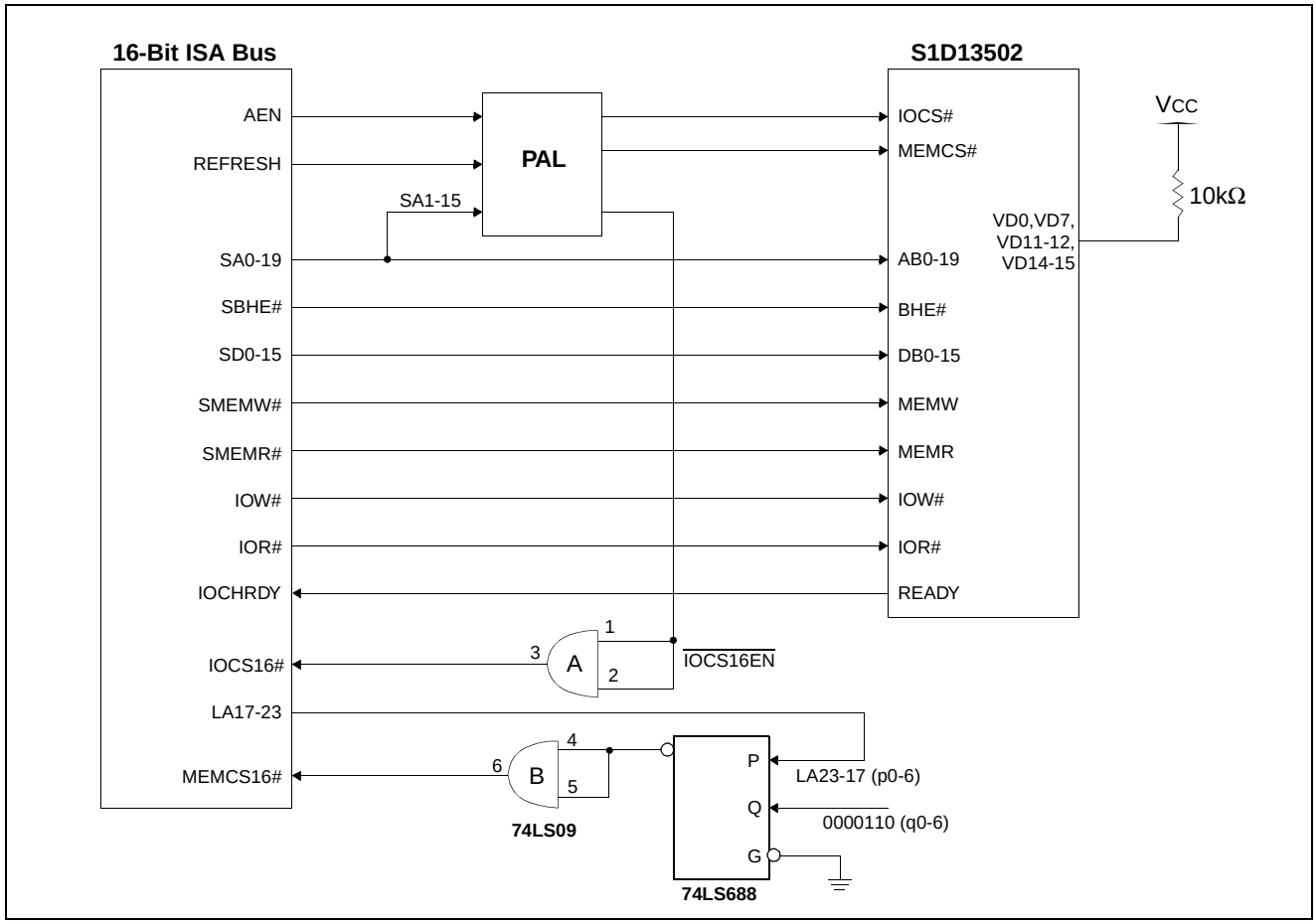


*Figure 8: 16-Bit ISA Bus Implementation*

## 1.2 PAL Equations

The PAL is programmed with the following equations:

1. As stated above, the default I/O address is from 0310h to 0311h. The S1D13502 provides internal decoding of address bits A0 to A9, therefore minimal external circuitry is necessary to provide signals IOCS# and IOCS16#

   IOCS# is required by the S1D13502 to indicate a valid IO cycle. In an ISA bus environment, valid IO decoding must include addresses A15-A0. Given this example, addresses A10-15 must all be '0' and AEN must also be '0'.
   IOCS# = !(!AEN & !A15 & !A14 & !A13 & !A12 & !A11 & !A10)

2. As the S1D13502 is capable of 16-bit IO access, the IOCS16# bus signal must be driven externally to indicate such a cycle. As stated in the ISA specification, the IOCS16# is a straight address decode without qualification.

   IOCS16EN# = !(!IOCS# & A9 & A8 & !A7 & !A6 & !A5 & A4 & !A3 & !A2 & !A1)

3. With 128Kbytes of display memory and A17 to A19 decoded internally to S1D13502;
   MEMCS# = !REFRESH

## 1.3 Additional Discrete Logic Description

1. As shown in Figure 1, the 74LS688 is configured as a memory decoder with valid addresses between 0Cxxxxh and 0Dxxxxh.
2. The 74LS09 is used simply to provide the Open-Collector outputs necessary for the IOCS16# and MEMCS16# signals.

## 1.4 S1D13502 Default Setup

### 1.4.1 Configuration Options

| | | |
|---|---|---|
| 1. | VD15 - VD13 = 110 | memory decoding for locations $C and $D segments |
| 2. | VD12 - VD4 = 110001000 | I/O decoding for locations 1100010000b - 1100010001b |
| 3. | VD3 = 0 | no byte swap of high and low bytes |
| 4. | VD2 = 0 | ISA Bus interface, i.e. non- MC68K interface |
| 5. | VD1 = 0 | indexing I/O |
| 6. | VD0 = 1 | 16-bit bus interface |

Where 1 = pull-up with a 10K resistor; 0 = no pull-up resistor

**Note**
The states of these data pins are internally latched during RESET.

### 1.4.2 Register Setting

AUX[1] bit 1 = 0 for 16-bit memory interface (must be 16-bit with a 16-bit bus).

# 3 8-BIT ISA BUS INTERFACE

For the purpose of the example shown below, the following conditions are set by default:

1. Indexing I/O with partial decoding, i.e. address lines A10 to A15 are not decoded for I/O cycles

**Note**
Partial decoding is quite safe on most ISA Bus systems as I/O addresses above 03FFh are rarely used.

2. I/O addresses are xxxxxx1100000000b and xxxxxx1100000001b
3. 64Kbytes of display memory occupying $A segment

**Note**
The 74LS00 is simply used to detect the $B segment and invalidate the MEMCS# input.

**Note**
This memory configuration will conflict with a VGA card installed on the same bus, therefore either a serial terminal or monochrome display adapter is recommended as the primary console.

This section provides the necessary settings to complete the interface between the S1D13502 and the 8-bit ISA Bus. Since I/O addresses are partially decoded, there is no need to use a PAL for decoding.

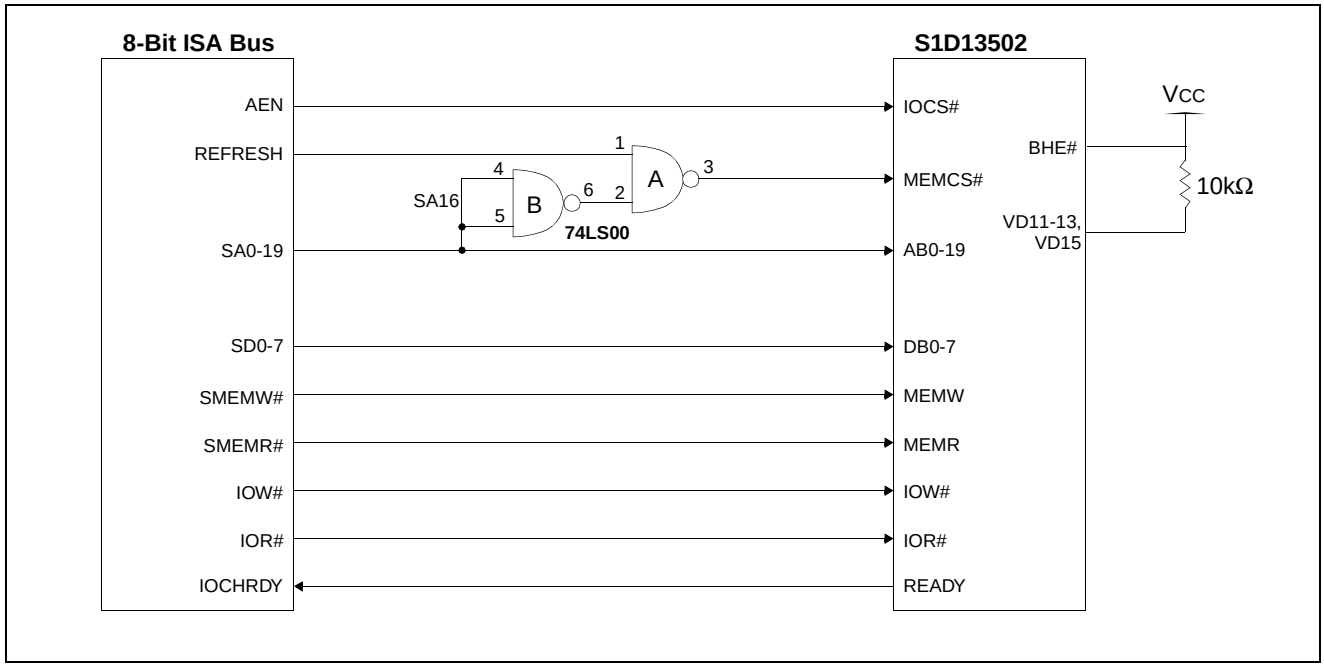


*Figure 9: 8-Bit ISA Bus Implementation*

## 1.5 S1D13502 Default Setup

### 1.5.1 Configuration Options

1. VD15 - VD13 = 101 memory decoding for locations $A segment
2. VD12 - VD4 = 110000000 I/O decoding for locations 1100000000b - 1100000001b
3. VD3 = 0 No byte swap of high and low bytes
4. VD2 = 0 ISA Bus interface, i.e. non- MC68K interface
5. VD1 = 0 Indexing I/O
6. VD0 = 0 8-bit bus interface

Where 1 = pull-up with a 10K resistor; 0 = no pull-up resistor

**Note**
The states of these data pins are internally latched during RESET.

### 1.5.2 Register Setting

AUX[1] bit 1 = 0 for 16-bit memory interface or

AUX[1] bit 1 = 1 for 8-bit memory interface.

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