EPSON

SED1672

Dot Matrix High Duty LCD Driver

- 68 Output
- 1/64 to 1/300 in display duty
- CMOS High Voltage Resistant Process

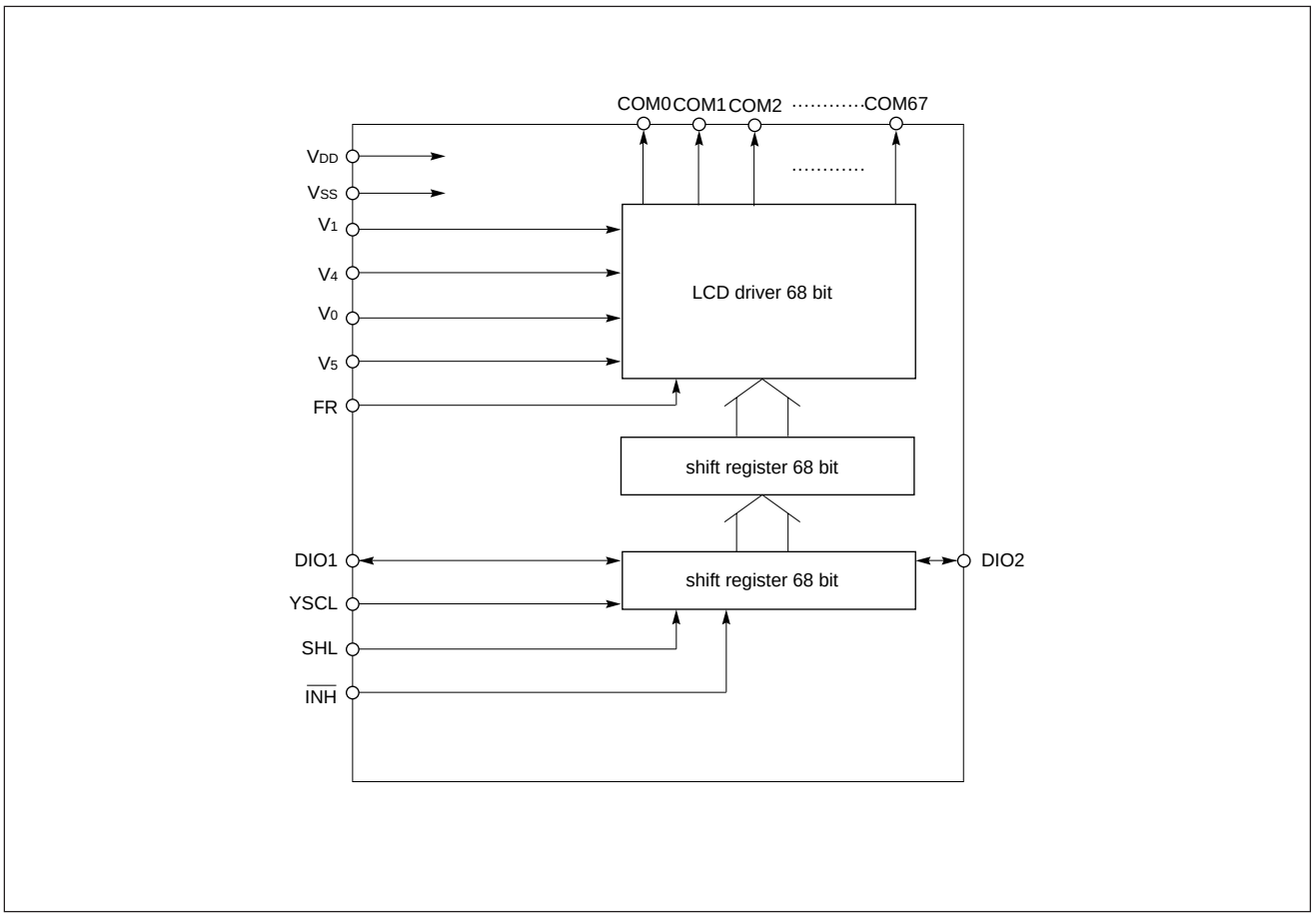
■ OVERVIEW

The SED1672 is a 68 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels up to a duty ratio of 1/300. It is intended to be used in conjunction with the SED1606 as a pair.
Since the SED1672 is so designed to drive LCD's over a wide range of voltages, and also the maximum potential V_0 of its LCD drive bias voltages is isolated from V_{DD} to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.
The SED1672 is featured in its simple pad layout which is easy in mounting PC boards in addition to its selectable bidirectional driver output sequence. It also has 68 LCD output segments of high pressure resistance and low output impedance.

■ FEATURES

- Number of LCD drive output segments: 68
- Common output ON resistance: 700Ω (Typ.)
- Display duty ratio: 1/64 to 1/300 (Reference)
- Display capacity: Possible to display 640 x 480 dots when used in combination with SED1606.
- Selectable pin output shift direction
- Instantaneous display blanking enabled by inhibit function
- Adjustable offset bias of LCD power to V_{DD} level
- Wide range of LCD drive voltages: –7 V to –28 V (Absolute maximum rated voltage: –30 V)
- Logic system power supply: –2.7 V to –5.5 V
- Chip packaging
  SED1672D$_{0A}$ (AL-pad die form)
  SED1672F$_{0A}$ (80-pin FP)
- No radial rays countermeasure taken in designing

■ BLOCK DIAGRAM



• ABSOLUTE MAXIMUM RATINGS

(V_{DD}=0V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_1, V_4	V_5–0.3 to +0.3	V
Input voltageV_I	V_{SS}–0.3	to+0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OCOM}	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature	Tstg	–65 to +150	°C
Soldering temperature and time	Tsol	260°C · 10sec	–

Notes: 1. The voltage of V_0, V_1 and V_4 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$.
2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = Å|2.6 V or more can cause permanent damage to the LSI. Functional operation under these conditions is not implied. Care should be taken to the power supply sequence especially in the system power ON or OFF.

• ELECTRICAL CHARACTERISTICS

● DC characteristics

(Unless otherwise specified, $V_{DD} = V_0 = 0V$, $V_{SS} = -5.0V \pm 10\%$, Ta = –40 to 85°C.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	–	–28.0	–	–7.0	V	V_5
Operation enable voltage	V_5	Functional operation	–	–	–7.0	V	V_5
Supply voltage (2)	V_0	Recommended value	–2.5	–	0	V	V_0
Supply voltage (3)	V_1	Recommended value	2/9·V_5	–	V_{DD}	V	V_1
Supply voltage (4)	V_4	Recommended value	V_5	–	7/9·V_5	V	V_4
"H" input voltage (1)	V_{IH}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	DIO1, DIO2,
"L" input voltage (1)	V_{IL}		V_{SS}	–	0.8V_{SS}	V	YSCL, SHL, FR
"H" input voltage (2)	V_{IHT}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	$\overline{INH}$
"L" input voltage (2)	V_{ILT}		V_{SS}	–	0.85V_{SS}	V	
"H" output voltage	V_{OH}	I_{OH}=–0.3mA I_{OH}=–0.2mA (V_{SS}=–2.7 to –4.5V)	–0.4	–	0	V	DIO1, DIO2
"L" output voltage	V_{OL}	I_{OL}=+0.3mA I_{OL}=+0.2mA (V_{SS}=–2.7 to –4.5V)	V_{SS}	–	V_{SS}+0.4	V	
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	–	–	2.0	µA	YSCL, SHL, $\overline{INH}$, FR
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$	–	–	5.0	µA	DIO1, DIO2
Static current	I_{DDS}	V_5=–7.0 to –28.0V $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	–	–	25	µA	V_{DD}
Output resistance	R_{COM}	ΔVON=0.5V, V_5=–20.0V: When the V_1, V_4, V_0 or V_5 level is output	–	0.70	1.40	KΩ	COM0 to COM99
Average operating current consumption (1)	I_{SS1}	V_{SS}=–5.0V, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$, f_{YSCL}=12KHz, Frame frequency=60Hz, Input data; "H" at no load every 1/200 duy	–	7	15	µA	V_{SS}
		Other conditions are the same as VSS = –3.0 V	–	5	10		
Average operating current consumption (2)	I_{SS2}	V_{SS}=–5.0V, V_1=–2.0V, V_4=–18.0V, V_5=–20.0V Other conditions are the same as in the item of I_{SS1}.	–	7	15	µA	V_5
Input pin capacitance	C_I	Ta=25°C	–	–	8	pF	YSCL, SHL, $\overline{INH}$, FR
Input/output pin capacitance	CI/O		–	–	15	pF	DIO1, DIO2

• DIFFERENT POINTS FROM REPLACEMENT PRODUCT

	SED1672*0*	SED1630***
Function	Bidirectional shift register $\overline{INH}$ 68 output segments	Bidirectional shift register $\overline{INH}$ 68 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	–
PAD coordinates	Different from the equivalent product	–

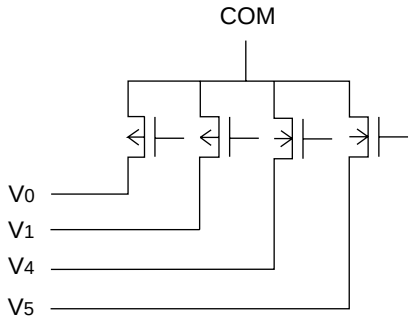
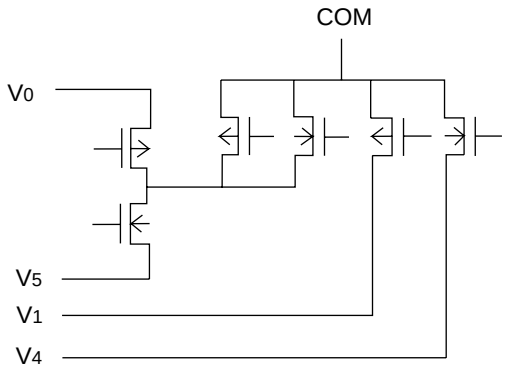


Fig. 1



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SEIKO EPSON CORPORATION
ELECTRONIC DEVICE MARKETING DEPARTMENT

IC Marketing & Engineering Group
421-8 Hino, Hino-shi, Tokyo 191, JAPAN
Phone: 0425-87-5816 FAX: 0425-87-5624

International Marketing Department I (Europe, U.S.A.)
421-8 Hino, Hino-shi, Tokyo 191, JAPAN
Phone: 0425-87-5812 FAX: 0425-87-5564

International Marketing Department II (Asia)
421-8 Hino, Hino-shi, Tokyo 191, JAPAN
Phone: 0425-87-5814 FAX: 0425-87-5110

Issue Nov. 1996, printed in Japan Ⓗ