

SED1794D0B

TFT LCD Driver

■ DESCRIPTION

The gate driver LSI SED1794 is designed to drive an active matrix LCD panel.

It enables high-voltage operation, positive and negative output voltages and is compatible with various TFT-LCD panel driving methods.

By switching the number of outputs between 200 and 192, it is compatible with the XGA/SXGA panel (192 outputs) and the SVGA panel (200 outputs)

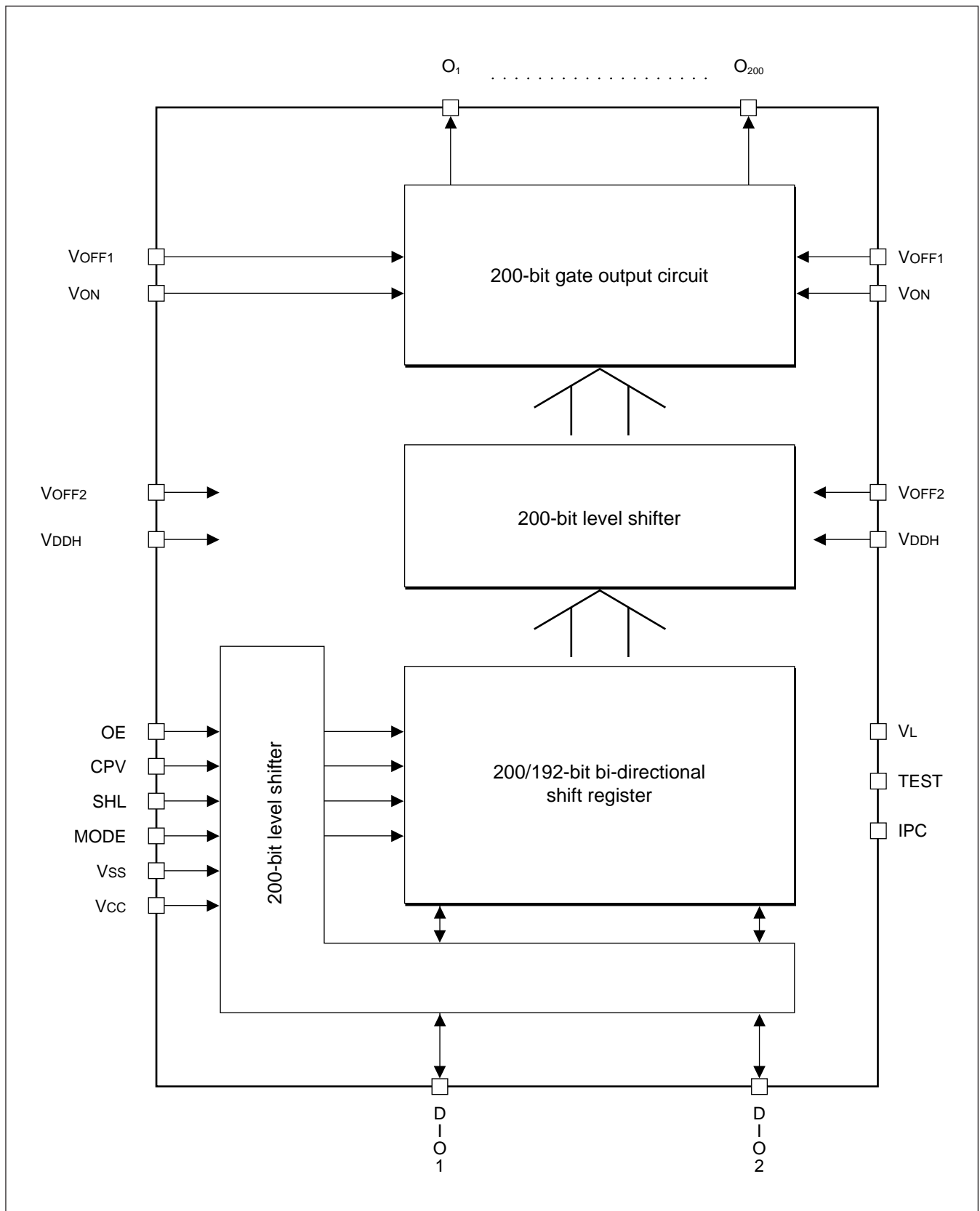
Thanks to its slim TCP shape, it enables a small-architected LCD module to be realized.

■ FEATURES

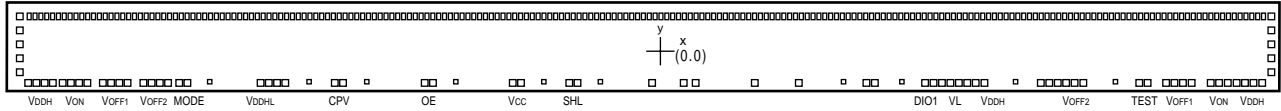
- Number of gate driving outputs: 200/192
- Super slim chip: Slim TCP
- Low voltage operation available: 2.7 V (min.)
- Output switching function available (200/192 outputs)
- Gate output voltage $V_{ON} - V_{OFF1}$ amplitude: 40 V (max.)
- Output shift direction-pin selection.
- Output enable function
- Package to be shipped
 - Au bump chip: SED1794D0B
 - TCP: SED1794T**
- This LSI is not designed to resist radiation or light.

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■ BLOCK DIAGRAM



■ PAD LAYOUT



Chip size: 16.00 mm × 1.08 mm
 Pad pitch: Output pin = 79 μm (min.) *1
 Same input pin = 99 μm (min.) *2
 Between input pins = 119 μm (min.) *2
 Chip thickness: 625 μm (typical)

Au bump specifications: SED1794D0B (reference)

(X direction) (Y direction)

Bump size A:	50.4 μm × 80.0 μm	*1
Bump size B:	77.6 μm × 78.4 μm	*2
Bump size C:	49.6 μm × 56.0 μm	*3
Bump size D:	50.4 μm × 60.0 μm	*4
Bump size E:	58.4 μm × 59.2 μm	*5

Notes

1. Pad # 81 to 280.
2. Pad # 1 to 18, 20 to 23, 25, 26, 28, 29, 31, 32, 34, 35, 37 to 41, 43, 44, 46 to 53, 55 to 60 and 62 to 75.
3. Pad # 76 to 79 and 282 to 285.
4. Pad # 80 and 281.
5. Pad # 19, 24, 27, 30, 33, 36, 42, 45, 54 and 61.

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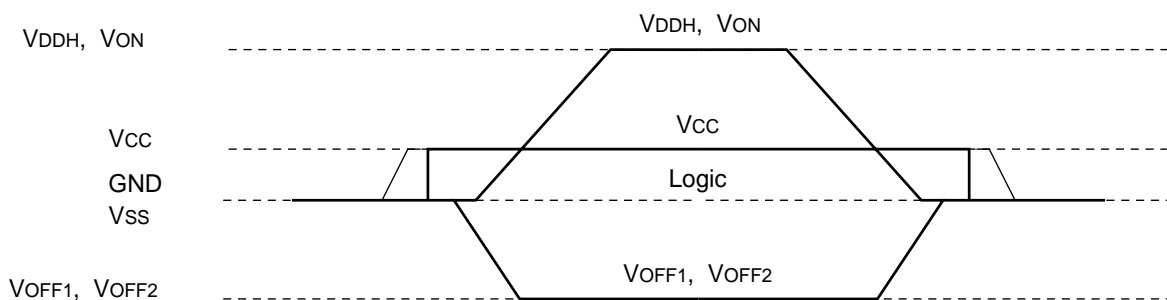
■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V _{CC}	-0.5 to +7.0	V
Supply voltage (2)	V _{DDH}	-0.5 to +45.0	V
Supply voltage (3)	V _{OH}	-0.5 to V _{DDH} +0.5	V
Supply voltage (4)	V _{OFF1} , V _{OFF2}	-23.0 to +0.5	V
Supply voltage (5)	V _{DDH} - V _{OFF2} V _{ON} - V _{OFF1}	-0.5 to +45.0	V
Input voltage	V _{IN}	-0.5 to V _{CC} +0.5	V
Input current	I _{IN}	±10	mA
Output current	I _O	±10	mA
Ambient operating temperature	T _a	-25 to +85	°C
Storing temperature	T _{stg2}	-55 to +125	°C

Notes

1. All power supplies refer to V_{SS} unless otherwise specified.
2. The LSI may permanently break if used outside the absolute maximum ratings shown above.
3. For voltages V_{CC}, V_{SS}, V_{DDH}, V_{ON}, V_{OFF1} and V_{OFF2}, be sure to keep the condition of "V_{OFF2} ≤ V_{OFF1} ≤ V_{SS} ≤ V_{CC} ≤ V_{DDH}".
4. Turn V_{CC}, V_{OFF2}/V_{OFF1} and V_{ON}/V_{DDH} on in this order and follow the opposite order when turning the power off.
5. Never float V_{CC} while a voltage of 10 V or higher is applied to V_{DDH} - V_{OFF2} and V_{ON} - V_{OFF1} or allow V_{CC} to go under 2.6 V, otherwise, an overcurrent may flow, disadvantageously affecting the LSI reliability.



■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V)

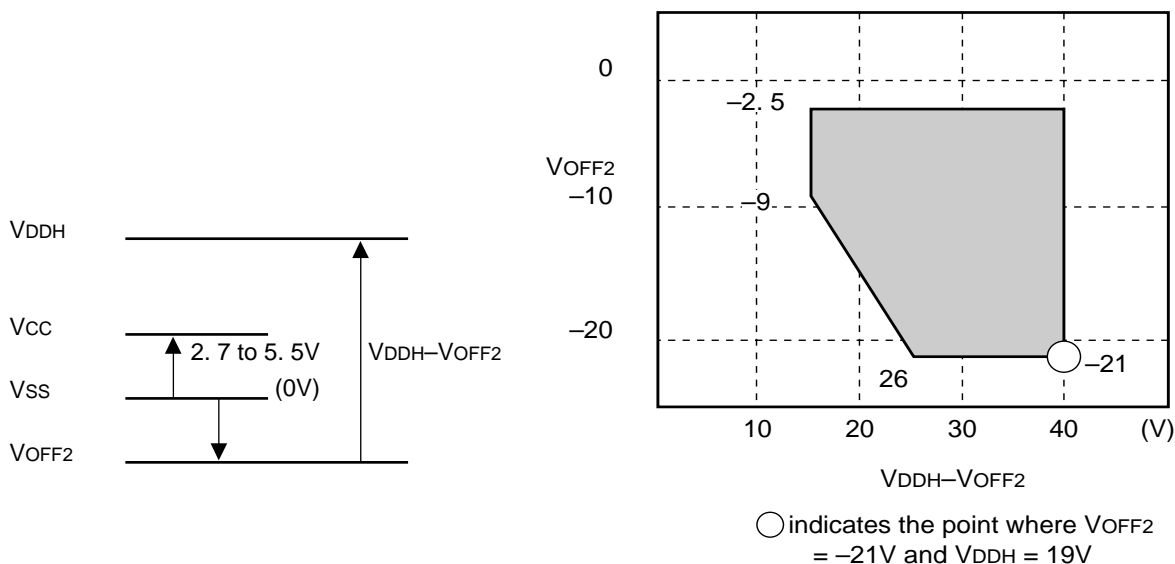
Parameter	Symbol	Rating	Unit
Supply voltage (1)	V _{CC}	2.7 to 5.5	V
Supply voltage (2)	V _{DDH}	10.0 to 40.0	V
Supply voltage (3)	V _{ON}	10.0 to 40.0	V
Supply voltage (4)	V _{OFF1} , V _{OFF2}	-21.0 to -2.5	V
Supply voltage (5)	V _{DDH} - V _{OFF2} V _{ON} - V _{OFF1}	15 to 40.0	V
Operating frequency	f _{CPV}	DC to 400	kHz

Notes

1. LSI operation is guaranteed within the recommended operating condition range.
2. Allowing for the power supply impedance in the mounted status, insert a bypass capacitor for noiseproof measures near the V_{SS}, V_{OFF1} and V_{OFF2} pins.
3. Unless swinging the V_{OFF1} supply voltage, make the electric potential the same as that of V_{OFF2}.
4. When swinging the V_{OFF1} supply voltage, keep the range within "V_{OFF2} ≤ V_{OFF1} ≤ V_{ON} - 15 V". In this case, the guaranteed output resistance and fall time ratings will differ.

- **Recommended operating voltage range**

The recommended operating voltage is based on the combination of the high-dielectric strength logic system power supply conditions and the logic system power supply conditions (the hatched portion in the figure below on the right).



■ ELECTRICAL CHARACTERISTICS

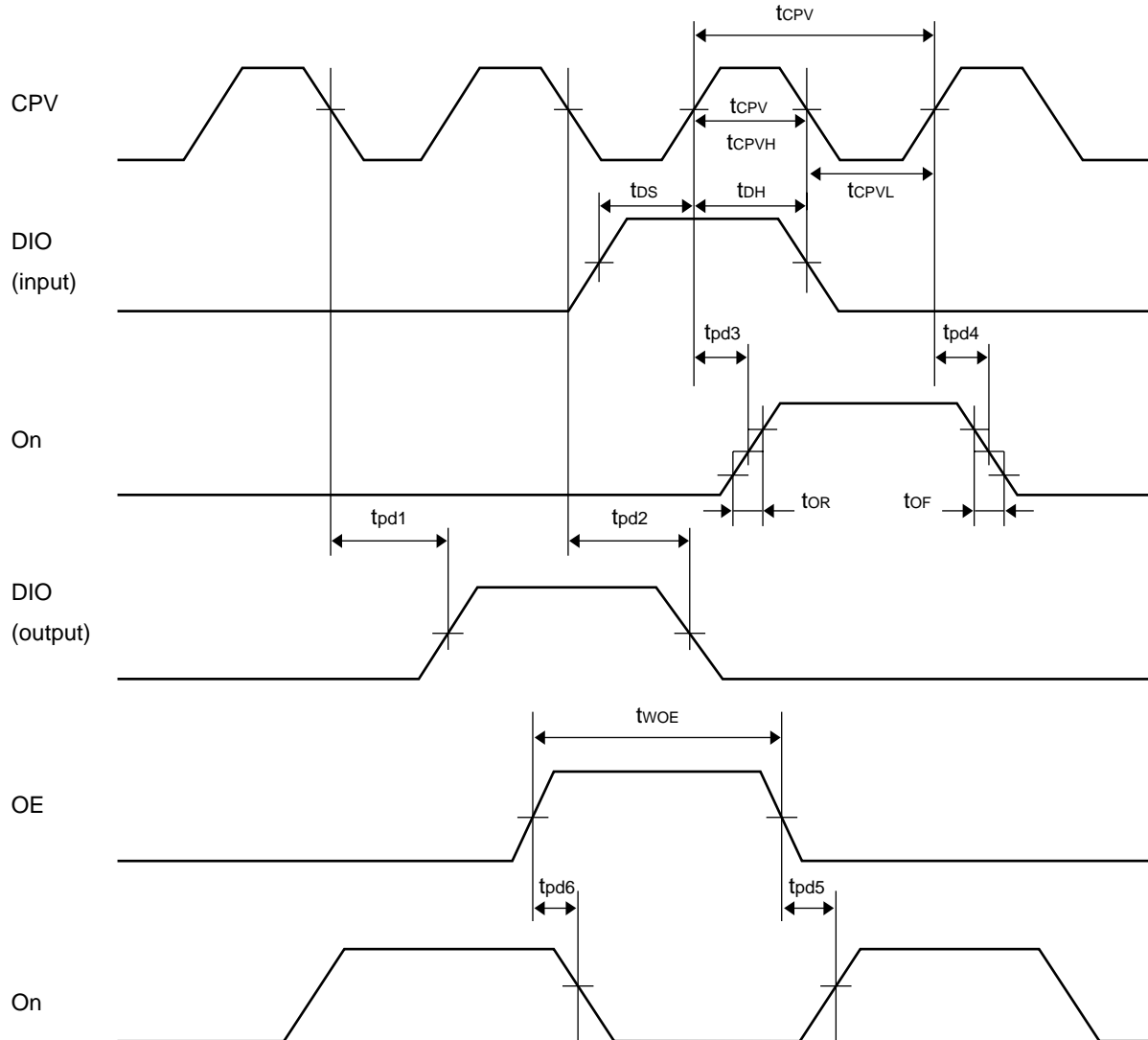
- **DC Characteristics**

Within the recommended operating voltage range when VSS = 0 V and Ta = -25 to 85°C unless otherwise specified.

Parameter	Symbol	Condition	Rating			Units	Pin used	
			Min.	Typ.	Max.			
"L" input voltage	VIL	—	VSS	—	0.3 × VCC	V	All input pins	
"H" input voltage	VIH	—	0.7 × VCC	—	VCC	V	All input pins	
"L" output voltage	VOL	IOL = 40 μA	VSS	—	VSS + 0.4		DIO1, 2	
"H" output voltage	VOH	IOH = 40 μA	VCC - 0.4	—	VCC		DIO1, 2	
Output resistance	RON	ΔVON = 1.0 V	VON - VOFF1 = 40 V	—	0.6	0.9	kΩ	O1 to O200
			VON - VOFF1 = 30 V	—	0.7	1.0		
			VON - VOFF1 = 15 V	—	0.9	1.5		
Input leakage current	ILI	—	-1.0	—	1.0	μA	All input pins	
Input capacity	CIN	Ta = 25°C	—	—	15	pF	All input pins	
Current consumption (1)	ICC	fCPV = 60 kHz	—	5	10	μA	VCC	
Current consumption (2)	IDDH		—	380	990	μA	VDDH	
Current consumption (3)	IOFF		—	-380	-990	μA	VOFF1, VOFF2	

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● AC Characteristics



Notes

The input and output signal timings refer to 50% of the signal amplitude.

On output signal t_{OR} and t_{OF} refer to 10% and 90%.

- Input Timing Characteristics**

Within the recommended operating voltage range when $V_{SS} = 0\text{ V}$ and $T_a = -25$ to 85°C unless otherwise specified.

Parameter	Symbol	Condition	Min.	Max.	Unit
CPV cycle	t_{CPV}	During cascade connection	2.5	—	μs
CPV high-level pulse width	t_{CPVH}	—	400	—	ns
CPV low-level pulse width	t_{CPVL}	—	500	—	ns
Data setup time	t_{DS}	—	100	—	ns
Data hold time	t_{DH}	—	100	—	ns
$\overline{\text{OE}}$ high-level pulse width	t_{WOE}	—	700	—	ns

The logic input rise/fall times (t_r and t_f) are specified at 30 ns or less.

- Output Timing Characteristics**

Within the recommended operating voltage range when $V_{SS} = 0\text{ V}$ and $T_a = -25$ to 85°C unless otherwise specified.

Parameter	Symbol	Condition	Min.	Max.	Unit
CPV to DIO output delay time	t_{pd1}	$CL = 20\text{ pF}$	—	600	ns
	t_{pd2}		—	600	ns
CPV to On output delay time	t_{pd3}	$CL = 220\text{ pF}$ $V_{DDH} = V_{ON} = 20\text{ V}$ $V_{OFF2} = V_{OFF1} = -20\text{ V}$	—	550	ns
	t_{pd4}		—	550	ns
$\overline{\text{OE}}$ to On output delay time	t_{pd5}	$CL = 220\text{ pF}$ $V_{DDH} = V_{ON} = 20\text{ V}$ $V_{OFF2} = V_{OFF1} = -20\text{ V}$	—	550	ns
	t_{pd6}		—	550	ns
On output rise time	t_{OR}	$CL = 220\text{ pF}$ $V_{DDH} = V_{ON} = 20\text{ V}$ $V_{OFF2} = V_{OFF1} = -20\text{ V}$	—	600	ns
On output fall time	t_{OF}		—	600	ns

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