EPSON

SED1794D0B

TFT LCD Driver

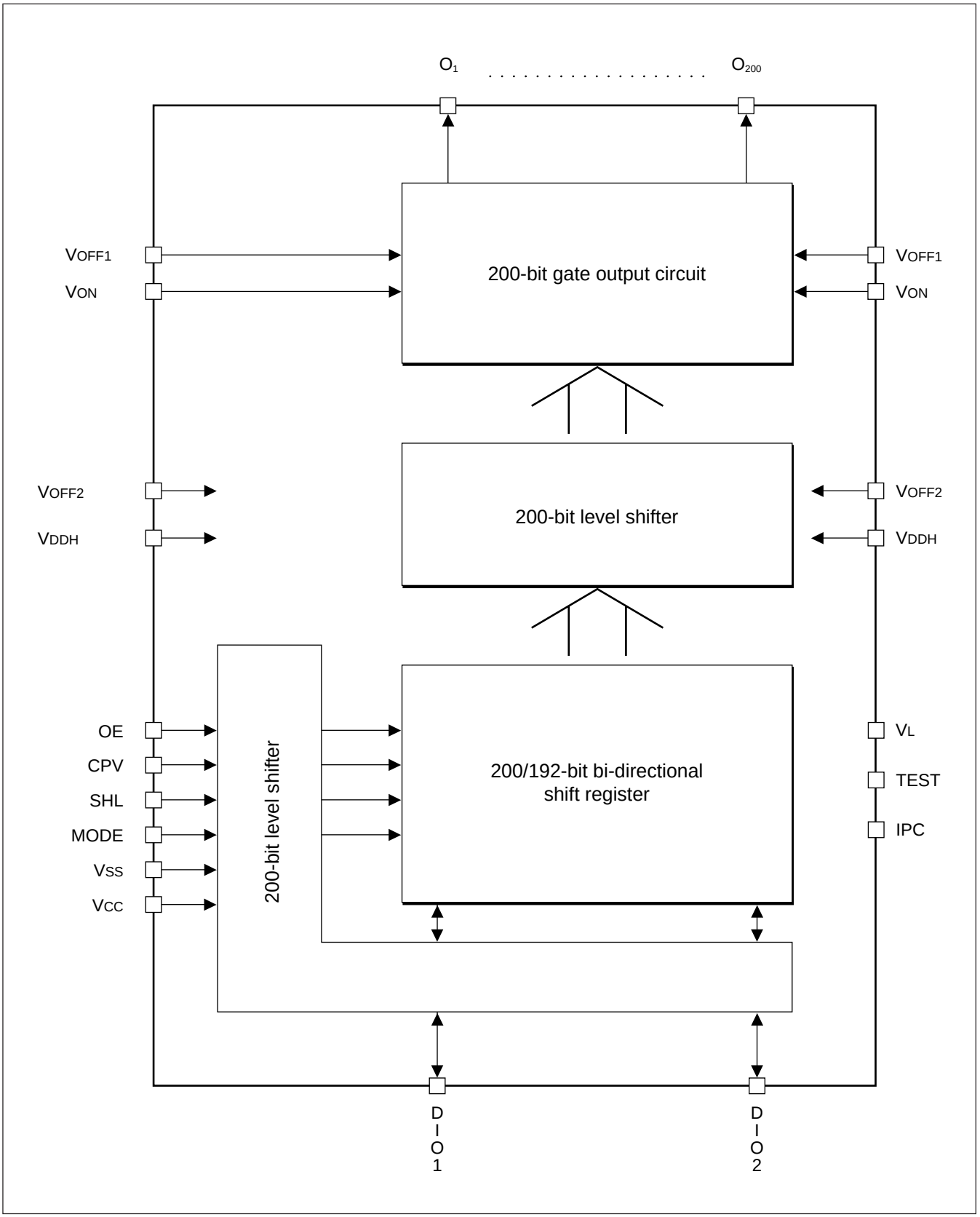
■ DESCRIPTION

The gate driver LSI SED1794 is designed to drive an active matrix LCD panel.
It enables high-voltage operation, positive and negative output voltages and is compatible with various TFT-LCD panel driving methods.
By switching the number of outputs between 200 and 192, it is compatible with the XGA/SXGA panel (192 outputs) and the SVGA panel (200 outputs)
Thanks to its slim TCP shape, it enables a small-architectured LCD module to be realized.

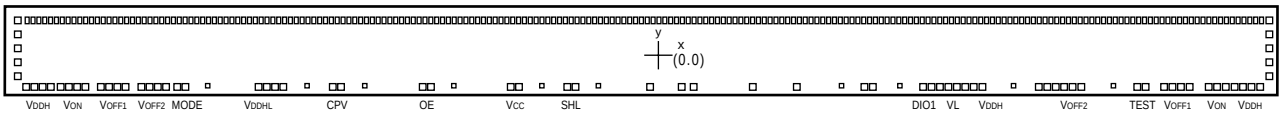
■ FEATURES

- Number of gate driving outputs: 200/192
- Super slim chip: Slim TCP
- Low voltage operation available: 2.7 V (min.)
- Output switching function available (200/192 outputs)
- Gate output voltage V_{ON} – V_{OFF1} amplitude: 40 V (max.)
- Output shift direction-pin selection.
- Output enable function
- Package to be shipped
  Au bump chip: SED1794D0B
  TCP: SED1794T**
- This LSI is not designed to resist radiation or light.

■ BLOCK DIAGRAM



■ PAD LAYOUT



Chip size: 16.00 mm × 1.08 mm
Pad pitch: Output pin = 79 µm (min.) *1
Same input pin = 99 µm (min.) *2
Between input pins = 119 µm (min.) *2
Chip thickness: 625 µm (typical)

Au bump specifications: SED1794D0B (reference)

	(X direction)		(Y direction)	
Bump size A:	50.4 µm	×	80.0 µm	*1
Bump size B:	77.6 µm	×	78.4 µm	*2
Bump size C:	49.6 µm	×	56.0 µm	*3
Bump size D:	50.4 µm	×	60.0 µm	*4
Bump size E:	58.4 µm	×	59.2 µm	*5

Notes
1. Pad # 81 to 280.
2. Pad # 1 to 18, 20 to 23, 25, 26, 28, 29, 31, 32, 34, 35, 37 to 41, 43, 44, 46 to 53, 55 to 60 and 62 to 75.
3. Pad # 76 to 79 and 282 to 285.
4. Pad # 80 and 281.
5. Pad # 19, 24, 27, 30, 33, 36, 42, 45, 54 and 61.

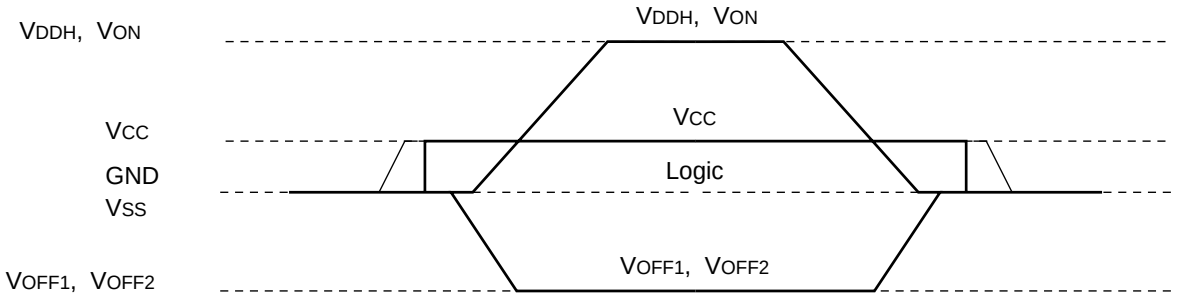
■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	–0.5 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.5 to +45.0	V
Supply voltage (3)	V_{OH}	–0.5 to V_{DDH} +0.5	V
Supply voltage (4)	V_{OFF1}, V_{OFF2}	–23.0 to +0.5	V
Supply voltage (5)	$V_{DDH} – V_{OFF2}$ $V_{ON} – V_{OFF1}$	–0.5 to +45.0	V
Input voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Input current	I_{IN}	±10	mA
Output current	I_O	±10	mA
Ambient operating temperature	Ta	–25 to +85	°C
Storing temperature	T_{stg2}	–55 to +125	°C

Notes

1. All power supplies refer to V_{SS} unless otherwise specified.
2. The LSI may permanently break if used outside the absolute maximum ratings shown above.
3. For voltages V_{CC}, V_{SS}, V_{DDH}, V_{ON}, V_{OFF1} and V_{OFF2}, be sure to keep the condition of "$V_{OFF2} \le V_{OFF1} \le V_{SS} \le V_{CC} \le V_{DDH}$".
4. Turn V_{CC}, V_{OFF2}/V_{OFF1} and V_{ON}/V_{DDH} on in this order and follow the opposite order when turning the power off.
5. Never float V_{CC} while a voltage of 10 V or higher is applied to $V_{DDH} – V_{OFF2}$ and $V_{ON} – V_{OFF1}$ or allow V_{CC} to go under 2.6 V, otherwise, an overcurrent may flow, disadvantageously affecting the LSI reliability.



■ RECOMMENDED OPERATING CONDITIONS

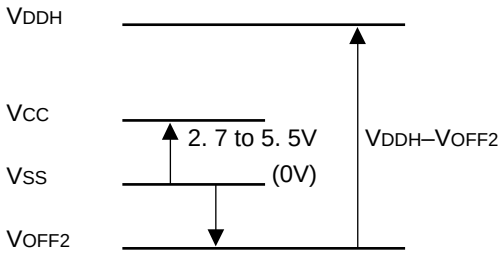
(V_{SS} = 0 V)

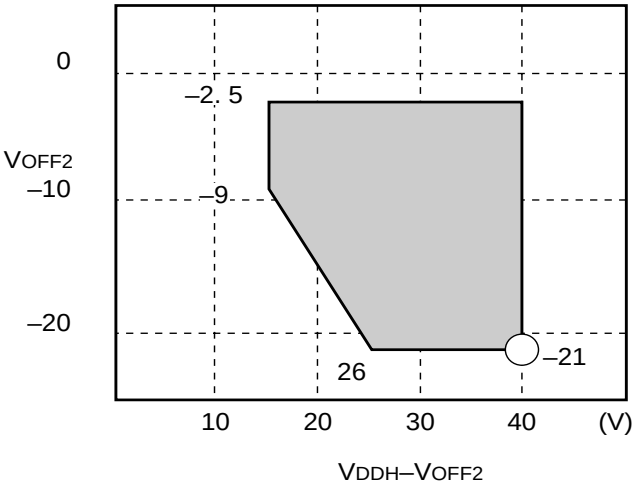
Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	2.7 to 5.5	V
Supply voltage (2)	V_{DDH}	10.0 to 40.0	V
Supply voltage (3)	V_{ON}	10.0 to 40.0	V
Supply voltage (4)	V_{OFF1}, V_{OFF2}	–21.0 to –2.5	V
Supply voltage (5)	$V_{DDH} – V_{OFF2}$ $V_{ON} – V_{OFF1}$	15 to 40.0	V
Operating frequency	f_{CPV}	DC to 400	kHz

Notes

1. LSI operation is guaranteed within the recommended operating condition range.
2. Allowing for the power supply impedance in the mounted status, insert a bypass capacitor for noiseproof measures near the V_{SS}, V_{OFF1} and V_{OFF2} pins.
3. Unless swinging the V_{OFF1} supply voltage, make the electric potential the same as that of V_{OFF2}.
4. When swinging the V_{OFF1} supply voltage, keep the range within "$V_{OFF2} \le V_{OFF1} \le V_{ON} – 15$ V". In this case, the guaranteed output resistance and fall time ratings will differ.

- **Recommended operating voltage range**
  The recommended operating voltage is based on the combination of the high-dielectric strength logic system power supply conditions and the logic system power supply conditions (the hatched portion in the figure below on the right).





◯ indicates the point where V_{OFF2} = –21V and V_{DDH} = 19V

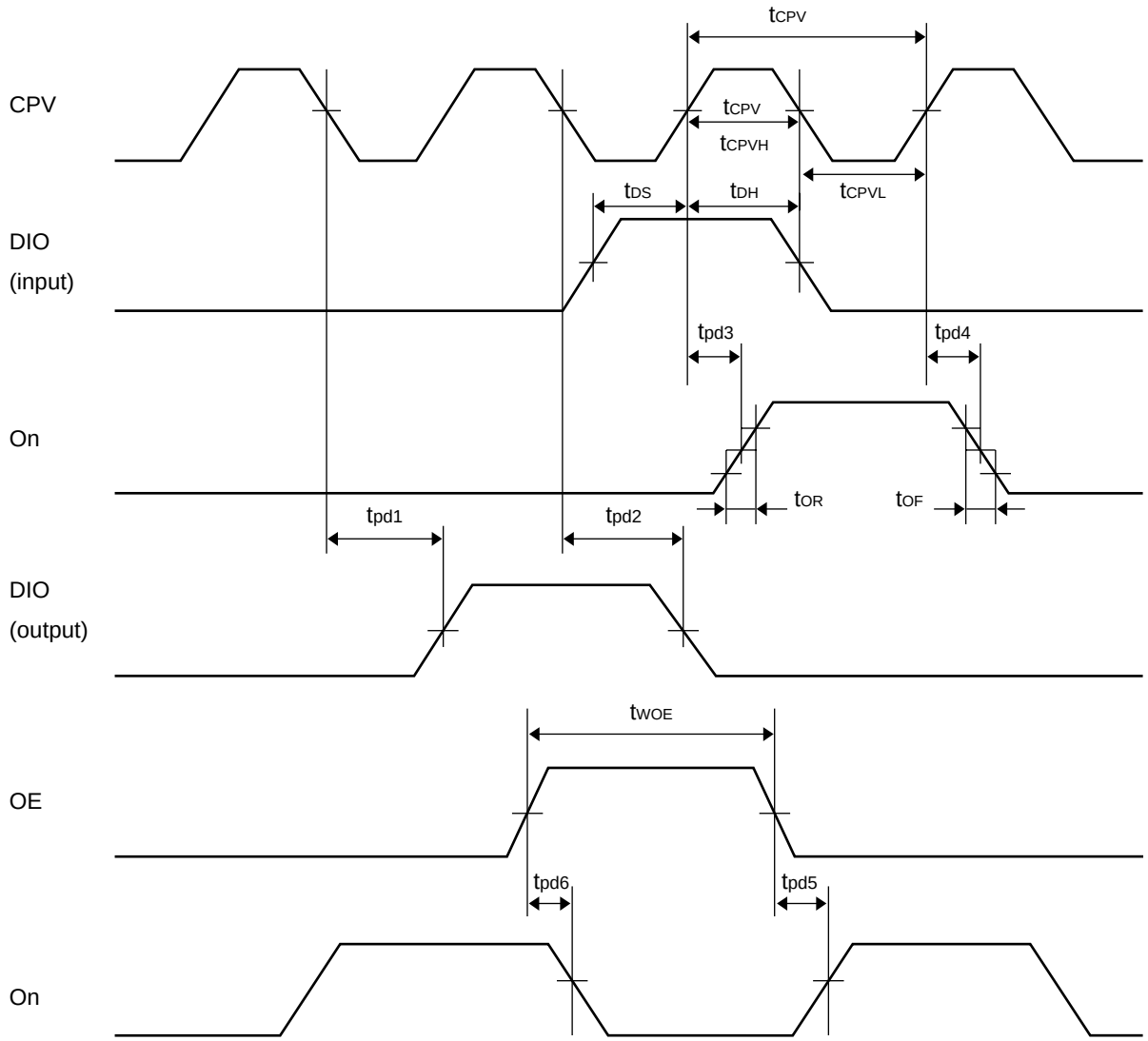
■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

Within the recommended operating voltage range when V_{SS} = 0 V and Ta = –25 to 85°C unless otherwise specified.

Parameter	Symbol	Condition		Rating			Units	Pin used
				Min.	Typ.	Max.		
"L" input voltage	V_{IL}	—		V_{SS}	—	0.3 × V_{CC}	V	All input pins
"H" input voltage	V_{IH}	—		0.7 × V_{CC}	—	V_{CC}	V	All input pins
"L" output voltage	V_{OL}	I_{OL} = 40 µA		V_{SS}	—	V_{SS} + 0.4		DIO1, 2
"H" output voltage	V_{OH}	I_{OH} = 40 µA		V_{CC} – 0.4	—	V_{CC}		DIO1, 2
Output resistance	R_{ON}	ΔVON = 1.0 V	V_{ON} – V_{OFF1} = 40 V	—	0.6	0.9	kΩ	O1 to O200
			V_{ON} – V_{OFF1} = 30 V	—	0.7	1.0		
			V_{ON} – V_{OFF1} = 15 V	—	0.9	1.5		
Input leakage current	I_{LI}	—		–1.0	—	1.0	µA	All input pins
Input capacity	C_{IN}	Ta = 25°C		—	—	15	pF	All input pins
Current consumption (1)	I_{CC}	f_{CPV} = 60 kHz		—	5	10	µA	V_{CC}
Current consumption (2)	I_{DDH}			—	380	990	µA	V_{DDH}
Current consumption (3)	I_{OFF}			—	–380	–990	µA	V_{OFF1}, V_{OFF2}

● **AC Characteristics**



Notes
The input and output signal timings refer to 50% of the signal amplitude.
On output signal t_{OR} and t_{OF} refer to 10% and 90%.

- **Input Timing Characteristics**
  Within the recommended operating voltage range when V_{SS} = 0 V and Ta = –25 to 85°C unless otherwise specified.

Parameter	Symbol	Condition	Min.	Max.	Unit
CPV cycle	t_{CPV}	During cascade connection	2.5	—	µs
CPV high-level pulse width	t_{CPVH}	—	400	—	ns
CPV low-level pulse width	t_{CPVL}	—	500	—	ns
Data setup time	t_{DS}	—	100	—	ns
Data hold time	t_{DH}	—	100	—	ns
$\overline{OE}$ high-level pulse width	t_{WOE}	—	700	—	ns

The logic input rise/fall times (t_r and t_f) are specified at 30 ns or less.

- **Output Timing Characteristics**
  Within the recommended operating voltage range when V_{SS} = 0 V and Ta = –25 to 85°C unless otherwise specified.

Parameter	Symbol	Condition	Min.	Max.	Unit
CPV to DIO output delay time	t_{pd1}	C_L = 20 pF	—	600	ns
	t_{pd2}			600	ns
CPV to On output delay time	t_{pd3}	C_L = 220 pF $V_{DDH} = V_{ON}$ = 20 V $V_{OFF2} = V_{OFF1}$ = –20 V	—	550	ns
	t_{pd4}		—	550	ns
$\overline{OE}$ to On output delay time	t_{pd5}	C_L = 220 pF $V_{DDH} = V_{ON}$ = 20 V $V_{OFF2} = V_{OFF1}$ = –20 V	—	550	ns
	t_{pd6}		—	550	ns
On output rise time	t_{OR}	C_L = 220 pF $V_{DDH} = V_{ON}$ = 20 V $V_{OFF2} = V_{OFF1}$ = –20 V	—	600	ns
On output fall time	t_{OF}		—	600	ns

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