EPSON

SED1753 Series

High Duty LCD Driver

- 120 Output Common Driver
- Slim TCP
- Common Output On-resistance 0.3kΩ (Typ.)

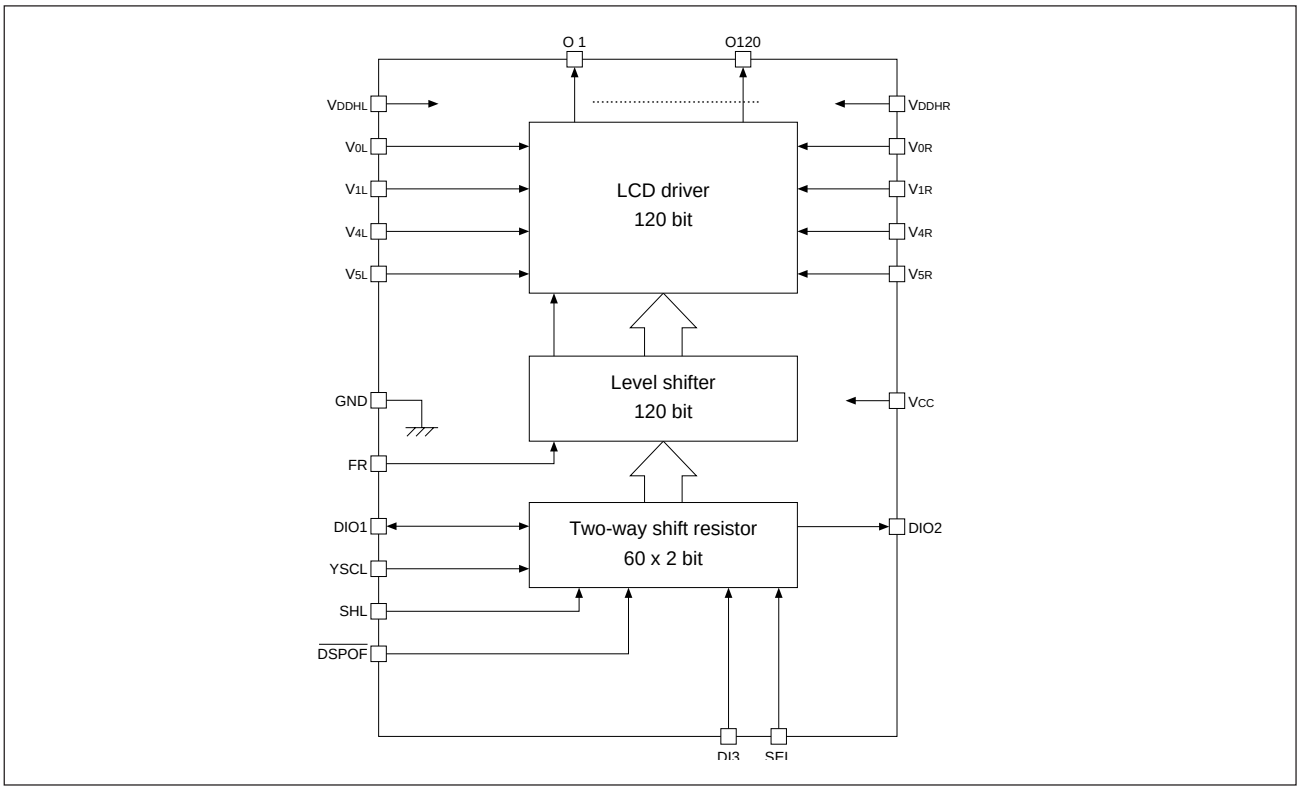
■ DESCRIPTION

SED1753 is a low output resistance-common (low) driver of 120 outputs suitable to drive dot matrix LCD panels of extremely large capacities for use in a pair with SED1752 or SED1758.
Thanks to its wide LCD drive voltage range and high density picture quality and owing to its slim shape contributing to thin profile LCD panel designs, SED1753 has a very wide application range.
Since two-way selection of the output sequence is available and as the SED1753 carries top-in-the-industry level 60 × 2 sets of high withstand voltage and low output impedance LCD outputs, highest driver efficiency can be expected with 1/240, 1/300 or 1/480 duty panels.

■ FEATURES

- 120 LCD drive output pins (60 × 2 layout)
- Common output-on resistance of 0.3kΩ (Typ.)
- High duty drive upto 1/480 is available (reference value)
- Pin selection in the output shift direction is feasible.
- Non-bias display off function
- Slim shape
- Off-set bias adjustment of the LCD power against V_{DDH} or GND level is available.
- A wide LCD drive voltage variations: 8V to 42V
- Logic power supply of 2.7V to 5.5V
- Shipped status: TCP
- Meanwhile, this IC is not of a radiation resistant structure.

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Num. of pin</th></tr>
<tr><td>O1 – O120</td><td>O</td><td>Common (Low) outputs for LCD drive.
They vary at the trailing edge of YSCL.</td><td>120</td></tr>
<tr><td>DIO1
DIO2</td><td>I/O</td><td>Scanning pulse of the 60 × 2 bit two-way shift resistor.
They can be set to input or output by SHL signals.
The output varies at the trailing edge of YSCL.</td><td>2</td></tr>
<tr><td>DI3</td><td>I</td><td>D13 is a scanning pulse input pin for the 60 × 2 configuration.
When SEL = L, it connects to D13 = GND.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Selective input of the two-way shift register operating mode.
H... 60 × 2 (D13 input) L .... 120</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Shift clock input of serial data.
Scanning data are shifted at the trailing edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>I/O control inputs for selection of the shift direction and I/O control inputs for the DIO terminals.
<table>
<tr><th>SHL</th><th colspan="5">O Output shift direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>H</td><td>1</td><td>→</td><td>60</td><td>61</td><td>→</td><td>120</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>120</td><td>→</td><td>61</td><td>60</td><td>→</td><td>1</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>Blanking control inputs of LCD indications.
By “L” input, all the common outputs become V5 level.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>For inputs of AC LCD-drive-outputs.</td><td>1</td></tr>
<tr><td>GND, V_{CC}</td><td>Power supply</td><td>Logic power supply. GND: 0V and V_{CC}: 2.7V to 5.5V</td><td>2</td></tr>
<tr><td>V_{0L}, V_{1L}, V_{4L}
V_{5L}, V_{DDHL}
V_{0R}, V_{1R}, V_{4R}
V_{5R}, V_{DDHR}</td><td>Power supply</td><td>LCD drive power supply.
GND : 0 V, V_{DDH} : 8V to 42 V
$V_{DDH} \geq V_0 \geq V_1$: 8/9 V_{DDH}
*1 1/9 $V_{DDH} \geq V_4 \geq V_5 \geq$ GND</td><td>10</td></tr>
</table>

*1 Always connect the pairs of V_{DDH} and V0 to V5 to respective LCD power supply. Total: 140
The voltage range given above for the LCD drive circuit power supply is a recommended range.

■ BLOCK FUNCTION

● Shift register

This is a two-way shift register for transferrence of common data.
The shift register is of a 60 × 2 bit configuration and selection between 60 × 2 bits or 120 bits is available changing the SEL status.
When 60 × 2 bit configuration is selected, the input to the later stage 60 bit shift register should be via D13.

● Level Shifter

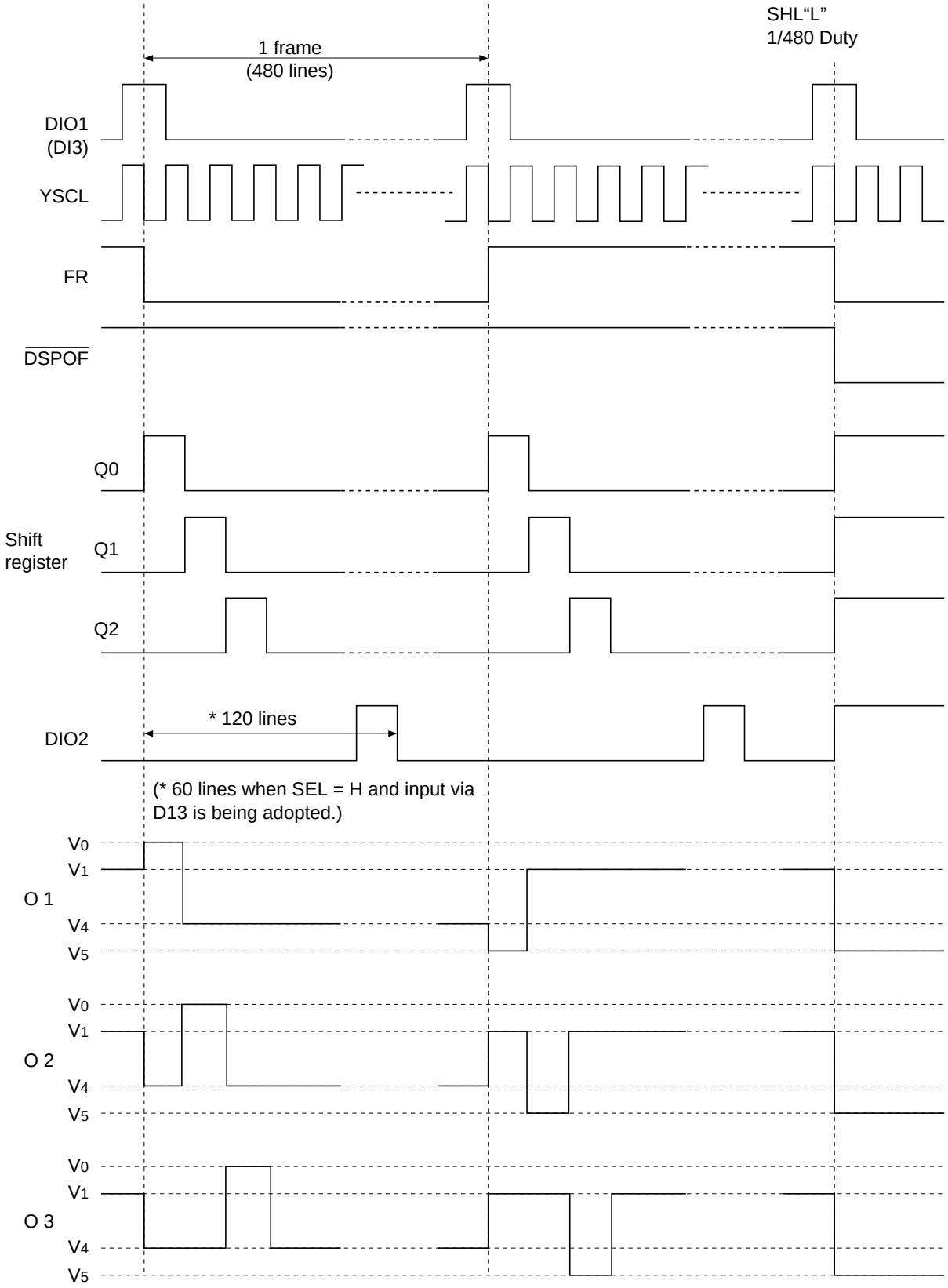
This is a voltage level interface circuit to shift the voltage level of signals from the logic level to the LCD drive level.

● LCD Driver

It outputs LCD drive voltage.
Given below are the relations among display blanking signals, shift register content, AC signal FR and common output voltage.

<table>
<tr><th>$\overline{DSPOF}$</th><th>Shift Register Content</th><th>FR</th><th colspan="2">ON Output Voltage</th></tr>
<tr><td rowspan="4">H</td><td rowspan="2">H</td><td>H</td><td>V_5</td><td rowspan="2">(Selecting Level)</td></tr>
<tr><td>L</td><td>V_0</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td><td rowspan="2">(Nonselecting Level)</td></tr>
<tr><td>L</td><td>V_4</td></tr>
<tr><td>L</td><td>–</td><td>–</td><td>V_5</td><td>–</td></tr>
</table>

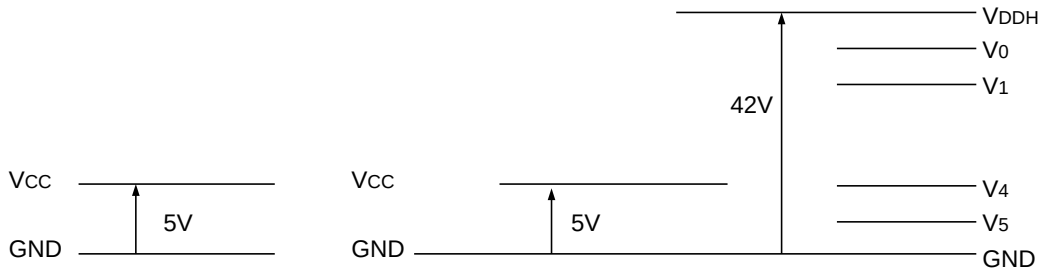
● **Timing Chart**



■ ABSOLUTE MAXIMUM RATINGS

Rating item	Symbol	Rating Value	Unit
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_1, V_4, V_5	GND –0.3 to V_{DDH} +0.3	V
Input voltage	V_I	GND –0.3 to V_{CC} +0.3	V
Output voltage	V_O	GND –0.3 to V_{CC} +0.3	V
DIO output current	I_O	20	mA
Operating temperature range	Topr	–40 to +85	°C
Chip storage temperature range	Tstg 1	–65 to +150	°C
TCP storage temperature range	Tstg 2	–55 to +125	°C

(Note 1) All the above voltage indications are based on GND = 0V.
(Note 2) V_0, V_1, V_4 and V_5 voltages must always be in the order of $V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq$ GND



(Note 3) If the logic power is made floated or becomes V_{CC} = 2.6V or less while LCD drive power is being applied, the LSI may be permanently damaged and avoid these situations. Pay particular attention when determining the power supply sequence for turning on and off of the system power.

■ ELECTRICAL CHARACTERISTICS

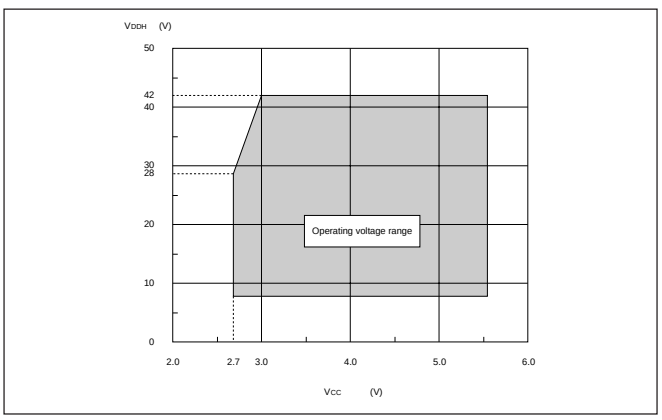
● DC Characteristics

(Unless otherwise designated: GND = V_5 = 0V, V_{CC} = 5.0V ±10%, Ta = –40 to 85°C)

Characteristic	Symbol	Condition		Pin	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{CC}	—		V_{CC}	2.7	5.0	5.5	V
Recommended working voltage	V_{DDH}	V_{CC} = 2.7 to 5.5 V		V_{DDHL}, V_{DDHR}	14.0	—	40.0	V
Workable voltage	V_{DDH}	Function only		V_{0L},V_{0R}	8.0	—	42.0	V
Supply voltage (2)	V_1	Recommended value		V_{1L}, V_{1R}	8/9•V_{DDH}	—	V_{DDH}	V
Supply voltage (3)	V_4	Recommended value		V_{4L}, V_{4R}	GND	—	1/9•V_{DDH}	V
High level input voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		DIO1,DIO2,FR YSCL, SHL,DI3, $\overline{DSPOF}$, SEL	0.8V_{CC}	—	—	V
Low level input voltage	V_{IL}				—	—	0.2•V_{CC}	V
High level output voltage	V_{OH}	V_{CC}= 2.7 to 5.5V	I_{OH} = –0.3mA	DIO1,DIO2	V_{CC}–0.4	—	—	V
Low level output voltage	V_{OL}		I_{OL} = 0.3mA		—	—	GND+0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		YSCL,SHL,DI3 $\overline{DSPOF}$,FR,SEL	—	—	2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		DIO1,DIO2	—	—	5.0	µA
Rest current	I_{GND}	V_{DDH} = 14.0 to 42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Output resistance	R_{COM}	△V_{ON} =0.5V Ta=25°C	V_{DDH}=+36.0V,1/24	O1-O120	—	0.29	0.48	KΩ
			V_{DDH}=+26.0V,1/20		—	0.3	0.5	
In-chip deviation of output resistance	△R_{COM}	V_{DDH}=+36.0V, 1/24 bias			—	—	50	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, f_{YSCL} = 33.6kHz f_{FR} = 70Hz, Input data: 1/480 Ta = 25°C No load		V_{CC}	—	TBD	TBD	µA
		V_{CC} = +3.0V Other conditions are the same as those when V_{CC} = 5V			—	TBD	TBD	
Mean working current consumption (2)	I_{DDH}	V_{DDH}=V_0=30.0V, V_1=28.0V V_4=2.0V, V_5=0.0V, V_{CC}=5.0V Other conditions are the same as those when I_{CC} column.		V_{DDHL} V_{DDHR}	—	TBD	TBD	µA
Input terminal capacity	C_I	Freq. = 1 MHz Ta = 25°C Independent chips	YSCL, SHL, $\overline{DSPOF}$, FR, DI3, SEL		—	—	8	pF
I/O terminal capacity	$C_{I/O}$		DIO1, DIO2		—	—	15	pF

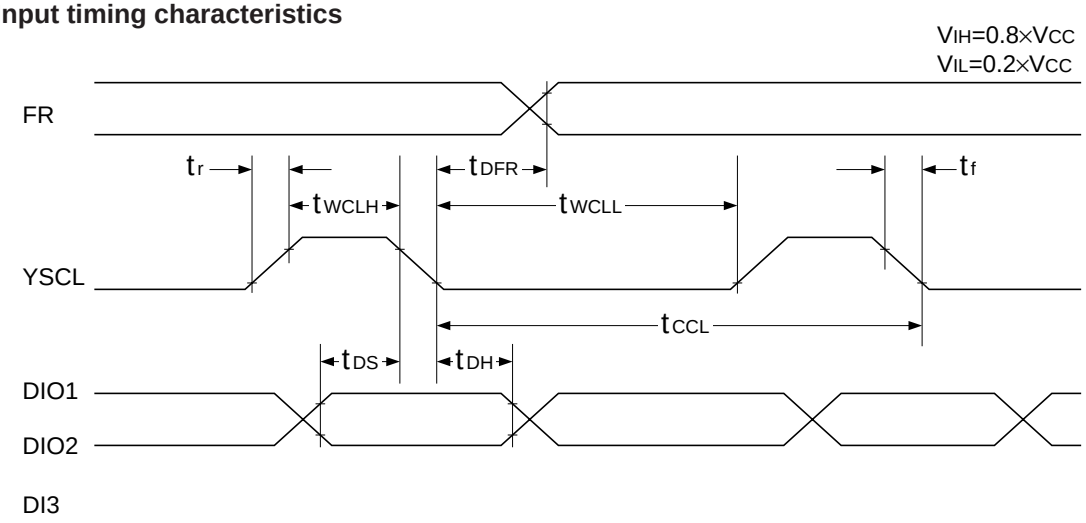
● Operating voltage range V_{CC} - V_{DDH}

Set up the V_{DDH} voltage within the V_{CC} - V_{DDH} operating voltage range given below:



● **AC Characteristics**

○ **Input timing characteristics**



(VCC = 5.0V ±10%, Ta = –40 to +85°C)

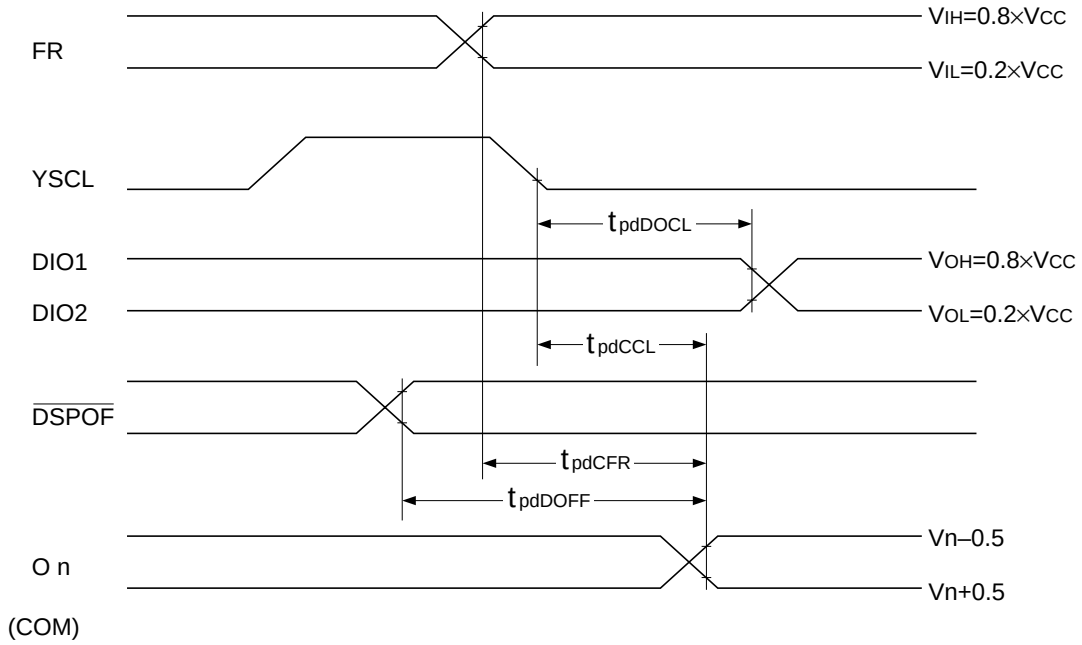
Characteristic	Symbol	Condition	Min.	Max.	Unit
YSCL cycle	t_{CCL}	—	400	—	nS
YSCL “H” pulse duration	t_{WCLH}	—	60	—	nS
YSCL “L” pulse duration	t_{WCLL}	—	330	—	nS
Data setup time	t_{DS}	—	50	—	nS
Data hold time	t_{DH}	—	40	—	nS
Input signal rise time	t_r	—	—	50	nS
Input signal fall time	t_f	—	—	50	nS

(VCC = 2.7V to 4.5V, Ta = –40 to +85°C)

Characteristic	Symbol	Condition	Min.	Max.	Unit
YSCL cycle	t_{CCL}	—	800	—	nS
YSCL “H” pulse duration	t_{WCLH}	—	80	—	nS
YSCL “L” pulse duration	t_{WCLL}	—	660	—	nS
Data setup time	t_{DS}	—	90	—	nS
Data hold time	t_{DH}	—	70	—	nS
Input signal rise time	t_r	—	—	50	nS
Input signal fall time	t_f	—	—	50	nS

*1 t_{DFR}: The changing point of FR signals and falling timing of LP signals should basically be set up within the range where the “On” output waveform does not become abnormal at “Ons”.

○ **Output timing characteristics**



(VCC = 5.0V ±10%, VDDH = 14.0 to 42.0V, Ta = –40 to +85°C)

Characteristic	Symbol	Condition	Min.	Max.	Unit
(YSCL fall → DIO) Delay time	t_{pdDOCL}	CL = 15pF	—	100	nS
(YSCL fall → On output) Delay time	t_{pdCCL}	CL = 100pF	—	200	nS
($\overline{DSPOF}$ → On output) Delay time	$t_{pdCDOFF}$				
(FR → On output) Delay time	t_{pdCFR}		—	300	nS

(VCC = 2.7V to 4.5V, VDDH = 14.0 to 28.0V, Ta = –40 to +85°C)

Characteristic	Symbol	Condition	Min.	Max.	Unit
(YSCL fall → DIO) Delay time	t_{pdDOCL}	CL = 15pF	—	200	nS
(YSCL fall → On output) Delay time	t_{pdCCL}	CL = 100pF	—	400	nS
($\overline{DSPOF}$ → On output) Delay time	$t_{pdCDOFF}$				
(FR → On output) Delay time	t_{pdCFR}		—	600	nS

■ LCD driving power

● Setting up of the respective voltage levels

To set up respective voltage levels for LCD drive, it is best to use the voltage follower by the operation amplifier dividing potentials between V_{DDH} and GND by resistors.
In preparation for use of the operation amplifier, it is suggested to separate the maximum potential levels V_0 and V_{DDH} and minimum potential levels V_5 and GND for LCD drive to separate pins.
Normally, connect V_0 and V_{DDH}, V_5 and GND to drive V_1 and V_4 by the voltage follower. When driving V_0 by the voltage follower, maintain the potential difference between V_{DDH} and V_0 within the range of 0V to 2.5V, since the efficiency of the LCD driving output driver deteriorates if the potential of the V_0 rises higher than the potential of the V_{DDH} to expand the potential difference.

When series resistance exists in the power lines to the GND and V_{DDH}, GND and V_{DDH} voltage drops occur at the power supply end of the LSI by the effect of I_{DDH} when the signal is being changed, thus making it impossible to maintain the prescribed order of the intermediate potentials of the LCD ($V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq$ GND) leading to breakage of the LSI.
Therefore, when inserting protective resistors, it becomes necessary to stabilize the potential by use of appropriate capacitance.

● Regarding stabilization of the power supply

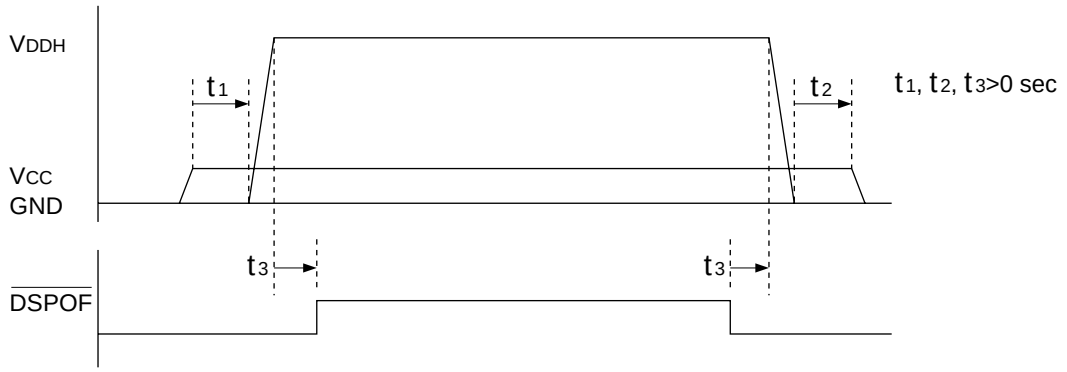
To prevent influence of noise occurring from passages of power lines and signal lines on the package substrate, it becomes necessary to insert bypass capacitors between power supplies (GND - V_{CC}, GND - V_{DDH}) to stabilize the potential as occasion calls.

● Precautions when setting up power on-off sequences.

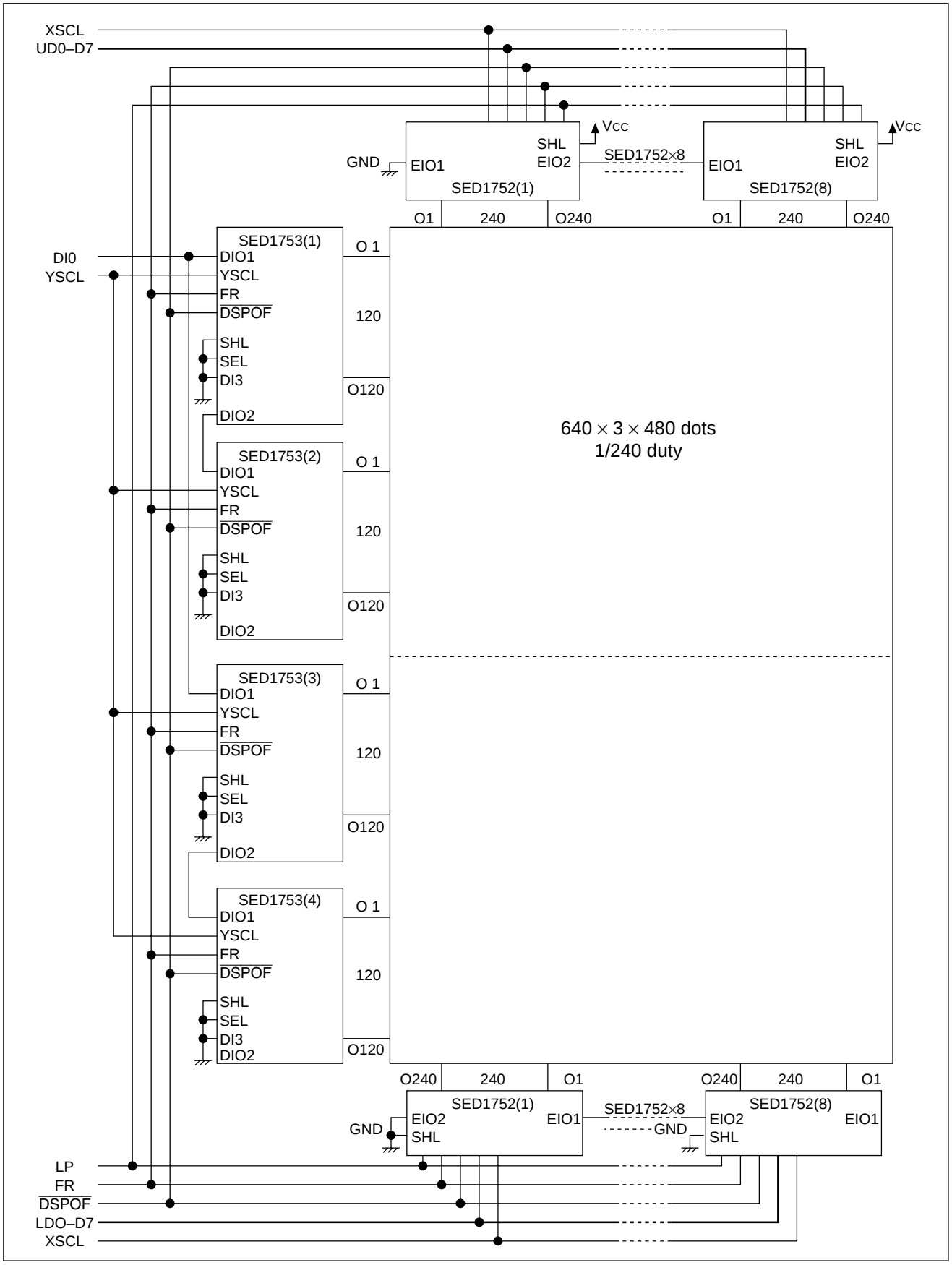
Since the LCD driving voltage is high with this LSI, when logic power is floated or when high LCD drive voltage is applied with the V_{CCS} remaining lower than 2.6V, or when LCD drive signals are output before the LCD drive voltage is stabilized, excess current flows through to possibly damage the LSI.
Therefore, it is suggested that the LCD drive output potentials be maintained at the V_5 level until the LCD drive voltage gets stabilized, using the display-off ($\overline{DSPOF}$) function

Maintain the following sequence when turning the power on and off.

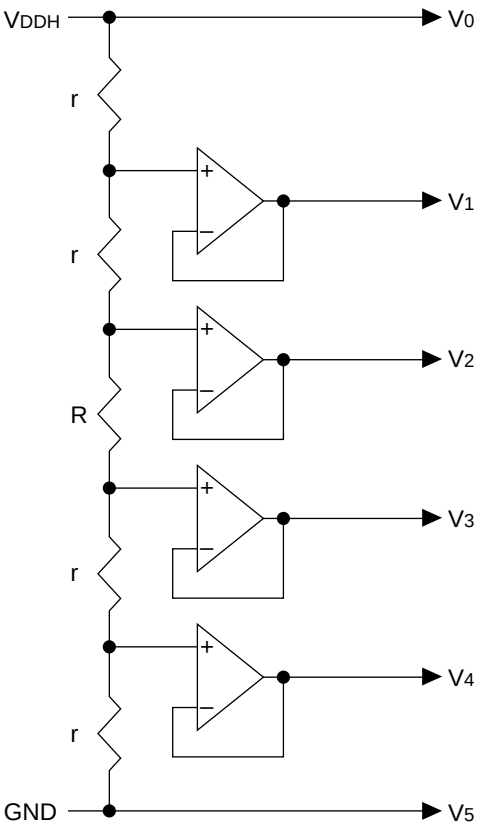
When turning the power on: Logic circuit "on" → LCD drive circuit "on", or both circuits "on" simultaneously.
When turning the power off: LCD drive circuit "off" → Logic circuit "off", or both circuits "off" simultaneously.



■ LCD PANEL CONNECTION EXAMPLE



● An example of LCD drive power circuit

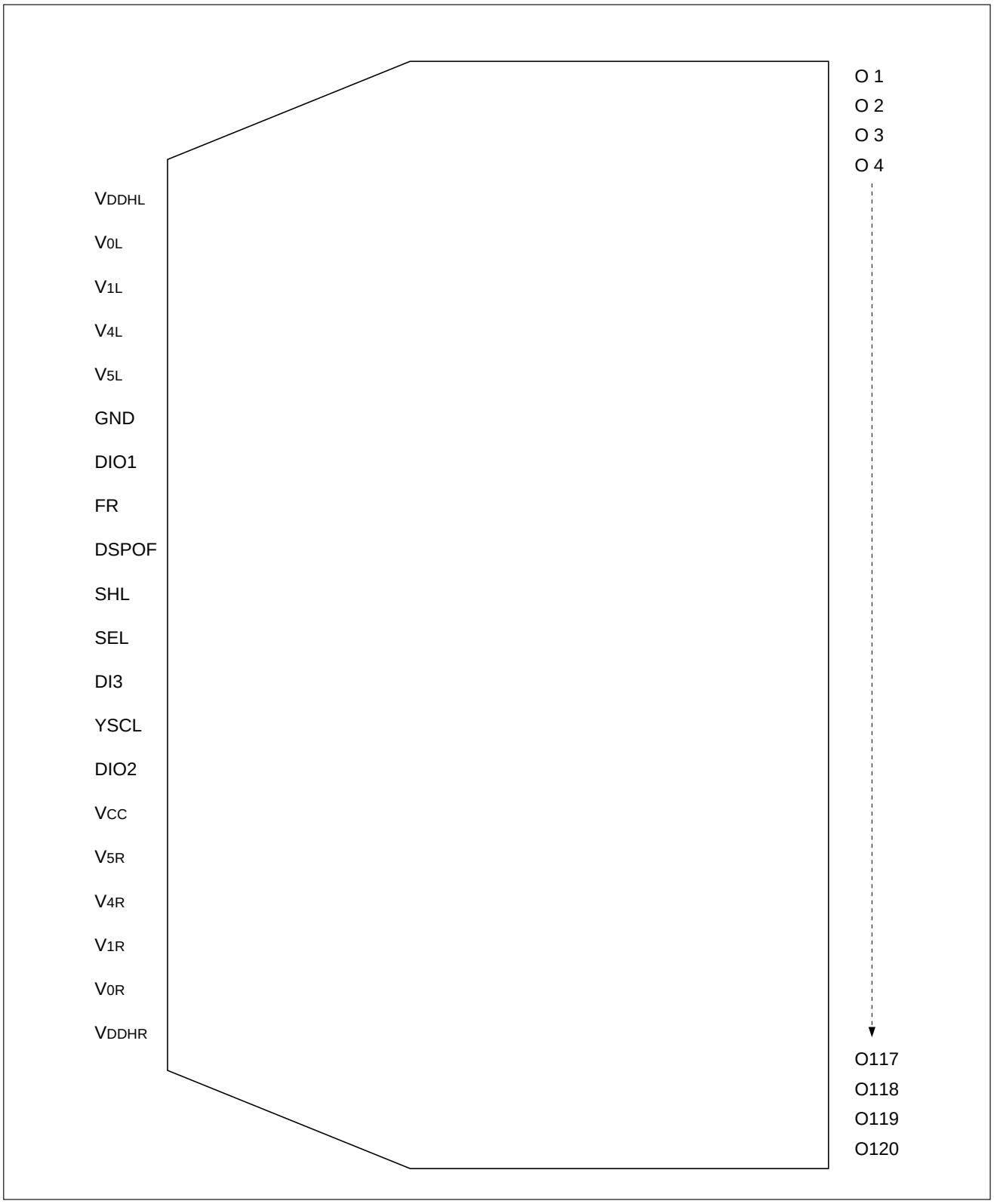


- It is necessary to provide smoothing capacitance to appropriate places on the LCD module for stabilization of LCD driving power supplies (V_0 through V_5).
- V_0, V_1, V_4 and V_5 supply power to the SED1753 and V_0, V_2, V_3 and V_5 supply power to the 7SED1752.
- Logic circuit voltage V_{CC} is supplied to each IC.
- As a noise prevention method, it is necessary to provide bypass capacitors at appropriate places between GND and V_{CC} and between GND and V_{DDH} to stabilize the supply voltage.
  Also, it is suggested to separate the high withstand voltage power supply (GNDR and GNDL) and logic power supply (GND) to different circuits.

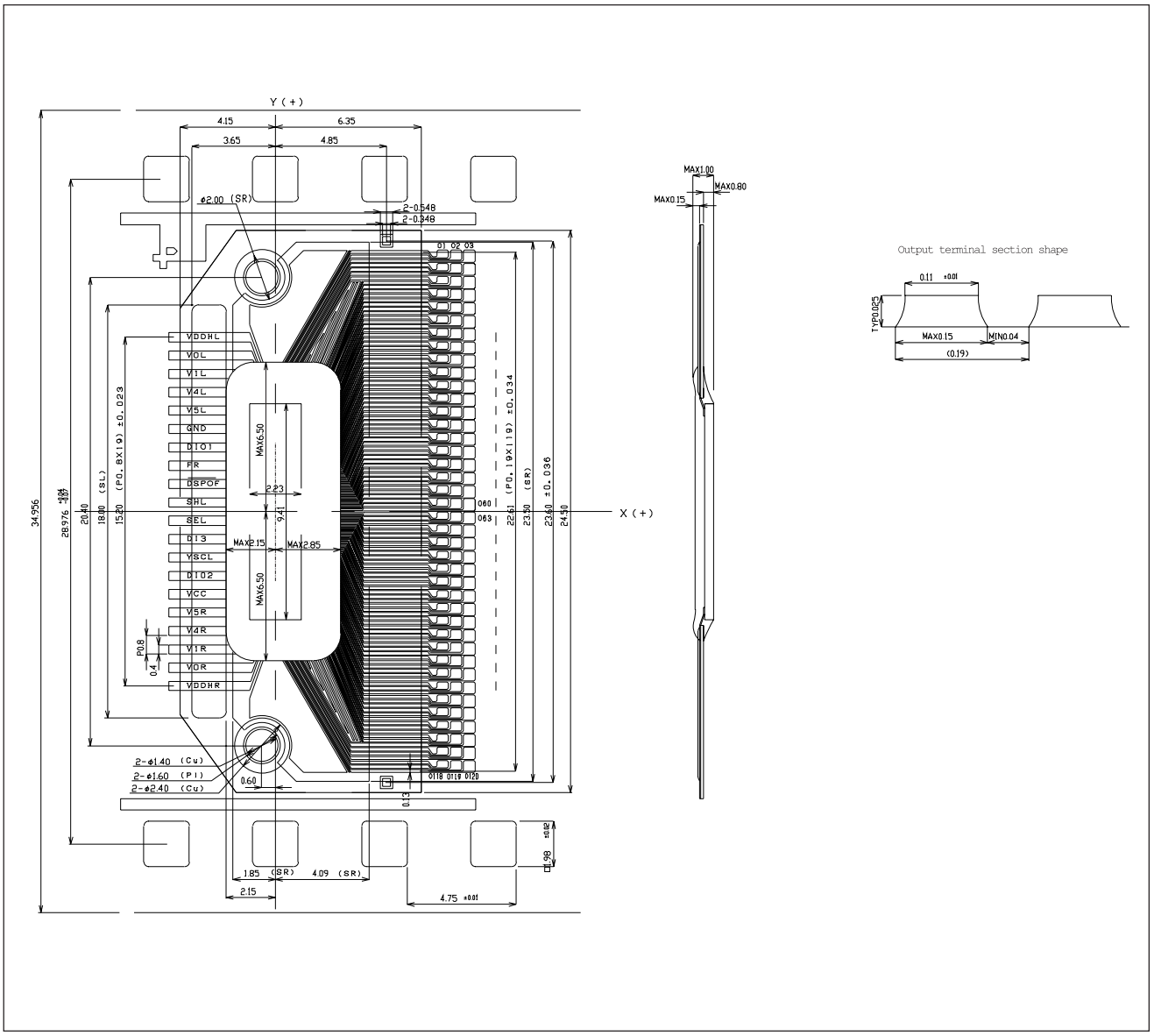
■ SED1753T TCP PIN LAYOUT

Remark) This layout drawing is not meant to specify the external shape and dimensions of the TCP.

For reference



■ TCP EXTERNAL DIMENSIONS



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