EPSON

SED15A6

Dot Matrix LCD Driver

- Support up to 55×102 Display
- Built-in Power Supply Circuit for LCD
- Few External Parts Required

■ OVERVIEW

The SED15A6 series is a single-chip liquid crystal display (=LCD) driver for dot-matrix LCDs that can be connected directly to a microprocessor (=MPU) bus. It accepts 8-bit parallel or serial display data from a MPU, stores it in an on-chip display data RAM (=DDRAM), and generates a LCD drive signal independent of the MPU clock.

The use of the on-chip DDRAM of 65×102 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip DDRAM bits offer high flexibility in graphic display.

The SED15A6 series does not need external operation clock for DDRAM read/write operations, and has a on-chip LCD power supply circuit featuring very low current consumption with few external components, and moreover has a on-chip CR oscillator circuit.

And the SED15A6 does not need smoothing capacitor on the LCD power supply.

Consequently, the SED15A6 series can be realize a high-performance handy display system with a minimum current consumption and the fewest components.

■ FEATURES

- Direct display of RAM data through the display data RAM.
- RAM bit data : "1" Non-illuminated
  "0" Illuminated
  (during normal display)
- RAM capacity 65×102 = 6630 bits
- Display driver circuits
  SED15A6*** : 55 common output and 102 segment outputs
- High-speed 8-bit MPU interface (The chip can be connected directly to the 8080 series MPUs and the 6800 series MPUs)
- High-speed Serial interface are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, common driver direction select, V_0 voltage regulation internal resistor ratio set.
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit(with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally)
  - High-accuracy voltage adjustment circuit
    (Thermal gradient –0.1%/°C)
  - V_0 voltage divider resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.

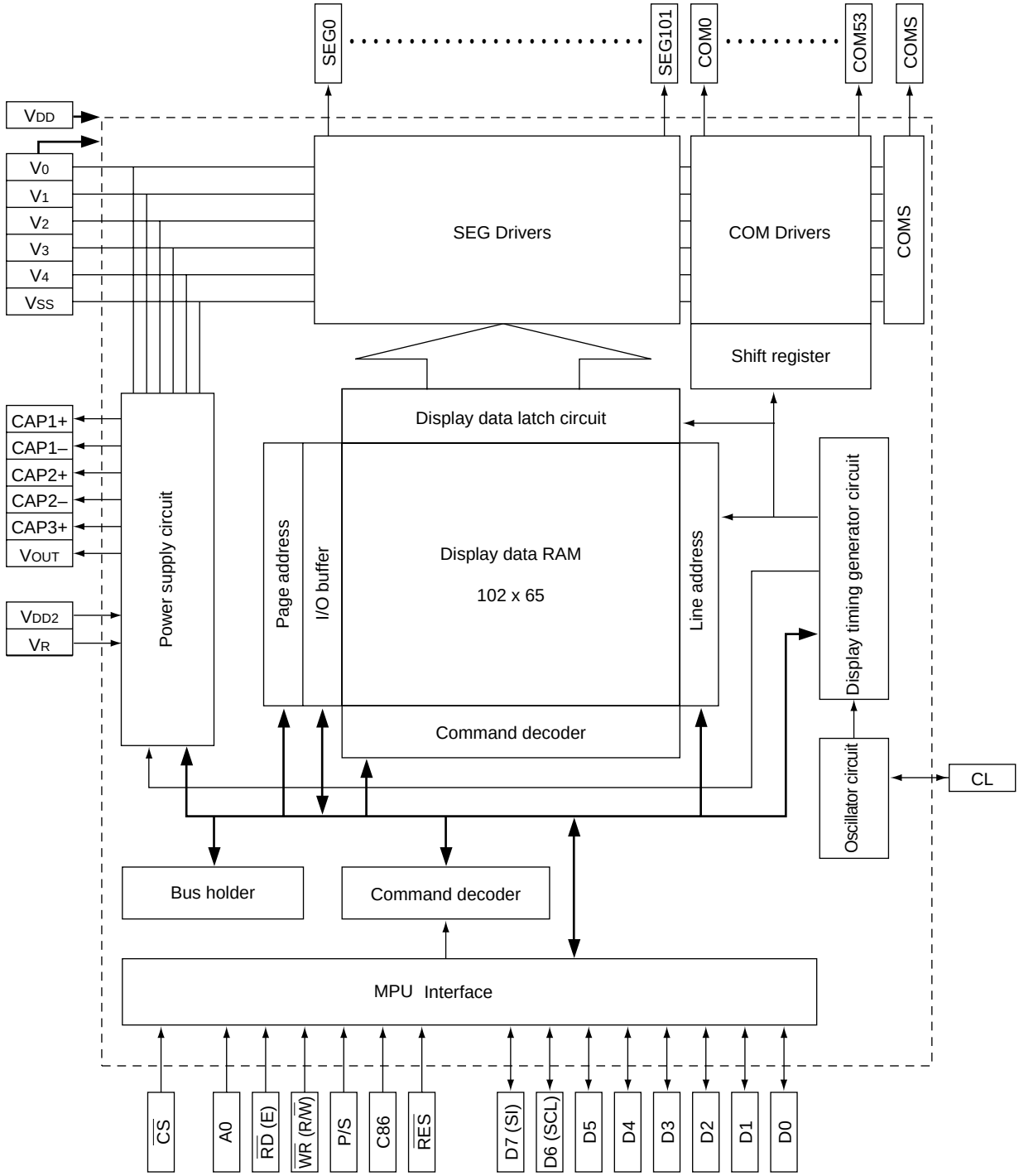
- Component that can be omitted (you may omit the smoothing capacitor on the voltage follower).
- CR oscillator circuit equipped internally (external clock can also be input)
- Extremely low power consumption
  Operating power when the built-in power supply is used (an example)
  SED15A6D$_{0B}$ (79µA)
  Condition : V_{DD}–V_{SS} = 1.8V, V_{DD2}–V_{SS} = 3.3V,V_0–V_{SS} = 9.0V, triple boosting, all white is displayed, Ta = 25°C
- Power supply
  Operable on the low 1.8 voltage
  Logic power supply : V_{DD}–V_{SS} = 1.8V to 3.6V
  Boost reference voltage : V_{DD2}–V_{SS} = 1.8V to 5.0V
  Liquid crystal drive power supply : V_0–V_{SS} = 4.5V to 9.0V
- Wide range of operating temperatures : -40 to +85°C
- CMOS process
- Shipping forms include bare chip and TCP.
- There chip not designed for resistance to light or resistance to radiation.

Series Specifications

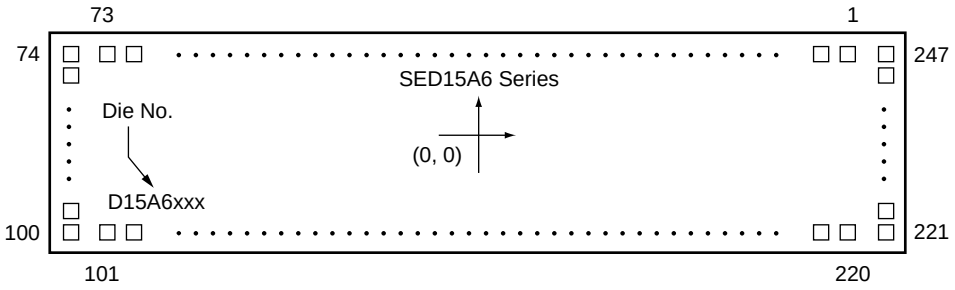
Product Name	Duty	Bias	SEG Dr	COM Dr	V_{REG} Temperature Gradient	Shipping Forms
SED15A6D$_{0B}$	1/55	1/6,1/8	102	55	–0.1%/°C	Bare Chip
SED15A6T$_0$	1/55	1/6,1/8	102	55	–0.1%/°C	TCP

* : Under preparation.

■ BLOCK DIAGRAM



■ PIN DIMENSIONS



		Size X	Size Y	Unit
Chip Size		9.93 × 2.15		mm
Chip Thickness		0.625		mm
Bump Pitch		70 (Min.)		µm
Bump Size	PAD No.1 to 73	85 × 85		µm
	PAD No.74	85 × 74		µm
	PAD No.75 to 99	85 × 45		µm
	PAD No.100	85 × 74		µm
	PAD No.101 to 220	52 × 85		µm
	PAD No.221	85 × 74		µm
	PAD No.222 to 246	85 × 45		µm
	PAD No.247	85 × 74		µm
Bump Height		17 (Typ.)		µm

■ PIN DESCRIPTION

● Power supply pins

Name	I/O	Description	Number of pins
V_{DD}	Supply	Power supply. Connect to MPU power pin V_{CC}.	5
V_{DD2}	Supply	Externally-input reference power supply for booster circuit.	3
V_{SS}	Supply	This is a 0V terminal connected to the system GND.	7
V_0, V_1, V_2 V_3, V_4	Supply	Multi-level power supply for LCD drive. The voltages are determined by LCD cell.The voltages should maintain the following relationship : $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$. When on-chip power supply circuit turns on, V_0 voltage are generated, and the following voltages are generated to V_1 to V_4. Either voltage can be selected by LCD bias set command.	5

	SED15A6***
V_1	5/6 • V0, 7/8 • V0
V_2	4/6 • V0, 6/8 • V0
V_3	2/6 • V0, 2/8 • V0
V_4	1/6 • V0, 1/8 • V0

● LCD power supply circuit pins

Name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP1- pins.	2
CAP1−	O	Boosting capacitor negative connection pin. Capacitor is connected across CAP1+ pins.	2
CAP2+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP2− pins.	2
CAP2−	O	Boosting capacitor negative connection pin. Capacitor is connected across CAP2+ pins.	2
CAP3+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP1− pins.	2
V_{OUT}	O	Booster output. Capacitor is connected across V_{SS} or V_{DD2}.	4
V_R	I	Voltage adjustment pin. Provides V_0 voltage using external resistors. When internal resistors are used, this pin cannot be used. Operable only when the built-in resistor for V_0 adjustment is not used. [V_0 resistance ratio is (D2, D1, D0) = (1.1.1)] This pin is disabled when the built-in resistor for V_0 adjustment is used. This pin must be open in this case.	1

● **System bus connection pins**

Pin name	I/O	Description	Number of pins
D7 to D0 (SL) (SCL)	I/O	8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit MPU data bus. When the serial interface is selected (P/S="L") ; D7 : Serial data input (SI) D6 : Serial clock input (SCL) At this time, D0 through D5 will go under the Hz mode. When the chip selects are in non-active state, D0 through D7 will go under the Hz mode.	8
A0	I	Control/data flag input. A0="H" : The data on D7 to D0 is display data. A0="L" : The data on D7 to D0 is control data.	1
$\overline{CS}$	I	Chip select input. Data input is enable when $\overline{CS}$ is low.	1
$\overline{RES}$	I	When $\overline{RES}$ is caused to go low, initialization is executed. A reset operation is performed at the signal level.	1
$\overline{RD}$ (E)	I	• When connected to an 8080-series MPU ; This is active-LOW. This pin is connected to the $\overline{RD}$ signal of the 8080-series MPU. While this signal is low, SED15A6 series data bus in an output status. • When connected to an 6800-series MPU ; This is active-HIGH. This is used as an enable clock input pin of the 6800-series MPU.	1
$\overline{WR}$ (R/$\overline{W}$)	I	• When connected to an 8080-series MPU ; This is active-LOW. This pin is connected to the $\overline{WR}$ signal of the 8080-series MPU. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. • When connected to an 6800-series MPU ; This is the read/write control signal input . R/$\overline{W}$="H" : Read. R/$\overline{W}$="L" : Write.	1
C86	I	MPU interface selection pin. C86="H" : 6800-series MPU interface C86="L" : 8080-series MPU interface	1
P/S	I	Serial data input/parallel data input selection pin. P/S="H" : Parallel data input P/S="L" : Serial data input The following applies depending on the P/S status :	1

P/S	Data/Command	Data	Read/Write	Serial Clock
"H"	A0	D7 to D0	$\overline{RD}$, $\overline{WR}$	–
"L"	A0	SI (D7)	Write only	SCL (D6)

In serial mode, no data can be read from DDRAM.
When P/S="L", D5 to D0 are HZ. D5 to D0 may be "H", "L" or Open, and moreover A0, RD, WR, C86 may be "H" or "L".

● LCD driver pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CL</td><td>I</td><td>This pin is used for enabling or disabling the built-in oscillation circuit for the display clock.
CL = "H": Built-in oscillation circuit is enabled.
CL = "L": Built-in oscillation circuit (external input) is disabled.
Select CL = "L" to turn the external clock off.
When using the built-in oscillation circuit, select CL = "H" (V_{DD}).</td><td>1</td></tr>
<tr><td>SEG0
to SEG101</td><td>O</td><td>These pins output the signal for the segment drive of LCD.
One of V_0, V_2, V_3 and V_{SS} levels is selected depending on a given combination of display RAM data and internal FR signal.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">Internal FR signal</th><th colspan="2">Output voltage</th></tr>
<tr><th>Normal display</th><th>Reversing display</th></tr>
<tr><td>H</td><td>H</td><td>V_0</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_0</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td>Power save</td><td>–</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0
to COM53</td><td>O</td><td>These pins output the signal for the common drive of LCD.
Following number of pins are assigned to SED15A6*$_{**}$.
<table>
<tr><th>Model</th><th>COM</th><th>Number of COM pins</th></tr>
<tr><td>SED15A6*$_{**}$</td><td>COM0~COM53</td><td>54</td></tr>
</table>
One of V_0, V_1, V_4 and V_{SS} levels is selected depending on a given combination of scan data and FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V_0</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{SS}</td></tr>
</table></td><td>54</td></tr>
<tr><td>COMS</td><td>O</td><td>They are COM pins exclusively used for the indicator.
Both pins output the same signal.
They must be made open when not used.</td><td>2</td></tr>
</table>

● Test pins

Name	I/O	Description	Number of pins
TEST0 to 10	I/O	These are terminals for IC chip testing. They are set to OPEN.	11

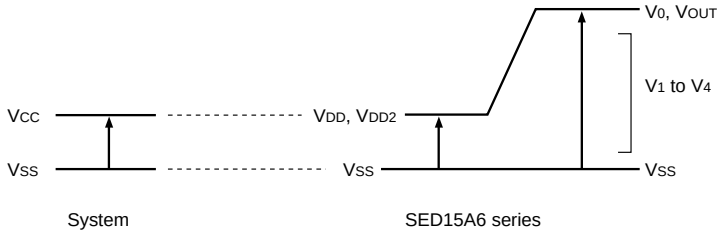
Total : 220 pins for the SED15A6*$_{**}$.

Note: If control signal from MPU is Hz,an over-current may flow through the IC. A protection is required to prevent the Hz signal at the input pins.

■ ABSOLUTE MAXIMUM RATING

Unless otherwise noted, V_{SS} = 0V.

Parameter		Symbol	Conditions	Unit
Power supply voltage (1)		V_{DD}	–0.3 to 0.6	V
Power supply voltage (2)		V_{DD2}	–0.3 to 0.6	V
	Double boosting		–0.3 to 5.0	
	Triple boosting		–0.3 to 3.3	
	Quadruple boosting		–0.3 to 2.5	
Power supply voltage (3)		V_0, V_{OUT}	–0.3 to 10.0	V
Power supply voltage (4)		V_1, V_2, V_3, V_4	–0.3 to V_0	V
Input voltage		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage		V_O	–0.3 to V_{DD}+0.3	V
Operating temperature		T_{OPR}	–40 to 85	°C
Storage temperature	TCP	T_{STR}	–55 to 100	°C
	Bare chip		–55 to 125	



Notes: 1. V_{SS} = 0V is assumed for every voltage indicated above.
2. Voltage V_0, V_1, V_2, V_3, V_4 must always keep up the condition of V_0 >= V_1 >= V_2 >= V_3 >= V_4 >= V_{SS} and V_{OUT} >= V_0 >= V_{SS}.
3. If the LSI exceeds its absolute maximum rating, it may be damage permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.

■ DC CHARACTERISTICS

V_{SS}=0V, V_{DD}=3V±10%, Ta=–40~85°C unless otherwise noted.

Item		Symbol	Condition	Standard value			Unit	Pin used
				Min.	Typ.	Max.		
Supply voltage(1)	Recommended operation	V_{DD}	(V_{SS} is used as the reference)	2.7	–	3.3	V	V_{DD} *1
	Operational available	V_{DD}	(V_{SS} is used as the reference)	1.8	–	3.6	V	
Supply voltage(2)	Recommended operation	V_{DD2}	(V_{SS} is used as the reference)	1.8	–	5.0	V	V_{DD2} *1
Supply voltage(3)	Operational available	V_0	(V_{SS} is used as the reference)	4.5	–	9.0		V_0 *2
	Operational available	V_1, V_2	(V_{SS} is used as the reference)	0.6×V_0	–	V_0	V	V_1, V_2
	Operational available	V_3, V_4	(V_{SS} is used as the reference)	V_{SS}	–	0.4×V_0		V_3, V_4
High-level input voltage		V_{IH}		0.7×V_{DD}	–	V_{DD}	V	*3
Low-level input voltage		V_{IL}		V_{SS}	–	0.3×V_{DD}		
High-level output voltage		V_{OH}	I_{OH}=–0.5mA	0.7×V_{DD}	–	V_{DD}	V	*4
Low-level output voltage		V_{OL}	I_{OL}=0.5mA	V_{SS}	–	0.3×V_{DD}		
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}	–1.0	–	1.0	µA	*5
Output leakage current		I_{LO}		–3.0	–	3.0	µA	*6
LCD driver ON resistance		R_{ON}	V_0=7.0V Ta=25°C	–	2.0	5.0	KΩ	SEGn, COMn *7
Static current consumption		I_{DDQ}	Ta=25°C	–	0.01	5.0	µA	V_{DD},V_{DD2}
Output leak current		I_{OQ}	V_0=7.0V Ta=25°C	–	0.01	15.0	µA	V_0
Input terminal capacitance		C_{IN}	Ta=25°C, f =1MHz		5.0	8.0	pF	
Oscillation frequency	Built-in oscillation	f_{OSC}	Ta=25°C	31.68	35.20	38.72	kHz	*8
	External input	f_{CL}		35.2	70.4	140.8		CL *8

Item		Symbol	Condition	Standard value			Unit	Pin used
				Min.	Typ.	Max.		
Built-in power supply circuit	Input voltage	V_{DD2}	When voltage is doubled (Vss is used as the reference)	1.8	–	5.0	V	V_{DD2} *1
			When voltage is tripled (Vss is used as the reference)	1.8	–	3.3		
			When voltage is quadrupled (Vss is used as the reference)	1.8	–	2.5		
	Boosted output voltage	V_{OUT}	(Vss is used as the reference)	–	–	10.0		V_{OUT}
	Operating current of voltage adjustment circuit	V_{OUT}	(Vss is used as the reference)	5.0	–	10.0		V_{OUT}
	V/F circuit operating voltage	V_0	(Vss is used as the reference)	4.5	–	9.0		V_0 *9
	Reference voltage	V_{REG}	–0.1%/°C Ta=25°C (Vss is used as the reference)	1.16	1.2	1.24		*10

Notes: 1. V_{SS} = 0V is assumed for every voltage indicated.

2. Voltages V_0, V_1, V_2, V_3 and V_4 must conform to the requirements that $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ as well as $V_{OUT} \geq V_0 \geq V_{SS}$.

3. Operating the LSI is operated beyond the maximum absolute rating can damage it permanently. In the normal operation, it is desirable to use the LSI in compliance with its electric characteristics. If the LSI is used under any conditions conflicting with its electric characteristics, not only its malfunctioning but also serious loss of reliability can result.

◊ Dynamic operating current (1) - When display is turned on with the built-in power supply being disconnected [Ta = 25°C and output under no-load].
Following shows current consumed by entire IC when external power supply is used.

Display: All-white

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=7.2V	–	23	48	µA	*11
	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=9.0V	–	25	50		

Display: Checker pattern

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=7.2V	–	26	54	µA	*11
	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=9.0V	–	29	57		

◊ Dynamic operating current (2) - When display is turned on with the built-in power supply being connected [Ta = 25°C and output under no-load].

Display: All-white

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	68	101	µA	*12
	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	79	112		

Display: Checker pattern

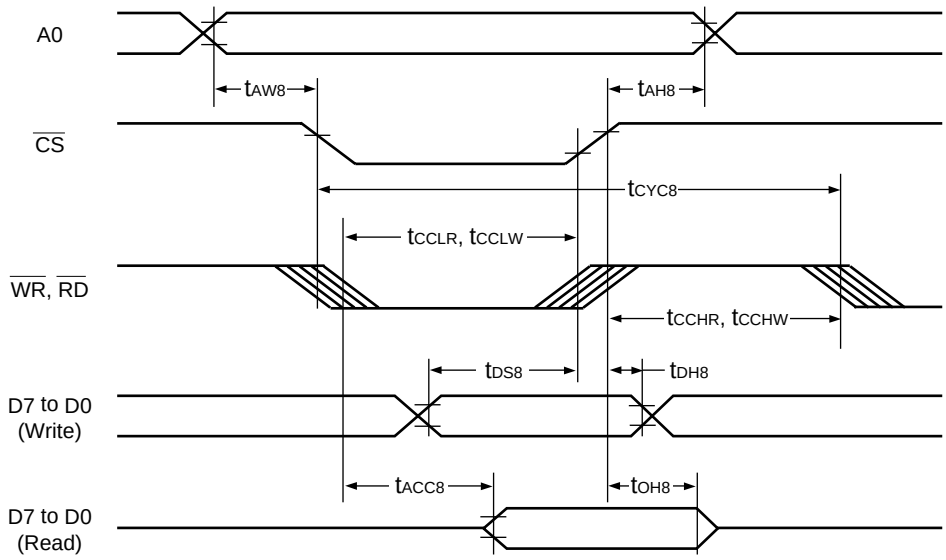
Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	75	103	µA	*12
	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	87	112		

◊ Current consumption in the power save mode [Ta = 25°C and output under no-load]

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(3)	V_{DD}=V_{DD2}=1.8~3.6V	–	0.01	5	µA	

■ AC CHARACTERISTICS

● System Bus Read/Write Characteristics 1 (For the 8080-series MPU)



[V_{DD}=2.7V~3.6V, Ta=–40~85°C]

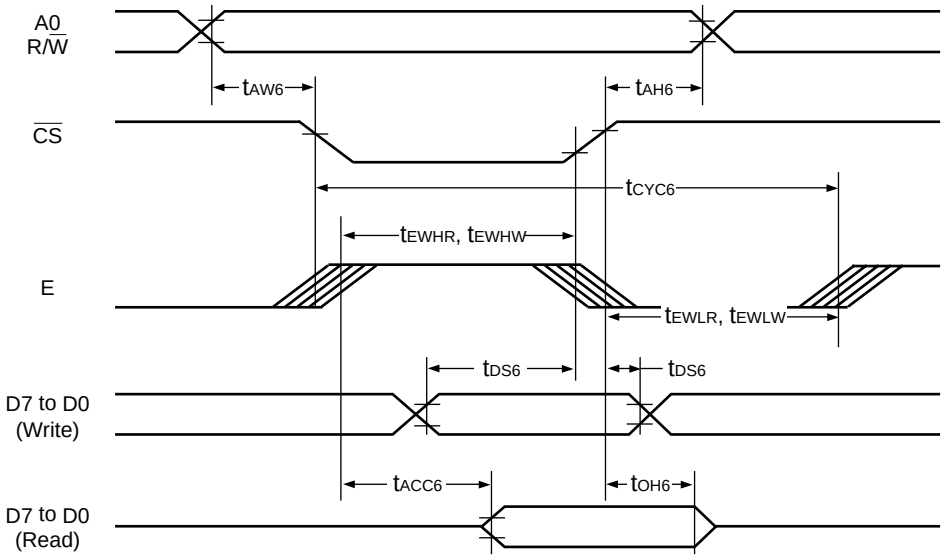
Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		500	–	
Control L pulse width($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		100	–	
Control L pulse width($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		200	–	
Control H pulse width($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		100	–	
Control H pulse width($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		100	–	
Data setup time	D7 to D0	t_{DS8}		70	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	180	
Output disable time		t_{OH8}		10	100	

[V_{DD}=1.8V~2.7V, Ta=–40~85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		1000	–	
Control L pulse width($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		150	–	
Control L pulse width($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		300	–	
Control H pulse width($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		150	–	
Control H pulse width($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		150	–	
Data setup time	D7~D0	t_{DS8}		120	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	260	
Output disable time		t_{OH8}		10	200	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. When the system cycle time is extremely fast, it is specified by (t_r, t_f) ≦ (t_{CYC8}-t_{CCLW}-t_{CCHW}) or (t_r, t_f) ≦ (t_{CYC8}-t_{CCLR}-t_{CCHR}).
*2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
*3. t_{CCLW} and t_{CCLR} are specified by the overlap period in which $\overline{CS}$ is “0” and $\overline{WR}$, $\overline{RD}$ are “0”.
*4. Timing of A0 is determined by the overlap period in which CS is “L” and $\overline{WR}$ and $\overline{RD}$ are “L”, too.

● **System Bus Read/Write Characteristics 2 (For the 6800-series MPU)**



[V_{DD}=2.7V~3.6V, Ta=–40~85°C]

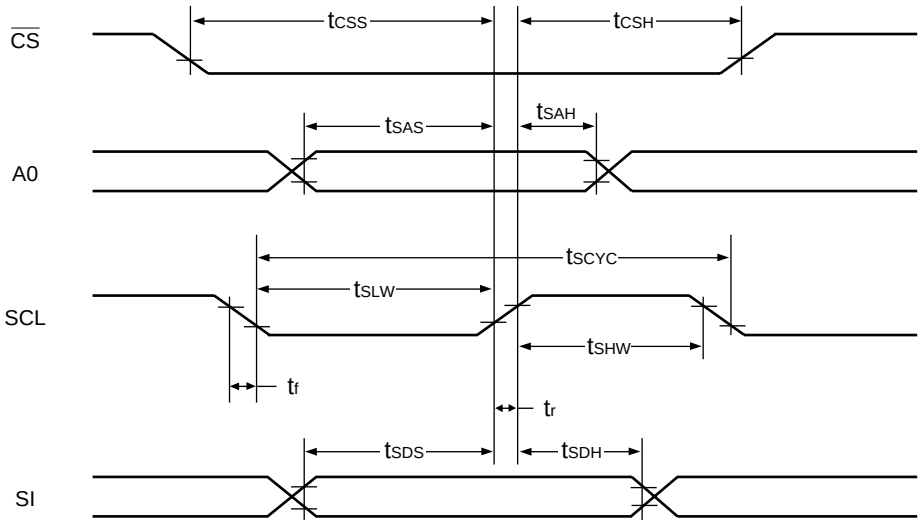
Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		WR	t_{AW6}		0	–	
System cycle time			t_{CYC6}		500	–	
Enable	width	E	t_{EWHW}		100	–	
high pulse width	Read		t_{EWHR}		200	–	
Enable	width		t_{EWLW}		100	–	
low pulse width	Read		t_{EWLR}		100	–	
Data setup time		D7~D0	t_{DS6}		70	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	180	
Output disable time			t_{OH6}		10	100	

[V_{DD}=1.8V~2.7V, Ta=–40~85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		WR	t_{AW6}		0	–	
System cycle time			t_{CYC6}		1000	–	
Enable	width	E	t_{EWHW}		150	–	
high pulse width	Read		t_{EWHR}		300	–	
Enable	width		t_{EWLW}		150	–	
low pulse width	Read		t_{EWLR}		150	–	
Data setup time		D7~D0	t_{DS6}		120	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	260	
Output disable time			t_{OH6}		10	200	

* 1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. When the system cycle time is extremely fast, it is specified by (t_r, t_f) ≥ (t_{CYC6}-t_{EWHW}-t_{EWLW}) or (t_r, t_f) ≥ (t_{CYC6}-t_{EWHR}-t_{EWLR}).
* 2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
* 3. t_{EWHW} and t_{EWHR} are specified by the overlap period in which CS is “0” and E is “1”.
* 4. Timing of A_0 is determined by the overlap period in which CS is “L” and E is “H”.

● **Serial interface**



[V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

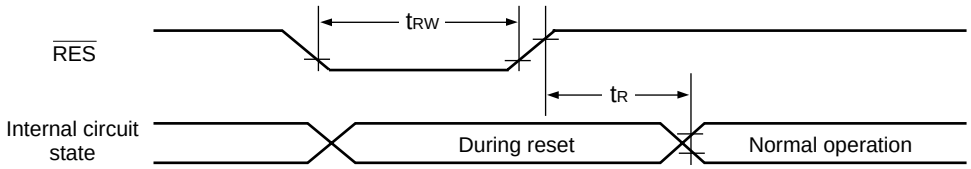
Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		125	–	ns
Serial clock H pulse width		t_{SHW}		50	–	
Serial clock L pulse width		t_{SLW}		50	–	
Address setup time	A0	t_{SAS}		75	–	
Address hold time		t_{SAH}		75	–	
Data setup time	SI	t_{SDS}		50	–	
Data hold time		t_{SDH}		50	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		75	–	
		t_{CSH}		75	–	

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		200	–	ns
Serial clock H pulse width		t_{SHW}		75	–	
Serial clock L pulse width		t_{SLW}		75	–	
Address setup time	A0	t_{SAS}		75	–	
Address hold time		t_{SAH}		75	–	
Data setup time	SI	t_{SDS}		50	–	
Data hold time		t_{SDH}		50	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		100	–	
		t_{CSH}		100	–	

Notes: 1. The input Signal rise and fall times must be with in 15ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

● Reset timing



[V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	1000	ns
Reset low pulse width	$\overline{RES}$	t_{RW}		1000	–	

[V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	1500	ns
Reset low pulse width	$\overline{RES}$	t_{RW}		1500	–	

Notes: 1. The input Signal rise and fall times must be with in 15ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

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