EPSON

SED1751

LCD Common Driver for MLS

■ DESCRIPTION

The 120-output, 3-value low-resistance common (low) driver SED1751 is designed to drive MLS (Multi Line Selection) for enabling high display quality and high-speed response.
Being used with the SED1580, it can drive 4-line MLS by receiving signals from the LCD controller SED1335/1351, etc.
The SED1751 can apply to a wide variety of application since its slim shape is advantageous for narrowing the LCD panel architecture and the logic system power supply can be operated with a low voltage.

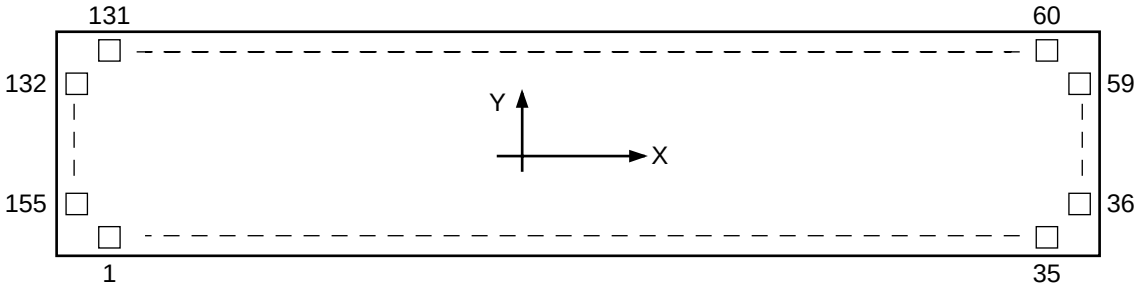
Its pad is designed to be easily mounted on a board and the driver output order can be selected in both directions, providing the highest driver operating performance for a 1/240 or 1/480 duty panel.

■ FEATURES

- Number of LCD drive outputs: 120
- Low voltage operation available: 2.7 V (min.)
- Output low On resistance
- High-duty driving available: 1/480 (reference)
- A wide range of liquid crystal drive voltage: +14 to +42 V (V_{CC} = 2.5 to 5.5 V)
- Output shift direction-pin selection.
- Number of outputs can be switched between 100 and 120.
- Non-bias display off function
- Logic system power supply: 2.7 V to 5.5 V
- Liquid crystal power supply offset bias for the V_{DDH} and GND levels can be adjusted.
- Slim chip
- Package: SED1751D0B ..... Au Bump Chip
  SED1751T0A ..... TCP

This product is not designed to resist radiation.

■ PAD LAYOUT



Chip size: 12.19 mm × 2.38 mm
Pad pitch: 80 μm (min.)
Chip thickness: 525 μm ± 25 μm

1) Au bump specifications (SED1751D0B) reference
Au vertical bump

	Scribe parallel	×	scribe vertical	±	tolerance	
Bump size A:	60 μm	×	75 μm	±	4 μm	(pad Nos. 1 to 35 and 60 to 131)
Bump size B:	80 μm	×	50 μm	±	4 μm	(pad Nos. 36 to 59 and 132 to 155)

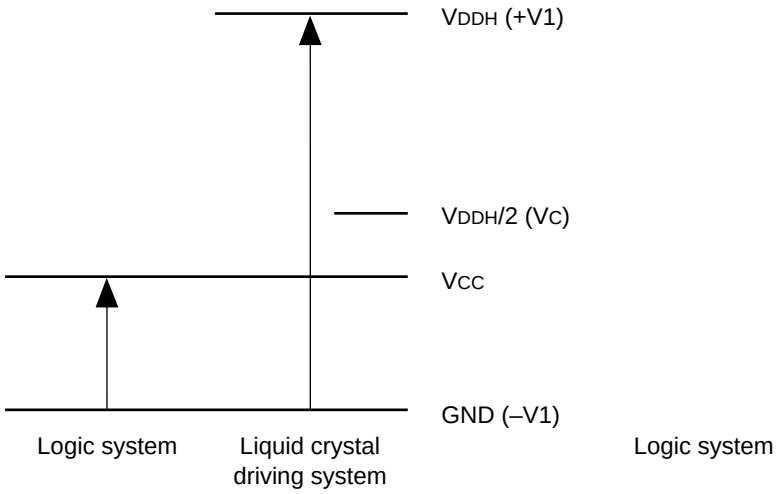
Bump height: 17 to 28 μm (refer to the delivery specifications for details)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	$\pm V_1$, V_C	GND –0.3 to V_{DDH} +0.3	V
Input voltage	V_I	GND –0.3 to V_{CC} +0.3	V
Output voltage	V_O	GND –0.3 to V_{CC} +0.3	V
CIO output current	I01	20	mA
Operating temperature	Topr	–30 to +85	°C
Storing temperature (1)	T_{stg1}	–65 to +150	°C
Storing temperature (2)	T_{stg2}	–55 to +100	°C

Notes

1. All voltages refer to GND as 0 V.
2. Storing temperature 1 applies to a situation of a single chip and 2 to a situation where TCP is mounted.
3. For voltages $+V_1$, V_C and $-V_1$, be sure to keep the condition of "$V_{DDH} \geq +V_1 \geq V_C \geq -V_1 \geq$ GND".



4. Never float the logic system power supply while the liquid crystal driving system power supply is turned on or allow Vcc to go under 2.6 V, otherwise, the LSI may permanently break. Pay special attention to the sequence for turning the system on and off.

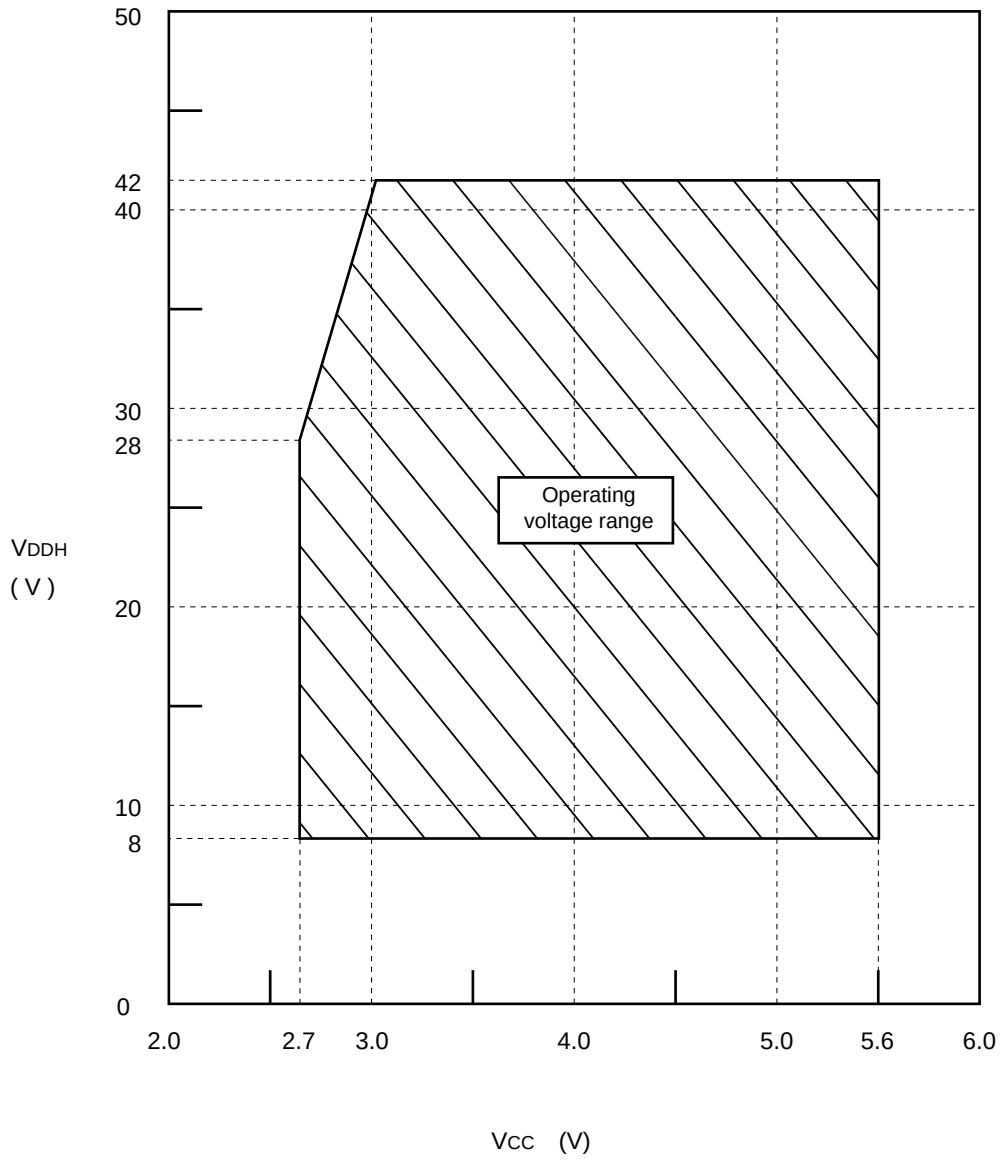
■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

GND = 0 V, V_{CC} = +5.0 V ± 10% and Ta = –30 to 85°C unless otherwise specified.

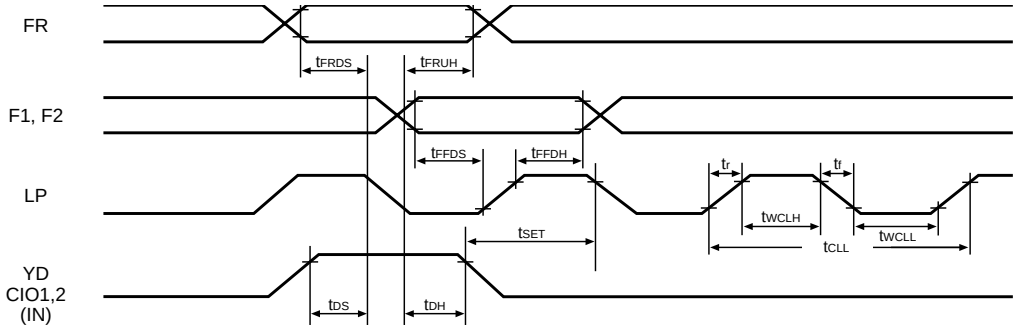
Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Units	Pin used
Supply voltage (1)	V_{CC}			2.7	5.0	5.5	V	V_{CC}
Operation enabling voltage	V_{DDH}	Operation enabled		8.0	—	42.0	V	V_{DDH}
Supply voltage (2)	$+V_1$	Recommended value		—	—	V_{DDH}	V	$+V_1$
Supply voltage (3)	V_C	Recommended value		—	$V_{DDH}/2$	—	V	V_C
Supply voltage (4)	$–V_1$	Recommended value		GND	—	—	V	$–V_1$
High-level input voltage	V_{IH}	V_{CC} = 2.7 to 5.5 V		0.8V_{CC}	—	—	V	CIO1, CIO2, FR, YD, LP, SHL, SEL, LSEL, CSEL, DOFF, F1, F2, TEST1
Low-level input voltage	V_{IL}			—	—	0.2V_{CC}	V	
High-level output voltage	V_{OH}	V_{CC} = 2.7 to 5.5 V	I_{OH} = –0.3 mA	V_{CC} – 0.4	—	—	V	CIO1, CIO2
Low-level output voltage	V_{OL}		I_{OL} = 0.3 mA	—	—	0.4	V	
Input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		—	—	2.0	µA	LP, YD, SHL, SEL, LSEL, CSEL, F1, F2, DOFF, TEST1, FR
I/O leakage current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		—	—	5.0	µA	CIO1, CIO2
Static current	I_{GND}	V_{DDH} = 14.0 to 42.0 V V_{IH} = V_{CC}, V_{IL} = GND		—	—	25	µA	GND
Output resistance	R_{COM}	ΔV_{ON} = 0.5 V Recommended condition	V_{DDH} = +30.0 V	—	0.55	0.7	kΩ	COM1 to COM120
			V_{DDH} = +40.0 V	—	0.5	0.7		
Average operating current consumption (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC} V_{IL} = GND, f_{LP} = 16.8 kHz f_{FR} = 70 Hz, Input data: 1/240, unloaded		—	10	25	µA	V_{CC}
		V_{CC} = 3.0 V Other conditions are the same as that in the case of V_{CC} = 5 V.		—	7	17		
Average operating current consumption (2)	I_{DDH}	V_{DDH} = $+V_1$ = +30.0 V V_C = $V_{DDH}/2$, $–V_1$ = 0.0 V V_{CC} = +5.0 V Other conditions are the same as that for I_{CC}.		—	6	13	µA	V_{DDH}
Input pin capacity	C_I	Freq. = 1 MHz, Ta = 25°C (for a single chip)		—	—	10	pF	LP, YD, SHL, SEL, LSEL, CSEL, F1, F2, DOFF, TEST1, FR
I/O pin capacity	$C_{I/O}$			—	—	18	pF	CIO1, CIO2

- **Operating voltage range: $V_{CC} – V_{DDH}$**
  The V_{DDH} voltage is required to be set within the $V_{CC} – V_{DDH}$ operating voltage range shown below.



● AC Characteristics

• Input Timing Characteristics



FR latched by “n”th LP is reflected on the output of “n + 1”th LP.

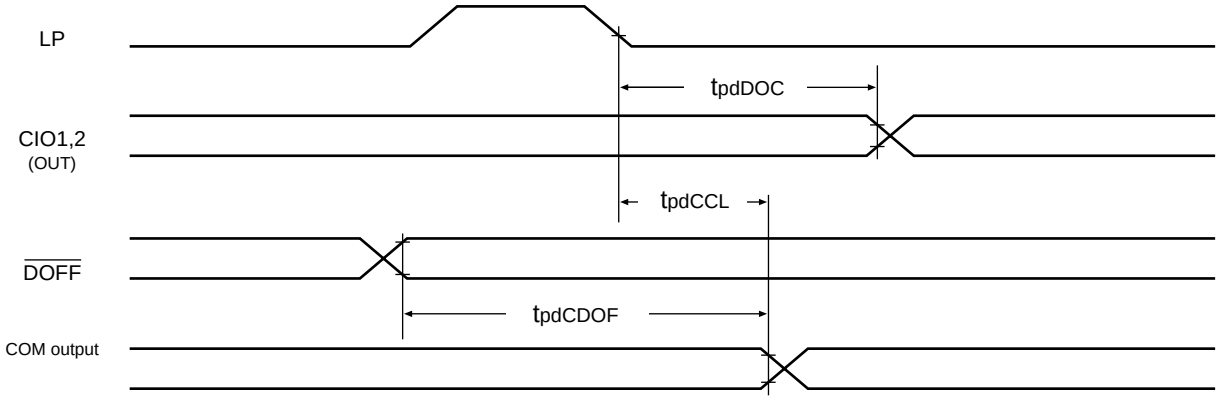
V_{CC} = +5.0 V ± 10%, Ta = –30 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
LP cycle	t_{CCL}	—	500	—	ns
LP high-level pulse width	t_{WCLH}	—	55	—	ns
LP low-level pulse width	t_{WCLL}	—	330	—	ns
FR setup time	t_{FRDS}	—	100	—	ns
FR hold time	t_{FRDH}	—	40	—	ns
F1/F2 setup time	t_{FFDS}	—	100	—	ns
F1/F2 hold time	t_{FFDH}	—	40	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns
CIO setup time	t_{DS}	—	100	—	ns
CIO hold time	t_{DH}	—	40	—	ns
YD to LP allowable time	t_{SET}	—	80	—	ns

V_{CC} = +2.7 V to 4.5 V, Ta = –30 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
LP cycle	t_{CCL}	—	800	—	ns
LP high-level pulse width	t_{WCLH}	—	100	—	ns
LP low-level pulse width	t_{WCLL}	—	660	—	ns
FR setup time	t_{FRDS}	—	200	—	ns
FR hold time	t_{FRDH}	—	80	—	ns
F1/F2 setup time	t_{FFDS}	—	200	—	ns
F1/F2 hold time	t_{FFDH}	—	80	—	ns
Input signal rise time	t_r	—	—	100	ns
Input signal fall time	t_f	—	—	100	ns
CIO setup time	t_{DS}	—	200	—	ns
CIO hold time	t_{DH}	—	80	—	ns
YD to LP allowable time	t_{SET}	—	150	—	ns

- **Output Timing Characteristics**



V_{CC} = +5.0 V ± 10%, V_{DDH} = +14.0 to +42.0 V, Ta = –30 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
LP to CIO output delay time	t_{pdDOC}	C_L = 15 pF	—	300	ns
LP to COM output delay time	t_{pdCCL}	V_{DDH} = 14.0 V to 40.0 V	—	350	ns
$\overline{DOFF}$ to COM output delay time	t_{pdCDOF}		—	700	ns

V_{CC} = +2.7 to 4.5 V, V_{DDH} = +14.0 to +28.0 V, Ta = –30 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
LP to CIO output delay time	t_{pdDOC}	C_L = 15 pF	—	600	ns
LP to COM output delay time	t_{pdCCL}	V_{DDH} = 14.0 V to 40.0 V	—	500	ns
$\overline{DOFF}$ to COM output delay time	t_{pdCDOF}		—	1400	ns

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