EPSON

SED1590 Series

LCD Segment Driver

■ DESCRIPTION

The segment (column) driver SED1590 having the built-in medium display capacity RAM enables low power demand and high display quality, which are required for handy equipment, and is used with the common (low) driver SED1751 and the power supply IC SCI7500.

This device can be directly connected to the micro processing unit (MPU) bus and is designed to store 8-bit parallel display data sent from the MPU in the built-in display RAM and generate liquid crystal drive signals independently of the MPU. The number of LCD drive outputs is 160 and it has a built-in display RAM of 160 outputs × 240 lines. Since one dot of the liquid crystal panel pixel corresponds to one dot of the built-in RAM (one-to-one correspondence), display of high degree of freedom can be achieved.

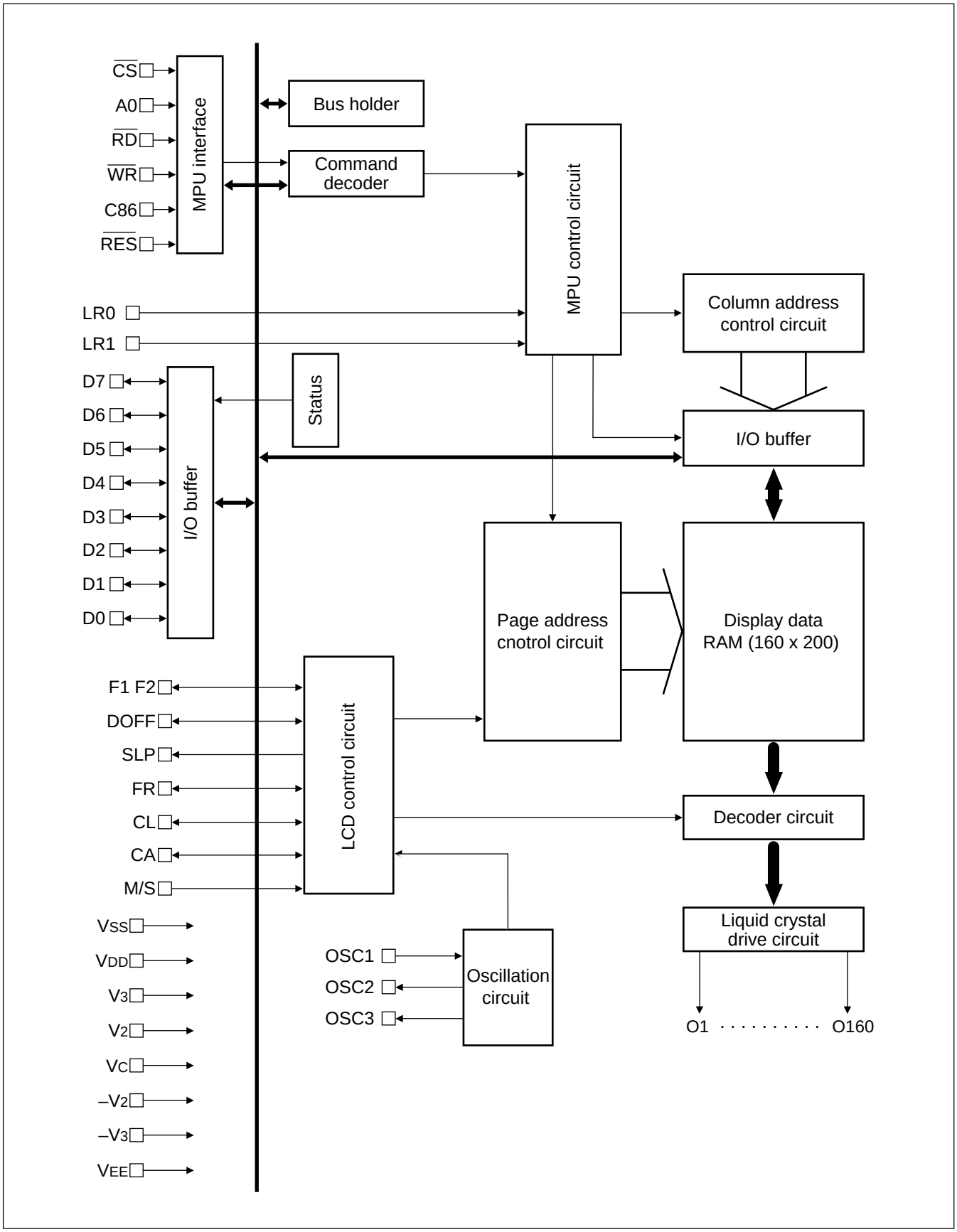
Writing into the built-in RAM from the MPU can be conducted with the minimum power demand since no external operation clock is required. In addition, the MPU need not distinguish several chips even when more than one SED1590s are used since the single chip selection function is available.

The SED1590 can apply to a wide variety of application since its slim shape is advantageous for narrowing the LCD panel architecture and the logic system power supply can be operated with a low voltage.

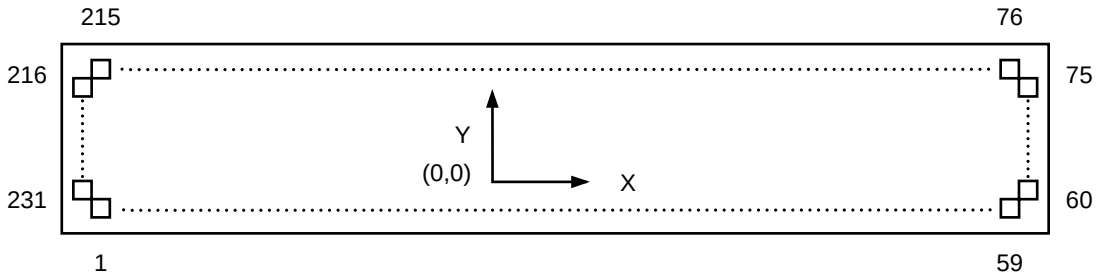
■ FEATURES

- Number of LCD drive outputs: 160
- Drive duty ratio (max.): 1/240 duty
- RAM data direct display using display data RAM
  RAM bit data: 0 = Off, 1 = On (at normal display)
- Built-in display RAM capacity: 160 × 240 bits
- 8-bit MPU interface
  Directly connectable to both 80- and 68-series MPUs.
- Single chip selection function available when several chips are used.
- Various command functions
- Ultra-low current consumption
- Power supply
  Logic system: 2.7 to 3.6 V
  LCD system: 5.4 to 7.2 V
- Non-bias display off function
- Slim chip
- Package: SED1590D0B ..... Au Bump Chip
  SED1590T0A ..... TCP
- This product is not designed to resist radiation or light.

■ BLOCK DIAGRAM



■ PAD LAYOUT



Chip size: 14.82 mm × 2.50 mm
Bump size: 67 μm × 80 μm (min.)
Bump pitch: 100 μm (min.)
Bump height: 22.5 ± 5.5 μm

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_{EE}	–8.0 to +0.3	V
Supply voltage (3)	V_3, V_2, V_C, $-V_2$, $-V_3$	V_{EE} to +0.3	V
Input voltage	V_{IN}	V_{SS} –0.3 to +0.3	V
Output voltage	V_{OUT}	V_{SS} –0.3 to +0.3	V
Operating temperature	Topr	–20 to +85	°C
Storing temperature (1)	T_{stg1}	–65 to +150	°C
Storing temperature (2)	T_{stg2}	–55 to +100	°C

Notes

1. All voltages refer to V_{DD} as 0 V.
2. Storing temperature (1) applies to a bare chip or plastic package product and (2) to when TCP is mounted.
3. For voltages V_3, V_2, V_C, $-V_2$ and $-V_3$, be sure to keep the condition of "$V_{DD} \geq V_3 > V_2 > V_C > -V_2 > -V_3 \geq V_{EE}$".
4. If the LSI is used outside the absolute maximum ratings, it may permanently break. Use under the electrical characteristics conditions is recommended for normal operation, otherwise, the LSI may malfunction, disadvantageously affecting its reliability.

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

V_{DD} = V_3 = 0 V, V_{SS} = –3.0 V, V_{EE} = –V_3 = –6.0 V, V_2 = –1.5 V, V_C = –3.0 V, –V_2 = –4.5 V and Ta = –20 to 85°C unless otherwise specified.

Parameter	Symbol	Condition	Rating			Units	Pin used
			Min.	Typ.	Max.		
Supply voltage (1)	V_{SS}		–3.6	–3.0	–2.7	V	V_{SS}
Supply voltage (2)	V_{EE}		–7.2	–6.0	–5.4	V	V_{EE}
Supply voltage (3)	V_3		—	—	V_{DD}	V	V_3
Supply voltage (4)	V_2		—	0.25V_{EE}	—	V	V_2
Supply voltage (5)	V_C		—	0.50V_{EE}	—	V	V_C
Supply voltage (6)	–V_2		—	0.75V_{EE}	—	V	–V_2
Supply voltage (7)	–V_3		V_{EE}	—	—	V	–V_3
High-level input voltage	V_{IHC}		0.3V_{SS}	—	V_{DD}	V	*1
Low-level input voltage	V_{ILC}		V_{SS}	—	0.7V_{SS}	V	*1
High-level output voltage	V_{OH}	I_{OH} = –0.6 mA	V_{DD} – 0.4	—	V_{DD}	V	*2
Low-level output voltage	V_{OL}	I_{OL} = +0.6 mA	V_{SS}	—	V_{SS} + 0.4	V	*2
Schmitt high-level input voltage	V_{IHS}		0.3V_{SS}	—	V_{DD}	V	$\overline{RES}$
Schmitt low-level input voltage	V_{ILS}		V_{SS}	—	0.7V_{SS}	V	$\overline{RES}$
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	—	—	5.0	µA	*3
I/O leakage current	$I_{LI/O}$	V_{IN} = V_{DD}, V_{SS}	—	—	5.0	µA	*4
Driver output resistance	R_{ON}	V_{SS} = –3.0 V, V_{EE} = –6.0 V V_3 = 0 V, V_2 = –1.5 V V_C = –3.0 V, –V_2 = –4.5 V –V_3 = –6.0 V, ΔV = 0.5 V	—	0.6	1.0	kΩ	O1 to O160
Static current consumption	I_{SSQ}	V_{IN} = V_{DD} or V_{SS}	—	—	5	µA	V_{SS}
Static current consumption	I_{EEQ}	V_{EE} = –6.0 V	—	—	5	µA	V_{EE}
Dynamic current consumption	I_{SSOP1}	MPU access *6	—	1.5	2.0	mA	V_{SS}
Dynamic current consumption	I_{SSOP2}	MPU no access *6	—	90	130	µA	V_{SS}
Dynamic current consumption	I_{EEOP}	V_{EE} = –6.0 V	—	12	20	µA	V_{EE}
Input pin capacity	C_I	Freq. = 1 MHz, Ta = 25°C	—	—	8	pF	*3
I/O pin capacity	$C_{I/O}$	(for a single chip)	—	—	15	pF	*4
Output pin capacity	C_O		—	—	7	pF	$\overline{SLP}$
Oscillating frequency	f_{OSC}	Ta = 25°C	—	24	—	kHz	*5

Supplementary explanation on DC characteristics

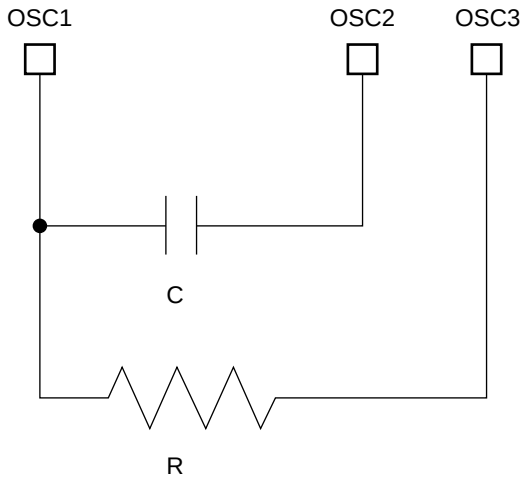
*1 • Input pins of A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, C86, OSC1, M/S, LR0 and LR1.
• I/O pins (in input mode) of Ds 0 to 7, CL, FR, CA, $\overline{DOFF}$, $\overline{SLP}$, F1 and F2.

*2 • I/O pins (in output mode) of Ds0 to 7, CL, FR, CA, $\overline{DOFF}$, F1 and F2.
• Output pins of OSC2, OSC3 and $\overline{SLP}$.

*3 • Input pins of A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, C86, OSC1, M/S, LR0 and LR1.

*4 • I/O pins (in input mode) of Ds0 to 7, CL, FR, CA, $\overline{DOFF}$, $\overline{SLP}$, F1 and F2.

*5 • Local oscillation circuit using CR



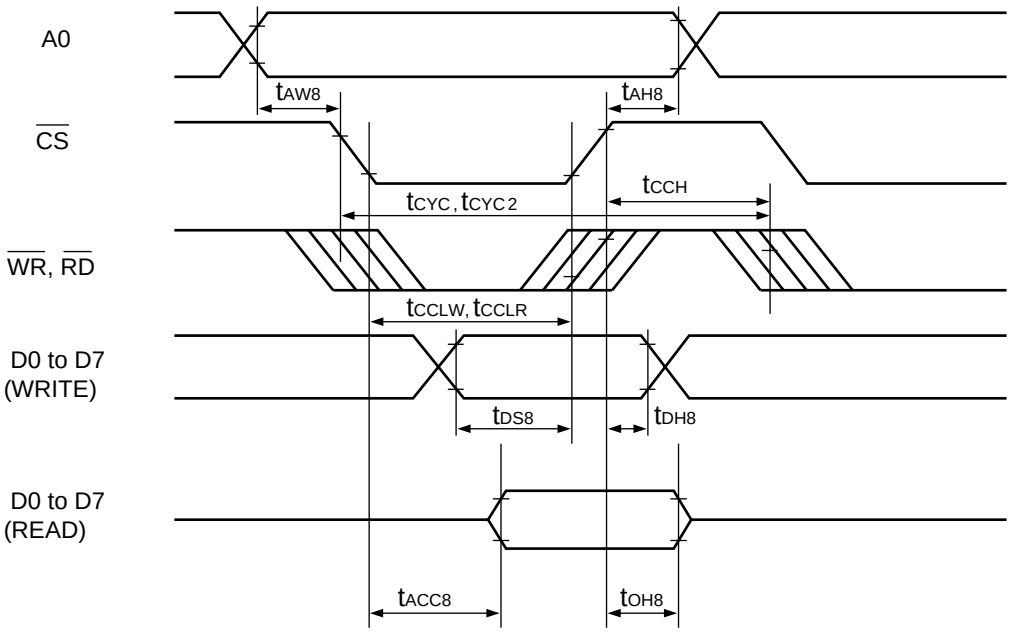
Oscillating frequency: f ≒ 1/(2.2CR)

*6 • Frame frequency of 60 Hz, duty of 1/200 and CR oscillation of 24 kHz are used by 2 dividing.
• C = 100 pF and R of CR oscillation is adjusted to 24 kHz by variable resistance.
• MPU access is in a cycle time of 1,333 ns (750 kHz) and display data is consecutively written.
• Display data repeats black and white every 4 lines.

● AC Characteristics

• System bus

Read/write characteristics I (80-series MPU)



(Ta = –20 to 85°C, V_{SS} = –3.0 to –3.6 V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions, etc.
A0	t_{AH8}	Address hold time	5	—	ns	—
	t_{AW8}	Address setup time	5	—	ns	
$\overline{WR}$, $\overline{RD}$	t_{CYC}	Write cycle	1300	—	ns	—
	t_{CYC2}	Read cycle (status read/output port read)	300	—	ns	
	t_{CCH}	Control pulse H width	600	—	ns	
	t_{CCLW}	Control pulse L width ($\overline{WR}$)	50	—	ns	
	t_{CCLR}	Control pulse L width ($\overline{RD}$)	140	—	ns	
D0 to D7	t_{DS8}	Data setup time	35	—	ns	
	t_{DH8}	Data hold time	5	—	ns	
	t_{ACC8}	Read access time	—	140	ns	C_L = 100 pF
	t_{OH8}	Output disable time	30	90	ns	

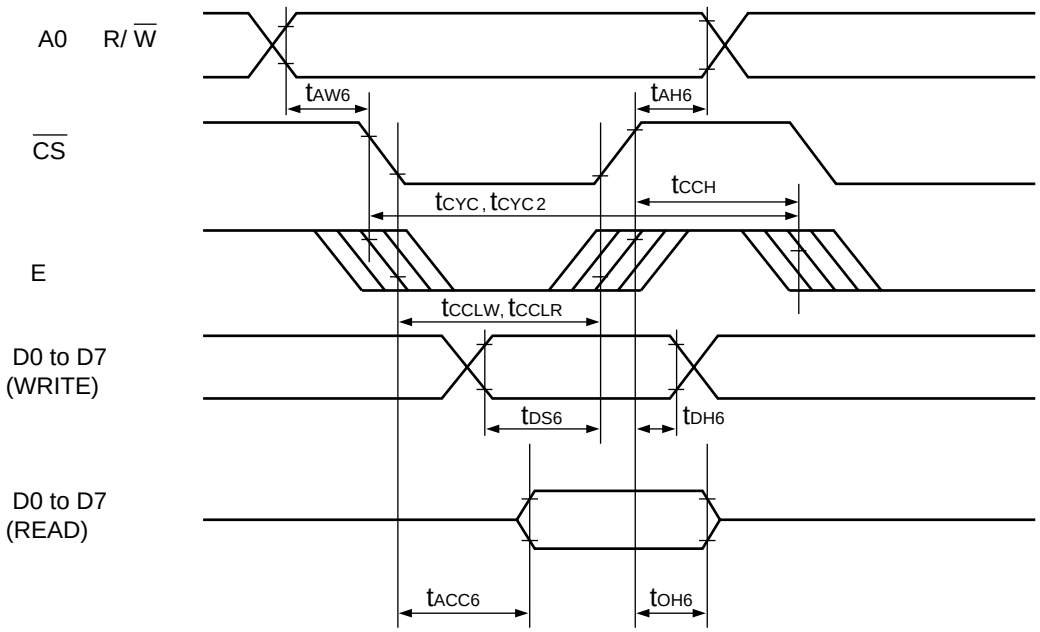
- The input signal rise and fall times (t_r and t_f) are specified at 15 ns or lower.
- All timings are specified by referring to 20% and 80% of V_{DD} – V_{SS}.
- t_{CCLW} and t_{CCLR} are specified by the overlap period when $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ are at “L” level.
- These specifications only guarantee writing of display data into the RAM, output port and status reading.

(Ta = –20 to 85°C, V_{SS} = –2.7 to –3.0 V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions, etc.
A0	t_{AH8}	Address hold time	5	—	ns	—
	t_{AW8}	Address setup time	5	—	ns	
$\overline{WR}$, $\overline{RD}$	t_{CYC}	Write cycle	1600	—	ns	—
	t_{CYC2}	Read cycle (status read/output port read)	350	—	ns	
	t_{CCH}	Control pulse H width	900	—	ns	
	t_{CCLW}	Control pulse L width ($\overline{WR}$)	70	—	ns	
	t_{CCLR}	Control pulse L width ($\overline{RD}$)	160	—	ns	
D0 to D7	t_{DS8}	Data setup time	50	—	ns	
	t_{DH8}	Data hold time	5	—	ns	
	t_{ACC8}	Read access time	—	160	ns	C_L = 100 pF
	t_{OH8}	Output disable time	40	110	ns	

- The input signal rise and fall times (t_r and t_f) are specified at 15 ns or lower.
- All timings are specified by referring to 20% and 80% of V_{DD} – V_{SS}.
- t_{CCLW} and t_{CCLR} are specified by the overlap period when $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ are at "L" level.
- These specifications only guarantee writing of display data into the RAM, output port and status reading.

- **Read/write characteristics II (68-series MPU)**



(Ta = –20 to 85°C, V_{SS} = –3.0 to –3.6 V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions, etc.
A0, R/$\overline{W}$	t_{AH6}	Address hold time	5	—	ns	—
	t_{AW6}	Address setup time	5	—	ns	
E	t_{CYC}	Write cycle	1300	—	ns	—
	t_{CYC2}	Read cycle (status read/output port read)	300	—	ns	
	t_{CCH}	Control pulse H width	600	—	ns	
	t_{CCLW}	Control pulse L width ($\overline{WR}$)	50	—	ns	
	t_{CCLR}	Control pulse L width ($\overline{RD}$)	140	—	ns	
D0 to D7	t_{DS6}	Data setup time	35	—	ns	
	t_{DH6}	Data hold time	5	—	ns	
	t_{ACC6}	Read access time	—	140	ns	C_L = 100 pF
	t_{OH6}	Output disable time	30	90	ns	

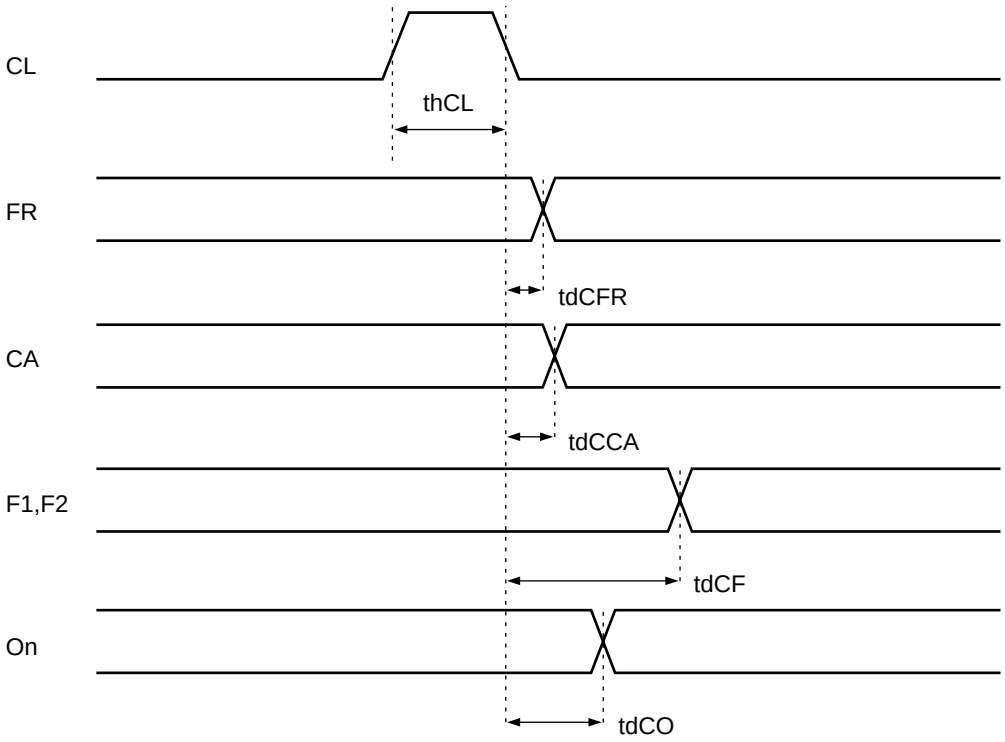
- The input signal rise and fall times (t_r and t_f) are specified at 15 ns or lower.
- All timings are specified by referring to 20% and 80% of V_{DD} – V_{SS}.
- t_{CCLW} and t_{CCLR} are specified by the overlap period when $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ are at "L" level.
- These specifications only guarantee writing of display data into the RAM, output port and status reading.

(Ta = –20 to 85°C, V_{SS} = –2.7 to –3.0 V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions, etc.
A0, R/$\overline{W}$	t_{AH6}	Address hold time	5	—	ns	—
	t_{AW6}	Address setup time	5	—	ns	
E	t_{CYC}	Write cycle	1600	—	ns	—
	t_{CYC2}	Read cycle (status read/output port read)	350	—	ns	
	t_{CCH}	Control pulse H width	900	—	ns	
	t_{CCLW}	Control pulse L width ($\overline{WR}$)	70	—	ns	
	t_{CCLR}	Control pulse L width ($\overline{RD}$)	160	—	ns	
D0 to D7	t_{DS6}	Data setup time	50	—	ns	
	t_{DH6}	Data hold time	5	—	ns	
	t_{ACC6}	Read access time	—	160	ns	C_L = 100 pF
	t_{OH6}	Output disable time	40	110	ns	

- The input signal rise and fall times (t_r and t_f) are specified at 15 ns or lower.
- All timings are specified by referring to 20% and 80% of V_{DD} – V_{SS}.
- t_{CCLW} and t_{CCLR} are specified by the overlap period when $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ are at "L" level.
- These specifications only guarantee writing of display data into the RAM, output port and status reading.

- **Output timing characteristics**



(Ta = –20 to 85°C, V_{SS} = –2.7 to –3.6 V)

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Measuring conditions
CL	t_{hCL}	CL pulse width	100	—	1000	ns	C_L = 100 pF
FR	t_{dCFR}	FR output delay	10	—	1000	ns	
CA	t_{dCCA}	CA output delay	10	—	1000	ns	
F1, F2	t_{dCF}	F1/F2 output delay	10	—	1000	ns	
On	t_{dCO}	On output delay	—	—	500	ns	

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