

# S1R72900F00A

## IEEE1394 PHY LSI

Preliminary

- IEEE1394-1995, 1394a-2000 compliant
- 400Mbps high-speed transfer supported
- 2 port

### ■ DESCRIPTION

The S1R72900F00A is an IEEE 1394-1995 Standard and the IEEE 1394a-2000 Standard compliant physical layer.

The S1R72900F00A has two 1394 ports and supports transfer speeds of 400/200/100 Mbit/sec. It incorporates a 400 MHz PLL, a reference voltage generation circuit, a high-speed transceiver, a LINK layer interface, and a state machine circuit for a bus initialization and arbitration functions.

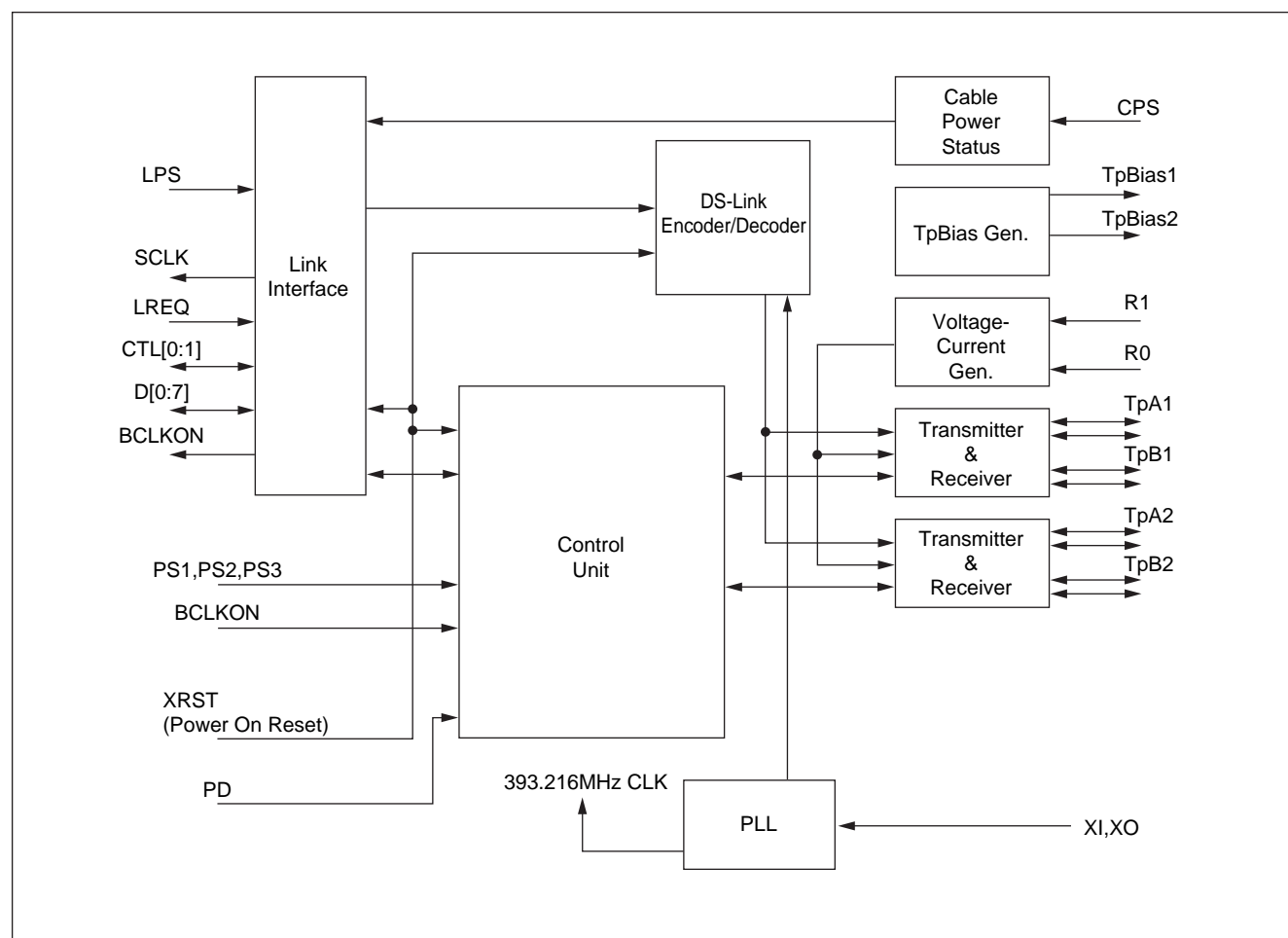
Making combination with our LINK layer S1R72801F00A, High speed 1394 transfer system can be easily realized.

### ■ FEATURES

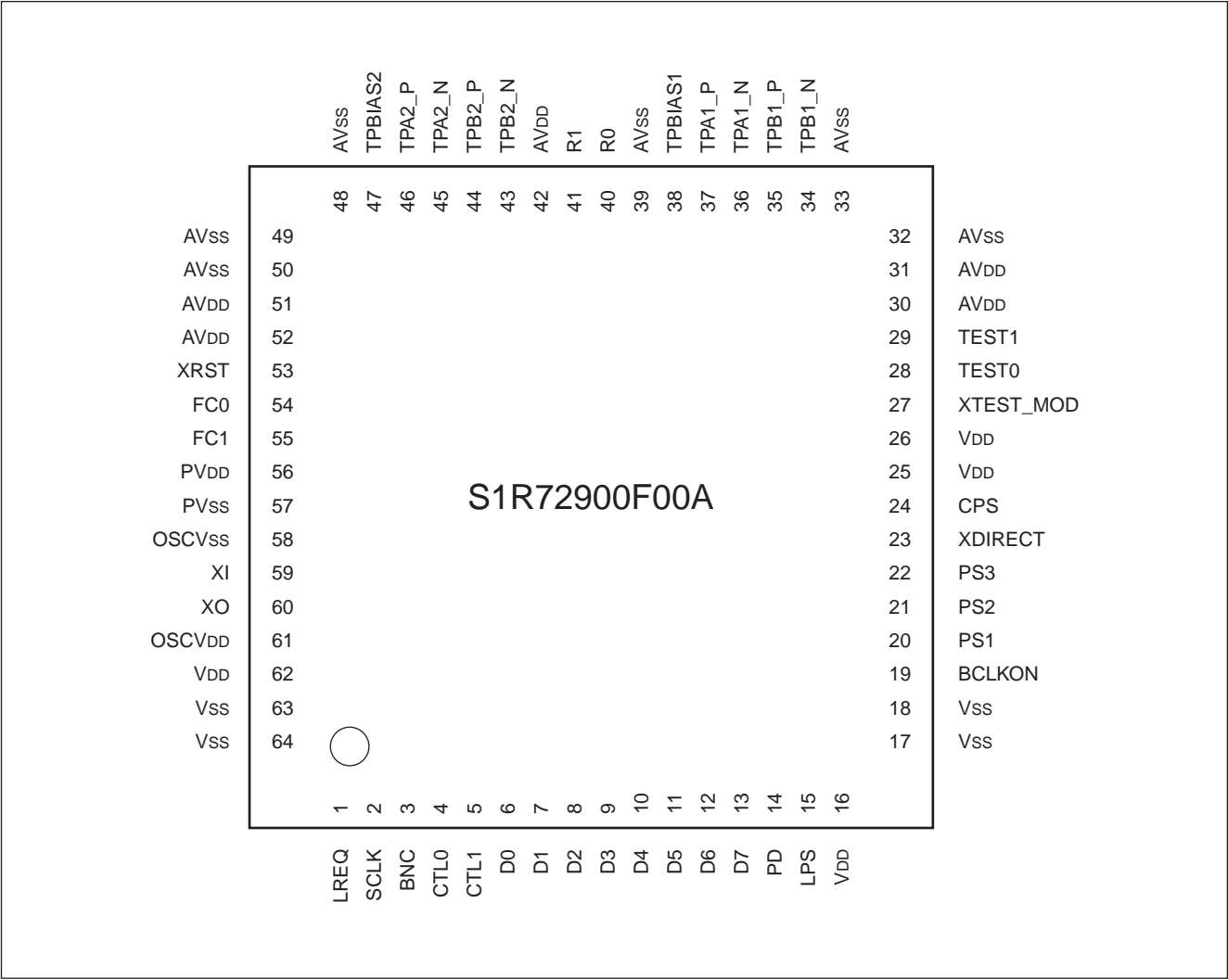
- IEEE 1394-1995 Standard and IEEE 1394a-2000 Standard compliant
- Transfer speeds of S400 (393.216 Mbit/sec), S200 (196.608 Mbit/sec) and S100 (98.304 Mbit/sec) are supported.
- Incorporates on-chip 400 MHz PLL that enables data transmissions of S400/S200/S100 and SCLK output at 50 MHz.
- Independent TpBias output for each port
- The Cable Power Status function which detects decline in cable power supply is supported.
- Built-in PHY/LINK interface circuit.
- Both DC and AC PHY/LINK interface connection are supported.
- A oscillation circuit is built in.
- High-precision, small-amplitude-differential, high-speed transceiver
- Control state machine circuit for bus initialization, arbitration and port connection
- High-speed DS encoder
- 3.3 V single power supply
- Plastic QFP 13-64 pin
- Low power CMOS technology
- The S1R72900F00A is not designed to be radiation-proof.

# S1R72900F00A

## ■ BLOCK DIAGRAM



PIN ARRANGEMENT



# S1R72900F00A

## ■ PIN DESCRIPTION

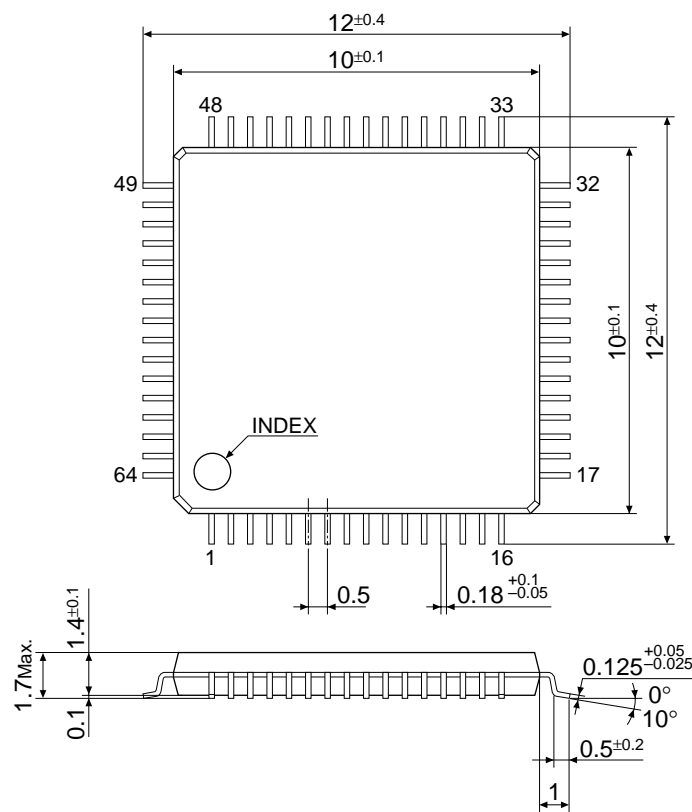
Pin Name	Function	Pin No.	Pin Type	I/O
AVDD	Analog circuit power supply pin	30,31,42,51,52	Supply	–
AVss	Analog circuit ground pin	32,33,39,48,49,50	Supply	–
PVDD	PLL circuit power supply pin	56	Supply	–
PVss	PLL circuit ground pin	57	Supply	–
VDD	Digital circuit power supply pin	16,25,26,62	Supply	–
Vss	Digital circuit ground pin	17,18,63,64	Supply	–
OSCVDD	Oscillation circuit power supply pin	61	Supply	–
OSCVss	Oscillation circuit ground pin	58	Supply	–
TPA1_P	Port 1, TPA + input/output signal	37	Differential	I/O
TPA1_N	Port 1, TPA - input/output signal	36	Differential	I/O
TPB1_P	Port 1, TPB + input/output signal	35	Differential	I/O
TPB1_N	Port 1, TPB - input/output signal	34	Differential	I/O
TPBIAS1	Port 1, TP bias voltage supply pin	38	Supply	O
TPA2_P	Port 2, TPA + input/output signal	46	Differential	I/O
TPA2_N	Port 2, TPA - input/output signal	45	Differential	I/O
TPB2_P	Port 2, TPB + input/output signal	44	Differential	I/O
TPB2_N	Port 2, TPB - input/output signal	43	Differential	I/O
TPBIAS2	Port 2, TP bias voltage supply pin	47	Supply	O
R1, R0	6.0k $\Omega$ ( $\pm 1.0\%$ ) external basic resistance connection pin	41,40	Analog	O
PD	Test pin Connect it to Vss in normal operation.	14	Hysteresis	I
BCLKON	Bus Manager Contender / LINK-On Pin On hardware resetting, whether or not the bus manager function is employed is decided by the condition of this pin. On receiving the LINK-On packet, this signal is used to make the LINK layer controller IC active.	19	CMOS	I/O
LREQ	Request signal from the LINK layer controller IC	1	Hysteresis	I
CTL0, CTL1	LINK interface interactive control signal	4,5	Hysteresis	I/O
D0 to D7	LINK interface interactive data signal	6,7,8,9,10,11,12,13	Hysteresis	I/O
SCLK	49.152 MHz system clock to the LINK layer controller IC	2		O
LPS	LINK power status pin This signal monitors whether the LINK layer controller IC is active or not.	15	Hysteresis	I
PS1 PS2 PS3	Power Status pin These pins set the power class bit of the Self-ID packet. PS1, PS2 and PS3 correspond to bits 21, 22 and 23 of the Self_ID packet.	20,21,22	CMOS	I
XDIRECT	This signal selects either DC or AC connection depending on whether or not the isolation barrier exists between PHY and LINK. Connect this pin to Vss for DC connection, and to VDD for AC connection.	23	CMOS	I
XTEST_MODE	Test pin Connect this pin to VDD in normal operation.	27	CMOS	I
XRST	Reset pin This pin initializes S1R72900F00A when '0'. Set it to '1' in normal operation.	53	Hysteresis	I
CPS	Cable Power Status detection pin Connect this pin to the cable power via the 240 k $\Omega$ resistance.	24	Hysteresis	I

Pin Name	Function	Pin No.	Pin Type	I/O
BNC	This signal indicates the cable condition. It outputs HIGH when all ports do not receive the bias voltage from the matched node.	3	CMOS	O
FC0	Filter connection pin for PLL S1R72900F00A does not require an external capacitor. Do not connect anything to this pin.	54	Analog	O
FC1	Filter connection pin for PLL S1R72900F00A does not require an external capacitor. Do not connect anything to this pin.	55	Analog	O
XI	Crystal oscillator 24.576 MHz input	59		
XO	Crystal oscillator 24.576 MHz input	60		
TEST0	Test pin Connect it to Vss in normal operation.	28	CMOS	I
TEST1	Test pin Connect it to Vss in normal operation.	29	CMOS	I

# S1R72900F00A

## DIMENSIONAL OUTLINE DRAWING

Plastic QFP13-64 pin (S1R72900F00A)



unit:mm

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# S1R72900F00A

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