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DESCRIPTION

The SLV series of transient voltage suppressors are designed to protect low voltage semiconductor components which are connected to data and transmission lines from transients caused by electrostatic discharge (ESD), lightning and other induced voltage surges.

The devices are constructed using Semtech's proprietary EPD process technology. The EPD process provides low standoff voltages with significant reductions in leakage currents and capacitance over silicon avalanche diode processes. The SLV series is specifically designed for protecting low voltage components such as microprocessors, ASICs, I/O transceivers, and high speed RAM. They provide ESD and latch-up protection for power and I/O ports, microprocessor bus interfaces, high speed data and video transmission lines, and low power portable and wireless systems.

The SLV series TVS diodes will meet the surge requirements of IEC 1000-4-2, Level 4, "Human Body Model" for air and contact discharge.

The low clamping voltage of the SLV minimizes the stress on the protected transceiver. The SO-8 package allows flexibility in the design of "crowded" circuit boards.

ORDERING INFORMATION

Part Number	Working Voltage	Qty per Reel	Reel Size
SLVDA2.8.TB	2.8V	500	7"
SLVDA3.3.TB	3.3V	500	7"

Note:
(1) Consult factory for the availability of 13" reels

FEATURES

- 300 watts peak pulse power (tp = 8/20µs)
- Transient protection for data lines to
  IEC 1000-4-2 (ESD) 15kV (air), 8kV (contact)
  IEC 1000-4-4 (EFT) 40A (tp = 5/50ns)
  IEC 1000-4-5 (Lightning) 12A (tp = 1.2/50µs)
- Protects up to four bidirectional lines
- Working Voltages: 2.8V & 3.3V
- Low leakage current for low power applications
- Low operating voltage ideal for latch-up protection
- Low capacitance
- Low clamping voltage
- Solid-state technology

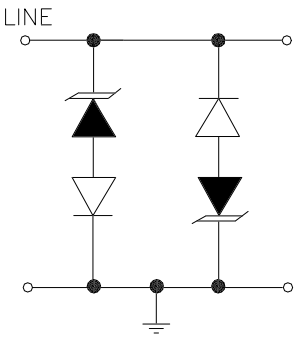
MECHANICAL CHARACTERISTICS

- JEDEC SO-8 package
- Molding compound flammability rating: UL 94V-0
- Marking : Part number, logo, date code
- Packaging : Tape and Reel per EIA 481

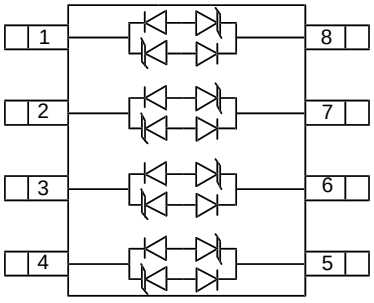
APPLICATIONS

- ESD and Latch-Up Protection
- Portable Electronics
- WAN/LAN Equipment
- Low Voltage ASICs
- Instrumentation
- Low Power Systems

CIRCUIT DIAGRAM (EACH LINE)



SCHEMATIC & PIN CONFIGURATION



SO-8 (Top View)

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20µs)	P_{pk}	300	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	24	A
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless Specified, T_A = 25°C)

SLVDA2.8

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				2.8	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2µA	3.0			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 2.8V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs			4.1	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs			5.3	V
Maximum Peak Pulse Current	I_{PP}	tp = 8/20µs			24	A
Junction Capacitance	C_j	Between I/O pins and Gnd V_R = 0V, f = 1MHz			100	pF

SLVDA3.3

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				3.3	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2µA	3.5			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs			4.5	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs			5.9	V
Maximum Peak Pulse Current	I_{PP}	tp = 8/20µs			17	A
Junction Capacitance	C_j	Between I/O pins and Gnd V_R = 0V, f = 1MHz			100	pF

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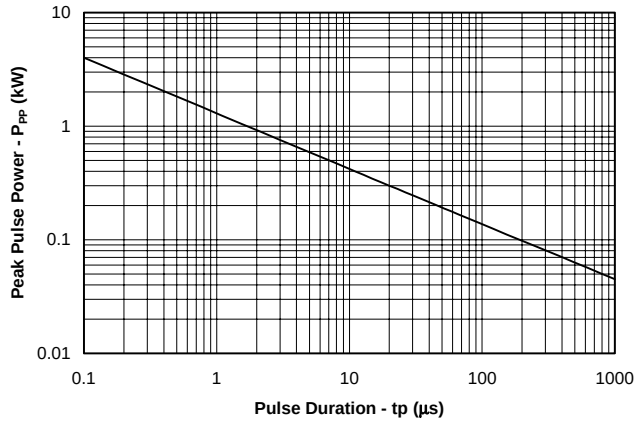
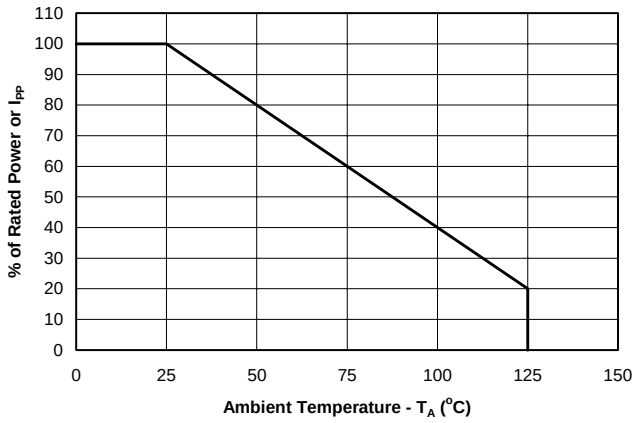
TYPICAL CHARACTERISTICS

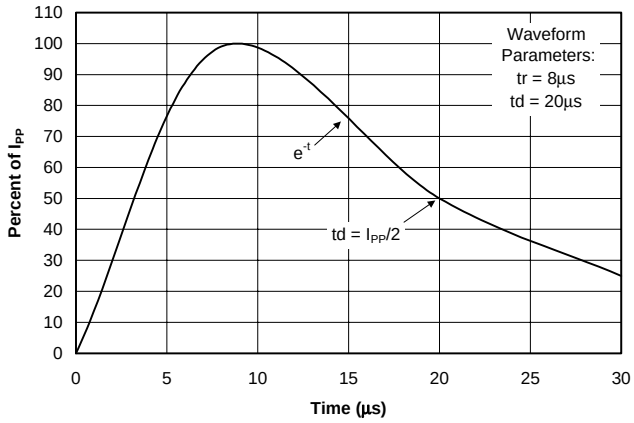
Non-Repetitive Peak Pulse Power vs. Pulse Time



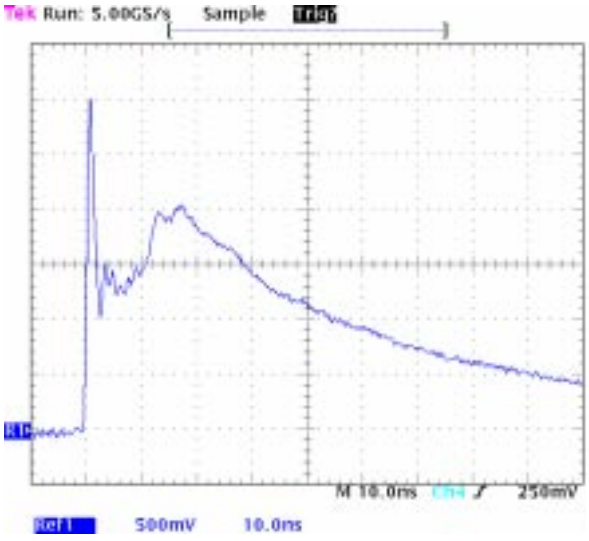
Power Derating Curve



Pulse Waveform



ESD Pulse Waveform (Per IEC 1000-4-2)



IEC 1000-4-2 Discharge Parameters

Level	First Peak Current (A)	Peak Current at 30ns (A)	Peak Current at 60ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

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APPLICATIONS INFORMATION

Device Connection for Protection of Four Data Lines

The SLVDA series devices are designed to protect up to four data lines. The devices are connected as follows:

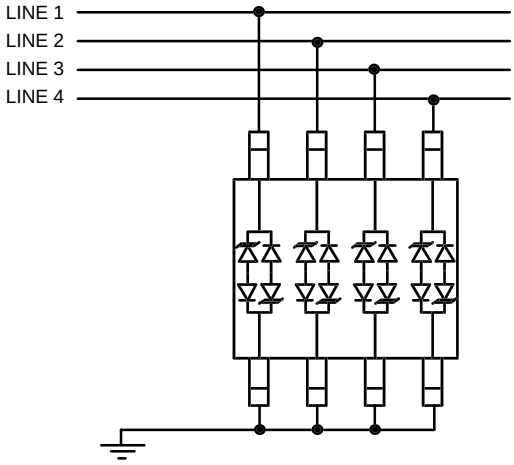
- Common mode protection of four data lines is achieved by connecting data lines at pins 1 - 4. Pins 5 - 8 are connected to ground (Device is symmetrical so connections may be reversed to serve a specific application). The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.
- Protecting 5V lines: The designer may take advantage of the superior reverse leakage and capacitance characteristics of the SLVDA2.8 to protect two 5V lines. This is achieved by connecting two lines of the device in series as shown. The series connection is made by shorting pins 5 & 6 together for the first line and pins 7 & 8 for the second line. Pins 1 & 4 are connected to the lines that are to be protected. Pins 2 & 3 are connected to ground. See application note SI96-14 for additional details.

Circuit Board Layout Recommendations for Suppression of ESD.

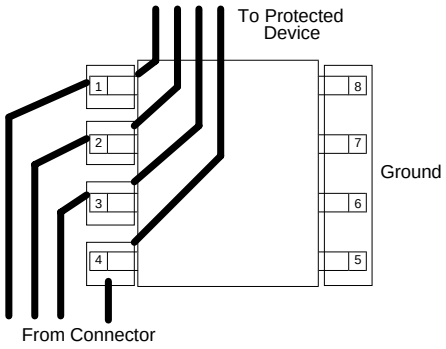
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

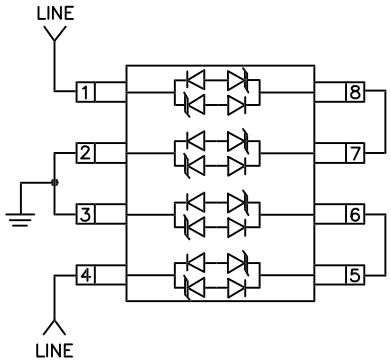
I/O Line Protection



Typical Connection



Optional Connection for Protecting 5V Lines



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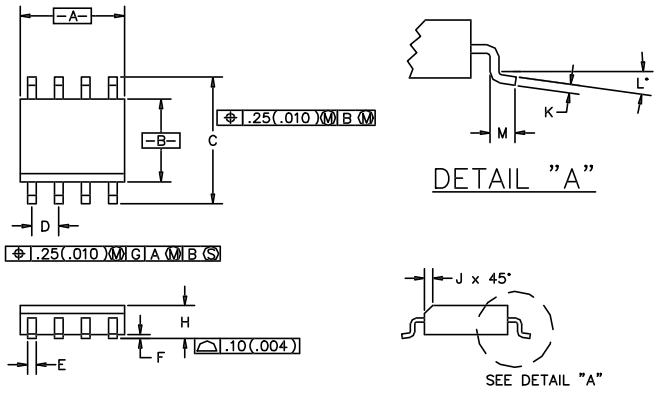
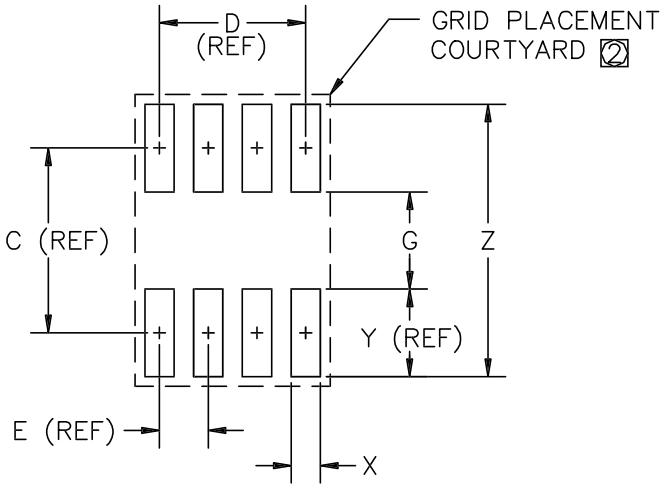
OUTLINE DRAWING SO-8



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050 BSC		1.27 BSC		
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

LAND PATTERN SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS