August 26, 1999

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1405 is a Dual-MOSFET Driver with an internal Overlap Protection Circuit to prevent shoot-through from V_{IN} to GND in the main switching and synchronous MOSFET's. Each driver is capable of driving a 3000pF load in 20ns rise/fall time and has ULTRA-FAST propagation delay from input transition to the gate of the power FET's. The Overlap Protection circuit ensures that the second FET does not turn on until the top FET source has reached a voltage low enough to prevent shoot-through. The delay between the bottom gate going low to the top gate transitioning to high is externally programmable via a capacitor for optimal reduction of switching losses at the operating frequency. The bottom FET may be disabled at light loads by keeping S_MOD low to trigger asynchronous operation, thus saving the bottom FET's gate drive current and inductor ripple current. An internal voltage reference allows threshold adjustment for an Output Over-Voltage protection circuitry, independent of the PWM feedback loop. Under-Voltage-Lock-Out circuit is included to guarantee that both driver outputs are low when the 5V logic level is less than or equal to 4.4V (typ) at supply ramp up (4.35V at supply ramp down). A CMOS output provides status indication of the 5V supply. A low enable input places the IC in stand-by mode thereby reducing supply current to less than 10µA. SC1405 is offered in a high pitch (.025" lead spacing) TSSOP package.

FEATURES

- Fast rise and fall times (20ns typical with 3000pf load)
- 20ns max. Propagation delay (BG going low)
- Adaptive/programmable shoot-through protection
- Wide input voltage range (4.5-25V)
- Programmable delay between MOSFET's
- Power saving asynchronous mode control
- Output overvoltage protection/overtemp shutdown
- Under-Voltage lock-out and power ready signal
- Less than 10µA stand-by current (EN=low)
- Power ready output signal

APPLICATIONS

- High Density/Fast transient power supplies
- Motor Drives/Class-D amps
- High frequency (to 1.2 MHz) operation allows use of small inductors and low cost caps in place of electrolytics
- Portable computers

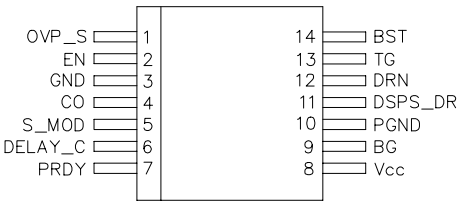
ORDERING INFORMATION

DEVICE(1)	PACKAGE	TEMP. RANGE (T_J)
SC1405TS	TSSOP-14	0 - 125°C

Note:
(1) Add suffix 'TR' for tape and reel.

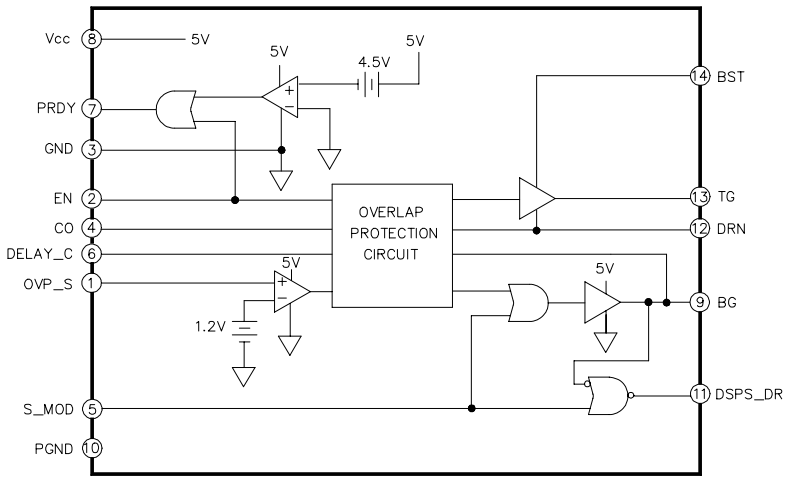
PIN CONFIGURATION

Top View



(14-Pin TSSOP)

BLOCK DIAGRAM



652 MITCHELL ROAD NEWBURY PARK CA 91320

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Maximum	Units
V_{CC} Supply Voltage	V_{MAX5V}		7	V
BST to PGND	$VMAX_{BST-PGND}$		30	V
BST to DRN	$VMAX_{BST-DRN}$		7	V
DRN to PGND	$VMAX_{DRN-PGN}$		25	V
OVP_S to PGND	$VMAX_{OVP\_S-PGND}$		10	V
Input pin	CO		-0.3 to 7.3	V
Continuous Power Dissipation	Pd	Tamb = 25°C, T_J = 125°C Tcase = 25°C, T_J = 125°C	0.66 2.56	W
Thermal Resistance Junction to Case	θ_{JC}		40	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}		150	°C/W
Operating Temperature Range	T_J		0 to +125	°C
Storage Temperature Range	T_{STG}		-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}		300	°C

NOTE:

(1) Specification refers to application circuit in Figure 1.

ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS)

Unless specified: -0 < θ_J < 125°C; V_{CC} = 5V; 4V ≤ V_{BST} ≤ 26V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{CC}	V_{CC}	4.15	5	6.0	V
Quiescent Current	Iq_stby	EN = 0V			10	µA
Quiescent Current, operating	Iq_op	V_{CC} = 5V,CO=0V		1		ma
PRDY						
High Level Output Voltage	V_{OH}	V_{CC} = 4.6V, Iload = 10mA	4.5	4.55		V
Low Level Output Voltage	V_{OL}	V_{CC} < UVLO threshold, Iload = 10µA		0.1	0.2	V
DSPS_DR						
High Level Output Voltage	V_{OH}	V_{CC} = 4.6V, Cload = 100pF	4.15			V
Low Level Output Voltage	V_{OL}	V_{CC} = 4.6V, Cload = 100pF			0.05	V
UNDER-VOLTAGE LOCKOUT						
Start Threshold	V_{START}		4.2	4.4	4.6	V
Hysteresis	$Vhys_{UVLO}$			0.05		V
Logic Active Threshold	V_{ACT}	EN is low			1.5	V

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ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS) Cont.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION						
Trip Threshold	V_{TRIP}		1.145	1.2	1.255	V
Hysteresis	$Vhys_{OVP}$			0.8		V
S_MOD						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
ENABLE						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
CO						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
THERMAL SHUTDOWN						
Over Temperature Trip Point	T_{OTP}			165		°C
Hysteresis	T_{HYST}			10		°C
HIGH-SIDE DRIVER						
Peak Output Current	I_{PKH}			1.5		A
Output Resistance	$Rsrc_{TG}$ $Rsink_{TG}$	duty cycle < 2%, tpw < 100µs, T_J = 125°C, V_{BST} - V_{DRN} = 4.5V, V_{TG} = 4.0V (src)+V_{DRN} or V_{TG} = 0.5V (sink)+V_{DRN}		1.4 1.4		Ω Ω
LOW-SIDE DRIVER						
Peak Output Current	I_{PKL}			2		A
Output Resistance	$Rsrc_{BG}$ $Rsink_{BG}$	duty cycle < 2%, tpw < 100µs, T_J = 125°C V_{V_5} = 4.6V, V_{BG} = 4V (src), or V_{LOWDR} = 0.5V (sink)		2 2		Ω Ω

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ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS) Cont.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC OPERATING SPECIFICATIONS						
HIGH-SIDE DRIVER						
rise time	tr_{TG},	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V,		16	**25**	ns
fall time	tf_{TG}	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V,		17	**27**	ns
propagation delay time, TG going high	$tpdh_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **C-delay=0**		35	**56**	ns
propagation delay time, TG going low	$tpdl_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V,		25	**40**	ns
LOW-SIDE DRIVER						
rise time	tr_{BG}	Cl = 3nF, V_{V_5} = 4.6V,		20	**32**	ns
fall time	tr_{BG}	Cl = 3nF, V_{V_5} = 4.6V,		18	**29**	ns
propagation delay time BG going high	$tpdh_{BGHI}$	Cl = 3nF, V_{V_5} = 4.6V, DRN ≤ 1V		45	**72**	ns
progagation delay time BG going low	$tpdl_{BG}$	Cl = 3nF, V_{V_5} = 4.6V,		12	**20**	ns
UNDER-VOLTAGE LOCKOUT						
V_5 ramping up	$tpdh_{UVLO}$	EN is High			10	us
V_5 ramping down	$tpdl_{UVLO}$	EN is High			10	us
PRDY						
EN is transitioning from low to high	tpdhPRDY	V_5 ≥ UVLO threshold, Delay measured from EN ≥ 2.0V to PRDY ≥ 3.5V			10	µs
EN is transitioning from high to low	$tpdh_{UVLO}$	V_5 ≥ UVLO threshold. Delay measured from EN ≤ 0.8V tp PRDY ≤ 10% of V_5			500	µs
DSPS_DR						
rise/fall time	tr_{DSPS_DR}, tf_{DSPS_DR}	Cl = 100pf, V_5 = 4.6V,			20	ns
propagation delay, DSPS_DR going high	$tpdh_{DSPS\_DR}$	S_MOD goes high and BG goes high or S_MOD goes low			10	ns
propagation delay DSPS_DR goes low	$tpdl_{DSPS\_DR}$	S_MOD goes high and BG goes low			10	ns
OVERVOLTAGE PROTECTION						
propagation delay OVP_S going high	$tpdh_{OVP\_S}$	V_5 = 4.6V, T_J = 125°C, OVP_S ≥ 1.2V to BG > 90% of V_5			1	µs

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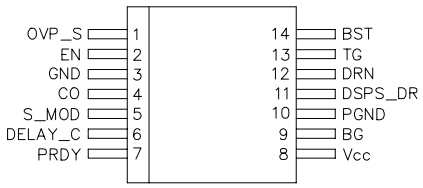
PIN DESCRIPTION

Pin #	Pin Name	Pin Function
1	OVP_S	Overvoltage protection sense. External scaling resistors required to set protection threshold.
2	EN	When high, this pin enables the internal circuitry of the device. When low, TG, BG and PRDY are forced low and the supply current (5V) is less than 10µA.
3	GND	Logic GND.
4	CO	TTL-level input signal to the MOSFET drivers.
5	S_MOD	When low, this signal forces BG to be low. When high, BG is not a function of this signal.
6	DELAY_C	Sets the additional propagation delay for BG going low to TG going high. Total propagation delay= 20ns + 1ns/pF.
7	PRDY	This pin indicates the status of 5V. When 5V is less than 4.4V(typ) this output is driven low. When 5V is greater than or equals to 4.4V(typ) this output is driven to 5V level. This output has a 10mA drive capability and 10µA sink capability.
8	V_{CC}	+5V supply. A .22-1µF ceramic capacitor should be connected from 5V to PGND very close to this pin.
9	BG	Output drive for the synchronous MOSFET.
10	PGND	Power ground. Connect to the synchronous FET power ground.
11	DSPS_DR	Dynamic Set Point Switch Drive. TTL level output signal. When S_MOD is high, this pin follows the BG driver pin voltage.
12	DRN	This pin connects to the junction of the switching and synchronous MOSFET's. This pin can be subjected to a -2V minimum relative to PGND without affecting operation.
13	TG	Output gate drive for the switching (high-side) MOSFET.
14	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1µF and 1µF (ceramic).

NOTE:

(1) All logic level inputs and outputs are open collector TTL compatible.

PIN CONFIGURATION



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APPLICATION CIRCUIT

Typical Distributed Power Supply

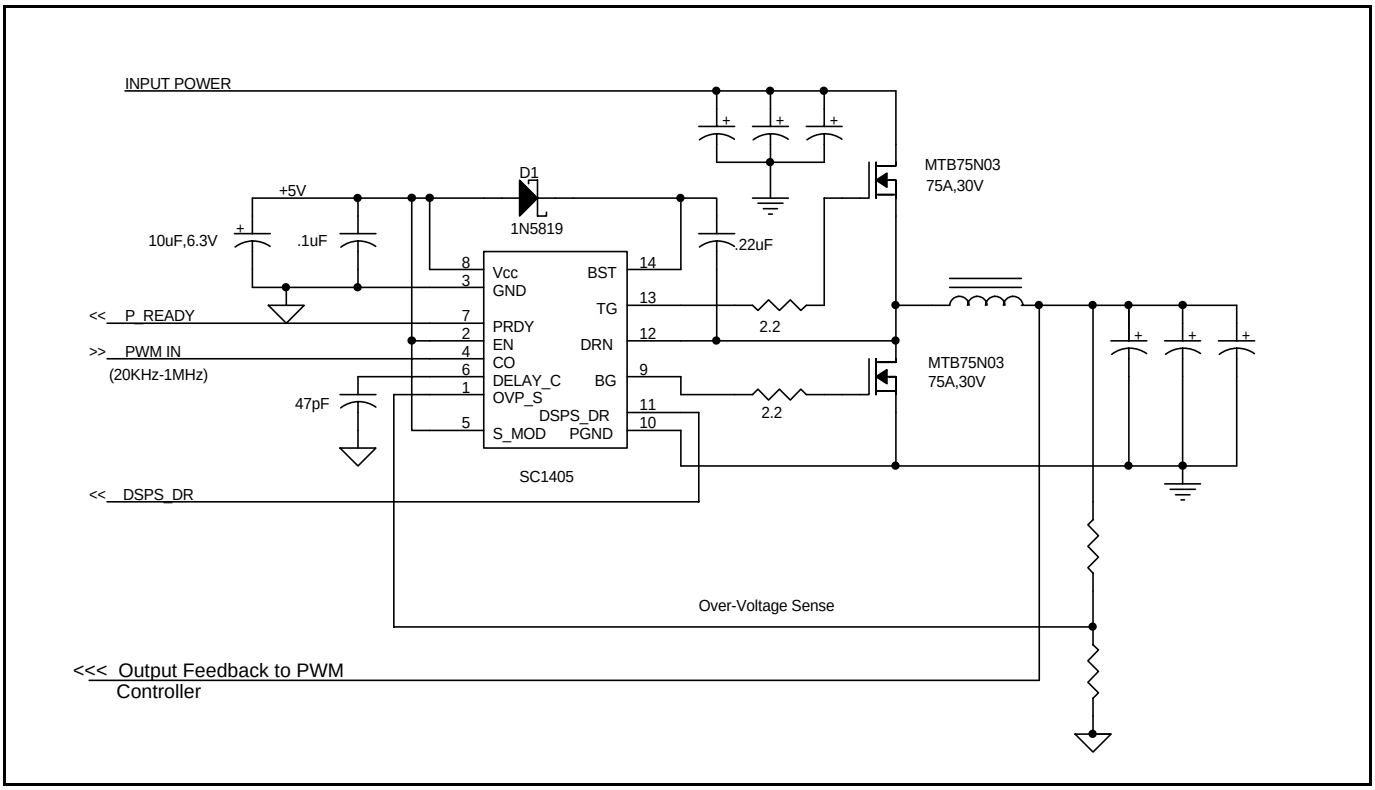

Figure 1.

TIMING DIAGRAM

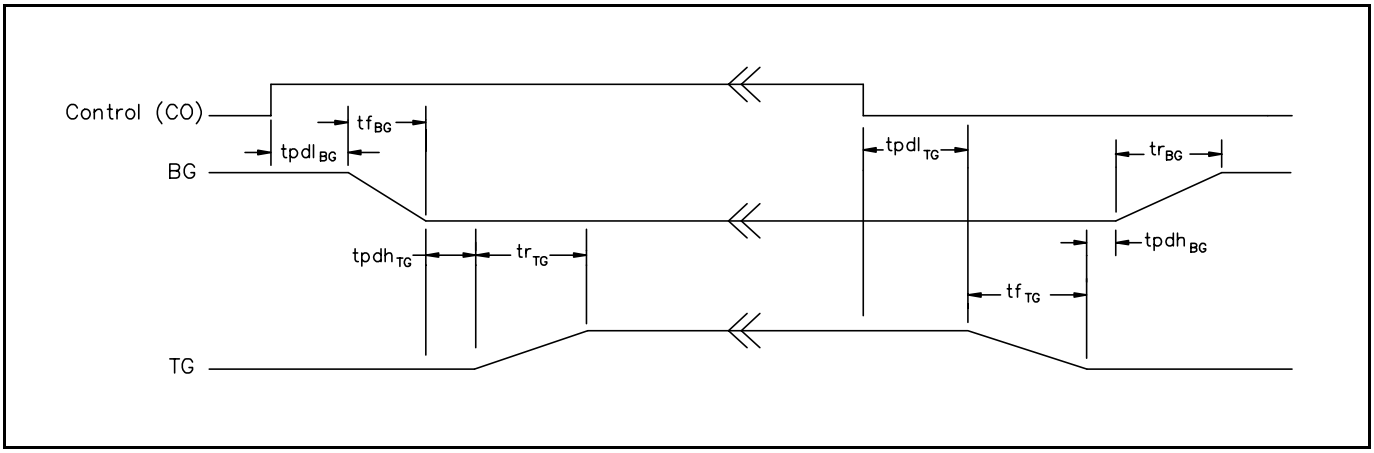

Figure 2.

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APPLICATION EVALUATION BOARD SCHEMATIC

SC1405/SC1144 Evaluation Board.
4-Phase synchronous, Freq.=1MHz

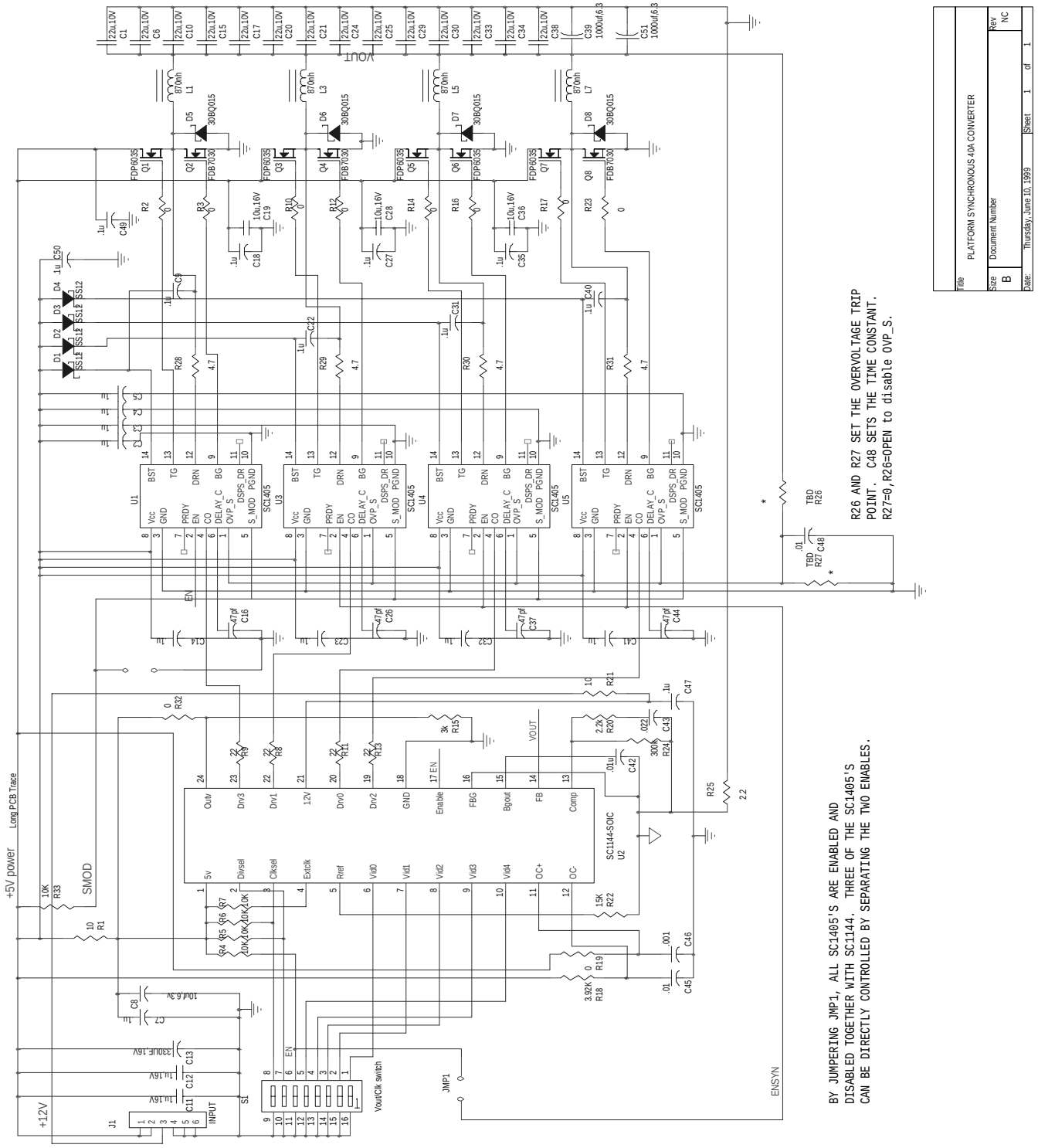

Figure 3

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BILL OF MATERIAL

Item	Qty	Reference	Value	Manufacturer
1	14	C1,C6,C10,C15,C17,C20,C21,C24,C25,C29,C30,C33,C34,C38	22u, 10V	Murata (GRM235Y5V226Z010)
2	19	C2,C3,C4,C5,C7,C9,C14,C18,C22,C23,C27,C31,C32,C35,C40, C41,C47,C49,C50	.1uF	any
3	1	C8	10uF, 6.3V	any
4	2	C11,C12	1uF, 16V	any
5	1	C13	330uf, 16V	Sanyo
6	4	C16,C26,C37,C44	44pF	any
7	3	C19,C28,C36	10uF, 16V	any
8	2	C39,C51	1000uF, 6.3V	any
9	3	C42,C45,C46	.01uf	any
10	1	C43	.022	Avx, any
11	1	C46	.001	Avx, any
12	4	D1,D2,D3,D4	SS12	General Instruments
13	4	D5,D6,D7,D8	30BQ015	Int. Rectifier (310) 252-7099
14	2	JMP1,JMP2	Jumper	
15	1	J1	Input	
16	4	L1,L3,L5,L7	.87uh	Falco, P/N: TO2509 (305) 662-9076
17	5	Q1,Q3,Q5,Q6,Q7	FDP6035	Fairchild Semi. (408) 822-2000
			IR7811	Int. Rectifier
18	3	Q2,Q4,Q8	FDB7030	Fairchild Semi.
19	2	R1,R21	10	any
20	10	R2,R3,R10,R12,R14,R16,R17,R19,R23,R32	0	any
21	5	R4,R5,R6,R7,R33	10k	any
22	4	R8,R9,R11,R13	22	any
23	1	R15	3k	any
24	1	R18	3.92k	any
25	1	R20	2.2k	any
26	1	R22	15K	any
27	1	R24	300K	any
28	1	R25	2.2	any
29	2	R26,R27	TBD	any
30	4	R28,R29,R30,R31	4.7	any
31	1	S1	Vout/Clk switch	Digikey
32	4	U1,U3,U4,U5	SC1405	Semtech, (805) 499-2111
33	1	U2	SC1144CSW	Semtech, (805) 499-2111

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APPLICATION INFORMATION:

SC1405 is a high speed, smart dual MOSFET driver. It is designed to drive Low Rds_On power MOSFET's with ultra-low rise/fall times and propagation delays. As the switching frequencies of PWM controllers is increased to reduce power supply and Class-D amplifier volume and cost, fast rise and fall times are necessary to minimize switching losses (TOP MOSFET) and reduce Dead-time (BOTTOM MOSFET). While Low Rds_On MOSFET's present a power saving in I^2R losses, the MOSFET's die area is larger and thus the effective input capacitance of the MOSFET is increased. Often a 50% decrease in Rds_On more than doubles the effective input gate charge, which must be supplied by the driver. The Rds_On power savings can be offset by the switching and dead-time losses with a sub-optimum driver. While discrete solution can achieve reasonable drive capability, implementing shoot-through, programmable delay and other housekeeping functions necessary for safe operation can become cumbersome and costly. The SC1405 family of parts presents a total solution for the high-speed, high power density applications. Wide input supply range of 4.5V-25V allows use in battery powered applications, new high voltage, distributed power servers as well as Class-D amplifiers.

THEORY OF OPERATION

The control input (CO) to the SC1405 is typically supplied by a PWM controller that regulates the power supply output. (See Application Evaluation Schematic, Figure 3). The timing diagram demonstrates the sequence of events by which the top and bottom drive signals are applied. The shoot-through protection is implemented by holding the bottom FET off until the voltage at the phase node (intersection of top FET source, the output inductor and the bottom FET drain) has dropped below 1V. This assures that the top FET has turned off and that a direct current path does not exist between the input supply and ground, a condition which both the top and bottom FET's are on momentarily. The top FET is also prevented from turning on until the bottom FET is off. This time is internally set to 20ns (typical) and may be increased by adding a capacitor to the C-Delay pin. The delay is approximately 1ns/pf in addition to the internal 20ns delay. The external capacitor may be needed if multiple High input capacitance MOSFET's are used in parallel and the fall time is substantially greater than 20ns.

It must be noted that increasing the dead-time by high values of C-Delay capacitor will reduce efficiency since the parallel Schottky or the bottom FET body diode will have to conduct during dead-time.

LAYOUT GUIDELINES

As with any high speed , high current circuit, proper layout is critical in achieving optimum performance of the SC1405. The Evaluation board schematic (Refer to figure 3) shows a four-phase synchronous design with all surface mountable components.
While components connecting to C-Delay, OVP_S, EN,S-MOD, DSPS_DR and PRDY are relatively non-critical, tight placement and short,wide traces must be used in layout of The Drives, DRN, and especially PGND pin. The top gate driver supply voltage is provided by bootstrapping the +5V supply and adding it the phase node voltage (DRN). Since the bootstrap capacitor supplies the charge to the TOP gate, it must be less than .5" away from the SC1405. Ceramic X7R capacitors are a good choice for supply bypassing near the chip. The Vcc pin capacitor must also be less than .5" away from the SC1405. The ground node of this capacitor, the SC1405 PGND pin and the Source of the bottom FET must be very close to each other, preferably with common PCB copper land with multiple vias to the ground plane (if used). The parallel Schottky must be physically next to the Bottom FETS Drain and source. Any trace or lead inductance in these connections will drive current way from the Schottky and allow it to flow through the FET's Body diode, thus reducing efficiency.

PREVENTING INADVERTENT BOTTOM FET TURN-ON

At high input voltages, (12V and greater) a fast turn-on of the top FET creates a positive going spike on the Bottom FET's gate through the Miller capacitance, Crss of the bottom FET. The voltage appearing on the gate due to this spike is:

Vspike=Vin*crss/(Crass+ciss)

Where Ciss is the input gate capacitance of the bottom FET. This is assuming that the impedance of the drive path is too high compared to the instantaneous impedance of the capacitors. (since dV/dT and thus the effective frequency is very high). If the BG pin of the SC1405 is very close to the bottom FET, Vspike will be reduced depending on trace inductance, rate if rise of current,etc.

While not shown in Figure 3, a capacitor may be added from the gate of the Bottom FET to its source, prefer-

ably less than .1" away. This capacitor will be added to Ciss in the above equation to reduce the effective spike voltage, Vspike.
The selection of the bottom MOSFET must be done with attention paid to the Crss/Ciss ratio. A low ratio reduces the Miller feedback and thus reduces Vspike. Also MOSFETs with higher Turn-on threshold voltages will conduct at a higher voltage and will not turn on during the spike. The MOSFET shown in the schematic (figure 3) has a 2 volt threshold and will require approximately 5 volts Vgs to be conducting, thus reducing the possibility of shoot-through. A zero ohm bottom FET gate resistor will obviously help keeping the gate voltage low. Ultimately, slowing down the top FET by adding gate resistance will reduce di/dt which will in turn make the effective impedance of the capacitors higher, thus allowing the BG driver to hold the bottom gate voltage low. It does this at the expense of increased switching times (and switching losses) for the top FET.

RINGING ON THE PHASE NODE

The top MOSFET source must be close to the bottom MOSFET drain to prevent ringing and the possibility of the phase node going negative. This frequency is determined by:

$F_{ring} = 1/(2¶* Sqrt(L_{st}*Coss))$

Where:

L_{st} = The effective stray inductance of the top FET added to trace inductance of the connection between top FET's source and the bottom FET's drain added to the trace resistance of the bottom FET's ground connection. Coss=Drain to source capacitance of bottom FET. If there is a Schottky used, the capacitance of the Schottky is added to the value.

Although this ringing does not pose any power losses due to a fairly high Q, it could cause the phase node to go too far negative, thus causing improper operation, double pulsing or at worst driver damage. This ringing is also an EMI nuisance due to its high resonant frequency. Adding a capacitor, typically 1000-2000pf, in parallel with Coss can often eliminate the EMI issue. If double pulsing is caused due to excessive ringing, placing 4.7-10 ohm resistor between the phase node and the DRN pin of the SC1405 should eliminate the double pulsing. Proper layout will guarantee minimum ringing and eliminate the need for external components. Use of SO-8 or other surface mount MOSFETs will reduce lead inductance as well as radiated EMI.

ASYNCHRONOUS OPERATION

The SC1405 can be configured to operate in Asynchronous mode by pulling S-MOD to logic LOW, thus disabling the bottom FET drive. This has the effect of saving power at light loads since the bottom FET's gate capacitance does not have to charged at the switching frequency. There can be a significant savings since the bottom driver can supply up to 2A pulses to the FET at the switching frequency. There is an additional efficiency benefit to operating in asynchronous mode. When operating in synchronous mode, the inductor current can go negative and flow in reverse direction when the bottom FET is on and the DC load is less than 1/2 inductor ripple current. At that point, the inductor core and wire losses, depending on the magnitude of the ripple current, can be quite significant. Operating in asynchronous mode at light loads effectively only charges the inductor by as much as needed to supply the load current, since the inductor never completely discharges at light loads. DC regulation can be an issue depending on the type of controller used and minimum load required to maintain regulation. If there are no Schottkys used in parallel with bottom FET, the FET's body diode will need to conduct in asynchronous mode. The high voltage drop of this diode must be considered when determining the criteria for this mode of operation.

DSPS DR

This pin produces an output which is a logical duplicate of the bottom FET's gate drive, if S-MOD is held LOW.

OVP_S/OVER TEMP SHUTDOWN

Output over-voltage protection may be implemented on the SC1405 independent of the PWM controller . A voltage divider from the output is compared with the internal bandgap voltage of 1.2V (typical). Upon exceeding this voltage, the overvoltage comparator disables the top FET, while turning on the bottom FET to allow discharge of the output capacitors excessive voltage through the output inductor. There should be sufficient RC time constant as well as voltage headroom on the OVP_S pin to assure it does not enter overvoltage mode inadvertently. The SC1405 will shutdown if its Tj exceeds 165 °C.

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Performance diagrams, Application Evaluation Board. (Fig.3)

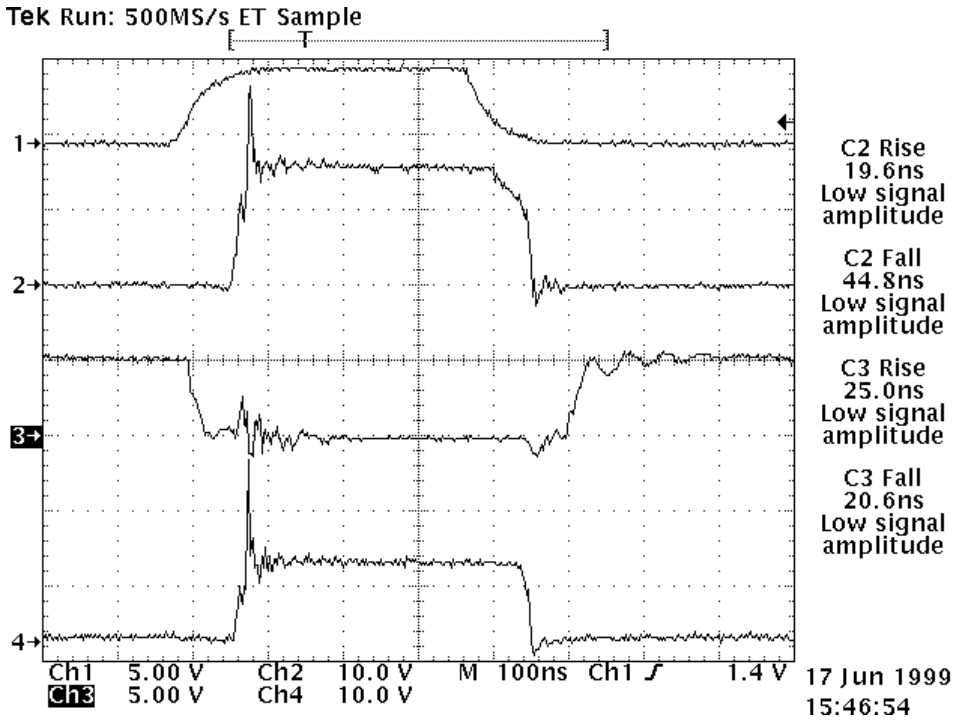

Figure 4-Timing diagram:

Ch1:CO input

Ch2:TG drive

Ch3:BG non-overlap drive

Ch4:phase node
Iout=20A (10A/phase)
Refer to Eval. Schematic (fig.3)

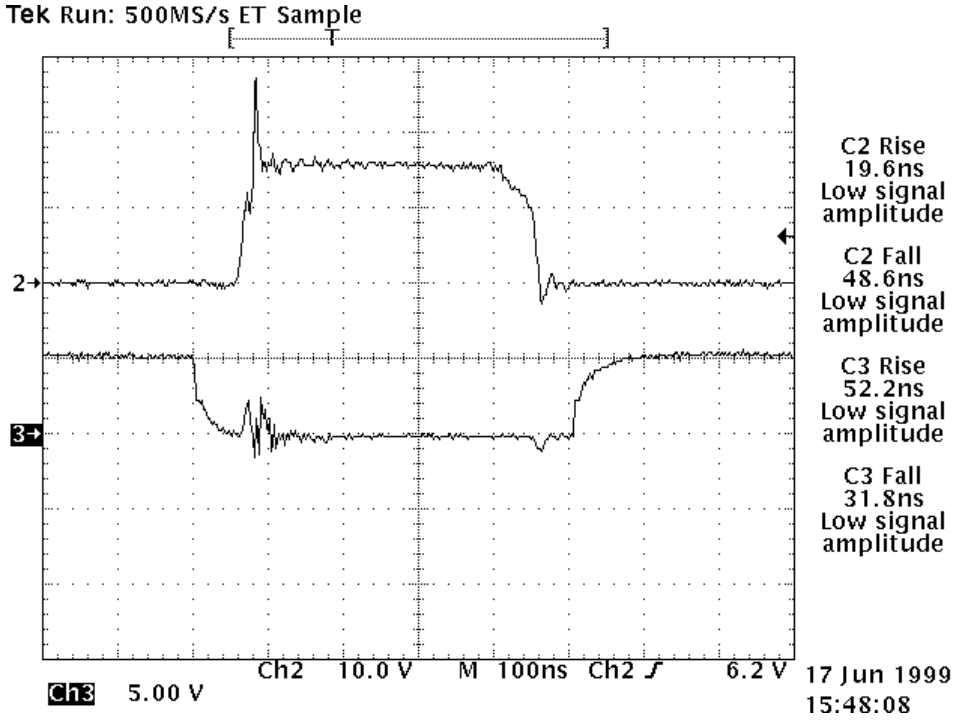

Figure 5-Timing diagram:
Rise/Fall times

Ch1:TG drive

Ch2:BG drive

Cursor:$Tpdh_{TG}$

Iout=20A (10A/phase)
Refer to Eval. Schematic (fig.3)

Vin=10V, Vout=2V TOP FET IR7811, Bottom FET IR7030(L) Qg(tot)=35nc

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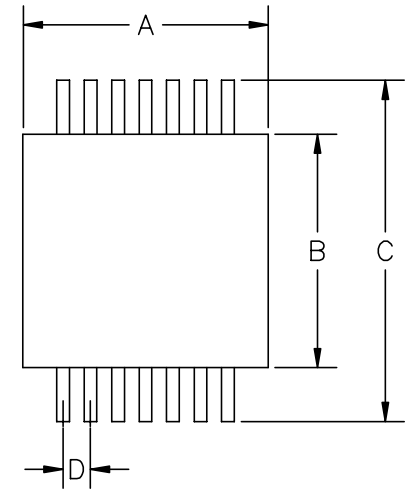
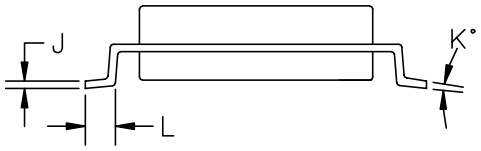
OUTLINE DRAWING TSSOP-14





DIMENSIONS ①					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.1929	.2007	4.90	5.10	②
B	.169	.177	4.30	4.50	②
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0015	.0080	.05	.15	—
G		.078		1.20	—
J	.0040	.0100	.09	.20	—
K	0°	8°	0°	8°	—
L	.022	.037	.45	.75	—

JEDEC MO-153AB1

② DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

① CONTROLLING DIMENSIONS: MILLIMETERS.