PRELIMINARY - May 17, 1999

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

Intended for applications such as Power Managed PCI, the SC1532 is designed to maintain a glitch-free 3.3V output when at least one of two inputs, 5V (VIN1) and 3.3V (VIN2), is present.

The SC1532 combines a 5V to 3.3V linear regulator with an integral 3.3V bypass switch, along with logic and detection circuitry to control which supply provides the power for the output.

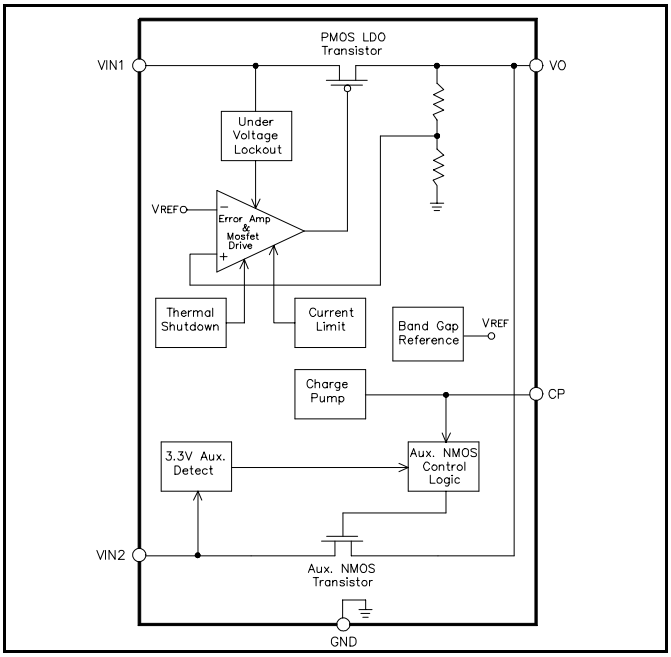
Whenever VIN1 exceeds a predetermined threshold value, the internal 3.3V PMOS linear regulator is enabled, and the internal pass NMOS is turned off. When VIN1 falls below a lower threshold value, the NMOS pass device is turned on and the PMOS linear regulator is turned off. This ensures an uninterrupted 3.3V output even if VIN1 falls out of specification.

When both supplies are simultaneously available, the PMOS linear regulator will be turned on, and the NMOS pass will be turned off, thus preferentially supplying the output from the 5V supply.

The internal 5V detector has its upper threshold (for VIN1 rising) set to 4.18V (typical) while the lower threshold (for VIN falling) is at 4.1V (typical) giving a hysteresis of approximately 80mV.

The SC1532 is available in the popular SO-8 surface mount package.

BLOCK DIAGRAM



FEATURES

- Glitch-free transition between input sources
- Internal logic selects input source
- 5V detector with hysteresis
- 1% regulated output voltage accuracy
- 400mA load current capability

APPLICATIONS

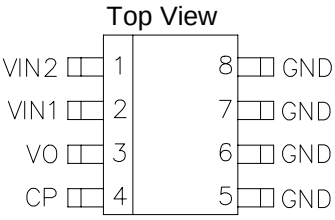
- Desktop Computers
- Network Interface Cards (NICs)
- PCMCIA/PCI Interface Cards
- Peripheral Cards

ORDERING INFORMATION

Part Number[1]	Package	Temp. Range (T_J)
SC1532CS	SO-8	-5° to 125°C

Note:
(1) Add suffix 'TR' for tape and reel packaging.

PIN CONFIGURATION



(SO-8)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Input Supply Voltage	VIN	-0.5 to +7	V
Output Current	I_O	400	mA
Operating Temperature Range	T_A	-5 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec	T_{LEAD}	300	°C
Thermal Impedance Junction to Ambient[1]	θ_{JA}	65	°C/W
ESD Rating	ESD	2	kV

Note:
(1) 1 inch square of 1/16" FR-4, double sided, 1 oz. minimum copper weight.

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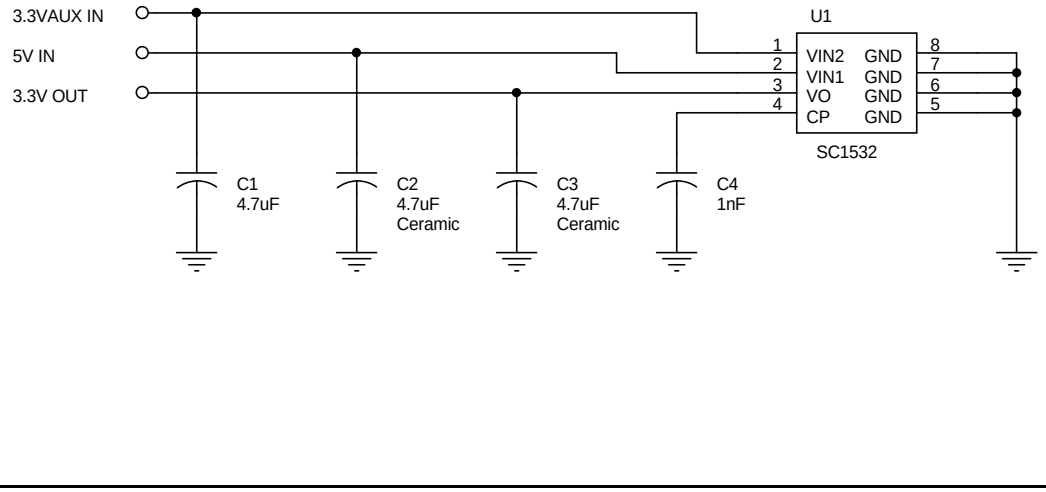
PIN DESCRIPTION

Pin	Pin Name	Pin Function
1	VIN2	Secondary input supply, nominally 3.3V.
2	VIN1	Main input supply for the IC, nominally 5V.
3	VO	3.3V out.
4	CP	Charge pump capacitor connection.
5	GND	Ground pin.
6	GND	Ground pin.
7	GND	Ground pin.
8	GND	Ground pin.

APPLICATION CIRCUIT



NOTE:
(1) Capacitors C2 and C3 need to be 1.0uF ceramics for stability. Additional capacitance (tantalum or ceramic) will improve overall performance.

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ELECTRICAL CHARACTERISTICS

Unless specified, T_A = 25°C, VIN1 = 5V, VIN2 = 3.3V, I_O = 400mA, CIN1 = 4.7uF, CIN2 = 4.7uF, C_O = 4.7uF, Cp=1nF.
Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
VIN1						
Supply Voltage	VIN1	VIN2 = 0V	4.3	5.0	5.5	V
Quiescent Current	I_{Q1}	VIN1 = 5V, 0V ≤ VIN2 ≤ 3.6V, I_O = 0mA		2.2	4.0	mA
					TBD	
Reverse Leakage From VIN2(1)	I_{VIN1}	VIN1 = 0V, VIN2 = 3.6V, I_O = 0mA		0	1	µA
VIN2						
Supply Voltage	VIN2		3.0	3.3	3.6	V
Quiescent Current	I_{Q2}	VIN2 = 3.3V, 0V ≤ VIN1 ≤ 5.5V, I_O = 0mA		650	1300	µA
					TBD	
Reverse Leakage From VIN1(1)	I_{VIN2}	VIN1 = 5.5V, VIN2 = 0V, I_O = 0mA		0	1	µA
5V Detect						
Low Threshold Voltage(1)	$V_{TH(LO)}$	VIN1 Falling, I_O = 20mA	**3.90**	4.10		V
Hysteresis(1)	V_{HYST}	I_O = 20mA	60	80	150	mV
High Threshold Voltage	$V_{TH(HI)}$	VIN1 Rising, I_O = 20mA		4.18	**4.30**	V
VO						
LDO Voltage Accuracy	VO	I_O = 20mA	-1		+1	%
		4.3V ≤ VIN1 ≤ 5.5V, 0mA ≤ I_O ≤ 400mA			**TBD**	
		3.90V ≤ VIN1 ≤ 4.3V, VIN2 = 3.3V, 0mA ≤ I_O ≤ 400mA	**3.000**			V
VIN2 Pass Device ESR(1)(2)	R_{ESR}	VIN1 < 3.9V, 0mA ≤ I_O ≤ 400mA		300		mΩ
(Aux. NMOS Transistor)					**TBD**	
Line Regulation	$REG_{(LINE)}$	VIN1 = 4.3V to 5.5V		0.3	0.6	%
					TBD	
Load Regulation	$REG_{(LOAD)}$	I_O = 20mA to 400mA		0.3	0.6	%
					TBD	
Current Limit (LDO)						
Output Current	I_{LIM}	VIN1=5V, VIN2=0V, Vout=0V	600	875	1100	mA
					TBD	
Over Temperature Protection						
High Trip Level	T_{HI}	VIN1=5V		165		ºC
Hysteresis	T_{HYS}	VIN1=5V		10		ºC

NOTES:
(1) Guaranteed by design.
(2) Refer to block diagram.

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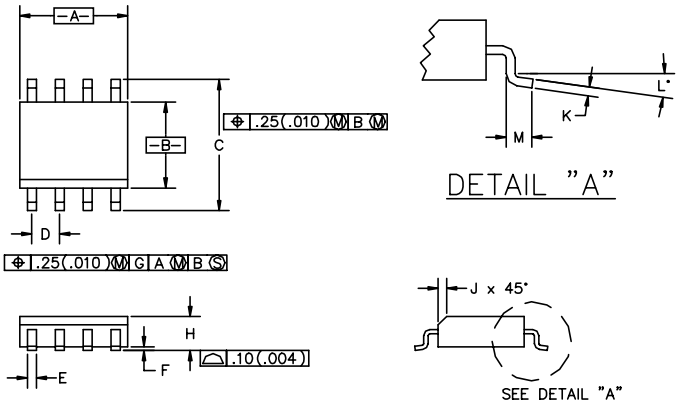
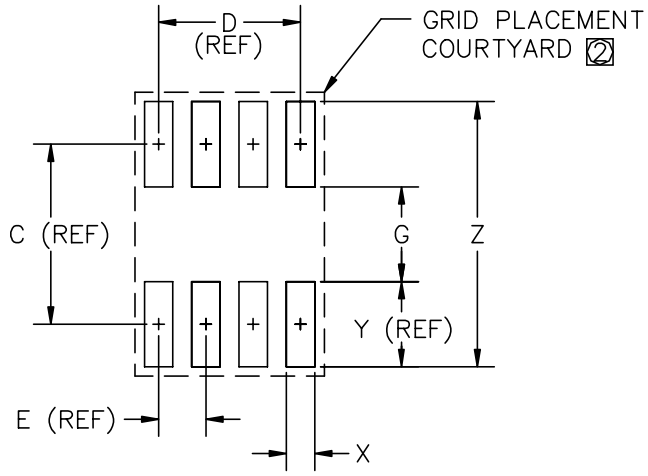
OUTLINE DRAWING - SO-8



JEDEC
REF: MS-012AA

DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

LAND PATTERN - SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS