PRELIMINARY - April 9, 1999
TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1531 is designed to maintain a glitch-free 3.3V output when at least one of two inputs, 5V (VIN) and 3.3V (VAUX), is present.

Whenever VIN exceeds a predetermined threshold value, the internal 3.3V linear regulator is enabled, and DR is pulled high.

When VIN falls below a lower threshold value, DR is pulled low and the internal linear regulator is turned off. DR has been designed to drive the gate of an external low threshold P-channel MOSFET, which can be used to connect the 3.3V supply directly to the regulator output. This ensures an uninterrupted 3.3V output even if VIN falls out of specification. A typical $R_{DS(ON)}$ of 400mΩ is recommended.

When both supplies are simultaneously available, the drive pin (DR) will be pulled High, turning off the external PMOS switch.

The internal 5V detector has its upper threshold (for VIN rising) set to 4.18V (typical) while the lower threshold (for VIN falling) is at 4.05V (typical) giving a hysteresis of approximately 130mV.

The SENSE pin, which is connected to the load, connects internally to the inverting input of the LDO error amplifier. It enables tight regulation of the load voltage (while the 5V supply is present) despite variations in load current.

The SC1531 is available in the popular SO-8 surface mount package.

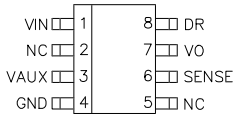
ORDERING INFORMATION

Part Number(1)	Package	Temp. Range (T_J)
SC1531CS	SO-8	-5° to 125°C

Note:
(1) Add suffix 'TR' for tape and reel packaging.

PIN CONFIGURATION

Top View



(SOIC-8)

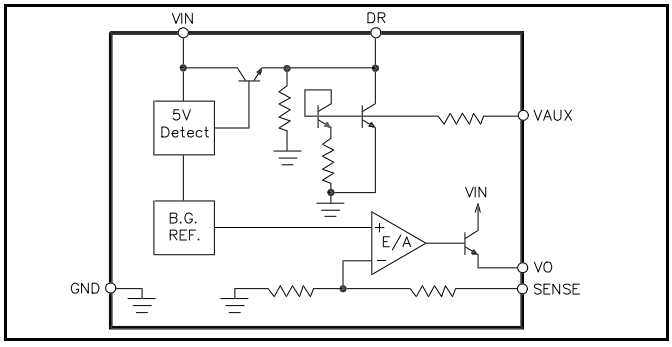
FEATURES

- Glitch-free transition between input sources
- Internal logic selects input source
- Gate drive for external PMOS bypass switch
- 5V detector with hysteresis
- 1% regulated output voltage accuracy
- 200mA load current capability
- Remote sense

APPLICATIONS

- Desktop Computers
- Network Interface Cards (NICs)
- PCMCIA/PCI Interface Cards
- Cardbus™ Technology
- Power supplies with multiple input sources

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Input Supply Voltage	VIN	-0.5 to +7	V
Auxiliary Supply Voltage	VAUX	-0.5 to +7	V
LDO Output Current	I_O	200	mA
Operating Temperature Range	T_A	-5 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec	T_{LEAD}	300	°C
Thermal Impedance Junction to Ambient	θ_{JA}	130	°C/W
Thermal Impedance Junction to Case	θ_{JC}	47	°C/W
ESD Rating	ESD	2	kV

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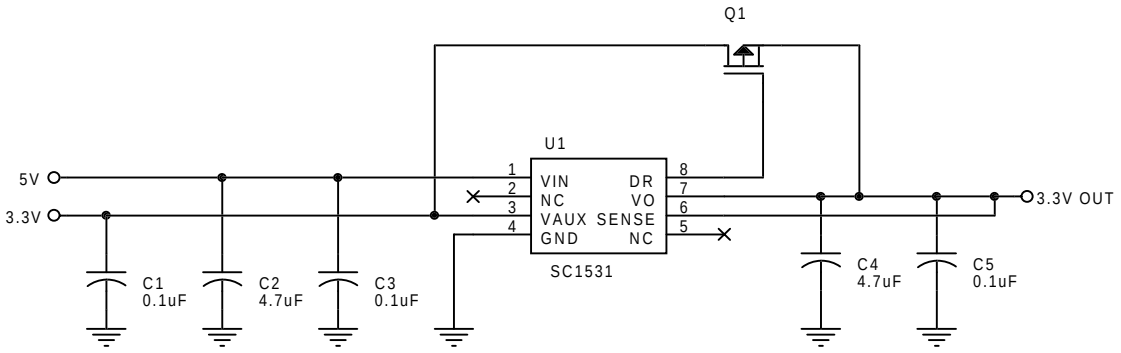
PIN DESCRIPTION

Pin	Pin Name	Pin Function
1	VIN	This is the main input supply for the IC, nominally 5V.
2	NC	No connection.
3	VAUX	This is the auxiliary input supply , nominally 3.3V.
4	GND	Logic and power ground.
5	NC	No connection.
6	SENSE	Sense pin for VO. Connect to VO at the load to minimize voltage drop across PCB traces.
7	VO	LDO 3.3V output.
8	DR	Driver output for external P-channel MOSFET pass element.

APPLICATION CIRCUIT



NOTE:
(1) External switch (Q1): use Motorola MGSF1P02ELT1 or equivalent (PMOS, typical Gate Threshold Voltage = 1V, typical $R_{DS(ON)}$ = 0.4Ω at V_{GS} = 2.5V).

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ELECTRICAL CHARACTERISTICS

Unless specified, T_A = 25°C, VIN = 5V, VAUX = 3.3V, I_O = 200mA, C_O = 4.7µF. Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
VIN						
Supply Voltage	VIN	VAUX = 0V	**4.3**	**5.0**	**5.5**	V
Quiescent Current	I_Q	VIN = 5V, VAUX = 0V, I_O = 0mA		7.0	10.0	mA
					11.0	
		VIN = 5V, VAUX = 3.3V, I_O = 0mA		7.5	10.0	mA
					12.0	
Reverse Leakage From VAUX	I_{VIN}	VAUX = 3.6V, VIN = 0V, I_O = 0mA		-1.0	-10	µA
					-20	
VAUX						
Supply Voltage	VAUX		**3.0**	**3.3**	**3.6**	V
Quiescent Current	$I_{Q(AUX)}$	VAUX = 3.3V, VIN = 0V, I_O = 0mA		0.8	1.5	mA
					2.0	
		VAUX = 3.3V, VIN = 5V, I_O = 0mA		0.6	1.0	mA
					2.0	
Reverse Leakage From VIN	I_{VAUX}	VIN = 5.5V, VAUX = 0V, I_O = 0mA		-7.0	-50.0	µA
					-100.0	
5V Detect[(1)(2)(3)]						
Low Threshold Voltage	$V_{TH(LO)}$	VIN Falling	**3.90**	4.05	**4.20**	V
Hysteresis	V_{HYST}		90	200		mV
			80			
High Threshold Voltage	$V_{TH(HI)}$	VIN Rising			**4.30**	V
VO						
LDO Output Voltage	VO	I_O = 20mA	3.267	3.300	3.333	V
		4.3V ≤ VIN ≤ 5.5V, 0mA ≤ I_O ≤ 200mA	**3.234**		**3.366**	
		3.9V ≤ VIN ≤ 4.3V, VAUX = 3.3V, 0mA ≤ I_O ≤ 200mA[(4)]	**3.000**			
Line Regulation	$REG_{(LINE)}$	VIN = 4.3V to 5.5V		0.12	0.40	%
					0.60	
Load Regulation	$REG_{(LOAD)}$	I_O = 20mA to 200mA		0.12	0.40	%
					0.60	

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ELECTRICAL CHARACTERISTICS

Unless specified, T_A = 25°C, VIN = 5V, VAUX = 3.3V, I_O = 200mA, C_O = 4.7µF. Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
SENSE						
SENSE Pin Impedance	R_{SENSE}		6.0	8.5		kΩ
			6.0			
DR						
Drive Voltage	V_{DR}	4.3V ≤ VIN ≤ 5.5V, I_{DR} = 200µA	3.4	VIN - 0.8		V
			3.3			
		VIN < $V_{TH(LO)}$, I_{DR} = -200µA		35	150	mV
					200	
Peak Drive Current	$I_{DR(PK)}$	Sinking: VIN = 3.9V, V_{DR} = 1V;	7			mA
		Sourcing: VIN = 4.3V, VIN - V_{DR} = 2V	**6**			
Drive High Delay(1)(5)	t_{DH}	C_{DR} = 1.2nF, VIN ramping up, measured		0.5	1.0	µs
		from VIN = $V_{TH(HI)}$ to V_{DR} = 2V			**2.0**	
Drive Low Delay(1)(5)	t_{DL}	C_{DR} = 1.2nF, VIN ramping down, measured		0.5	1.0	µs
		from VIN = $V_{TH(LO)}$ to V_{DR} = 2V			**2.0**	

NOTES:

(1) Guaranteed by design.
(2) See 5V Detect Thresholds on page 5.
(3) Recommended source impedance for 5V supply: ≤ 0.25Ω. This will ensure that I_O x R_{SOURCE} < V_{HYST}, thus avoiding DR toggling during 5V detect threshold transitions.
(4) In Application Circuit on page 2.
(5) See Timing Diagram on page 5.

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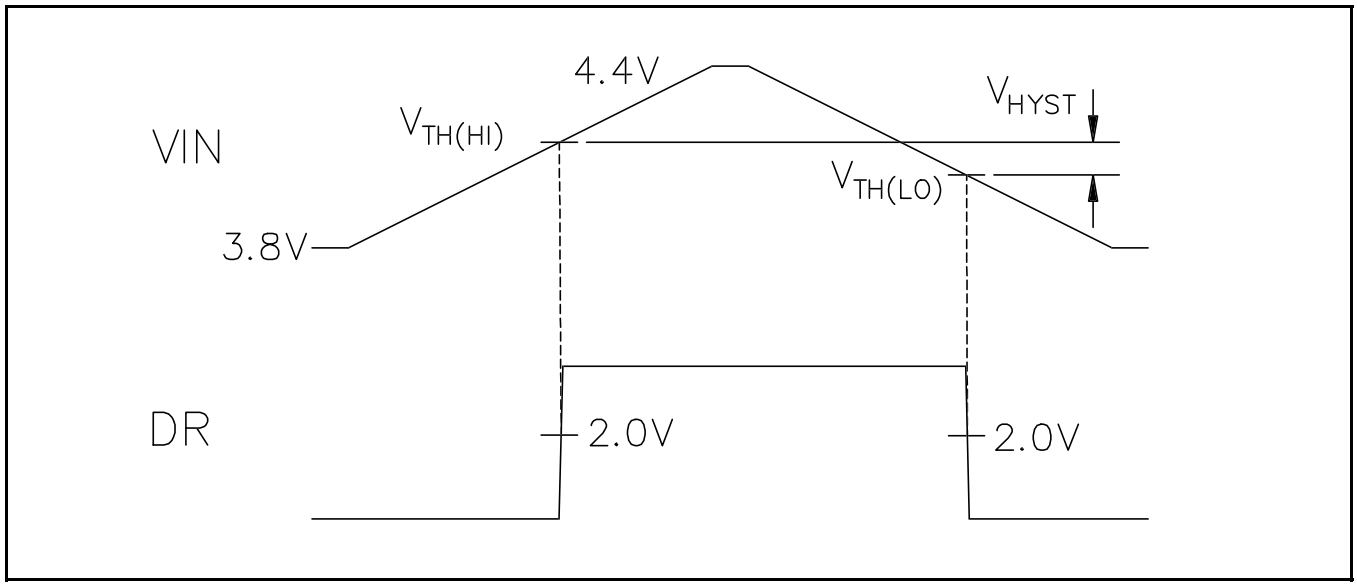
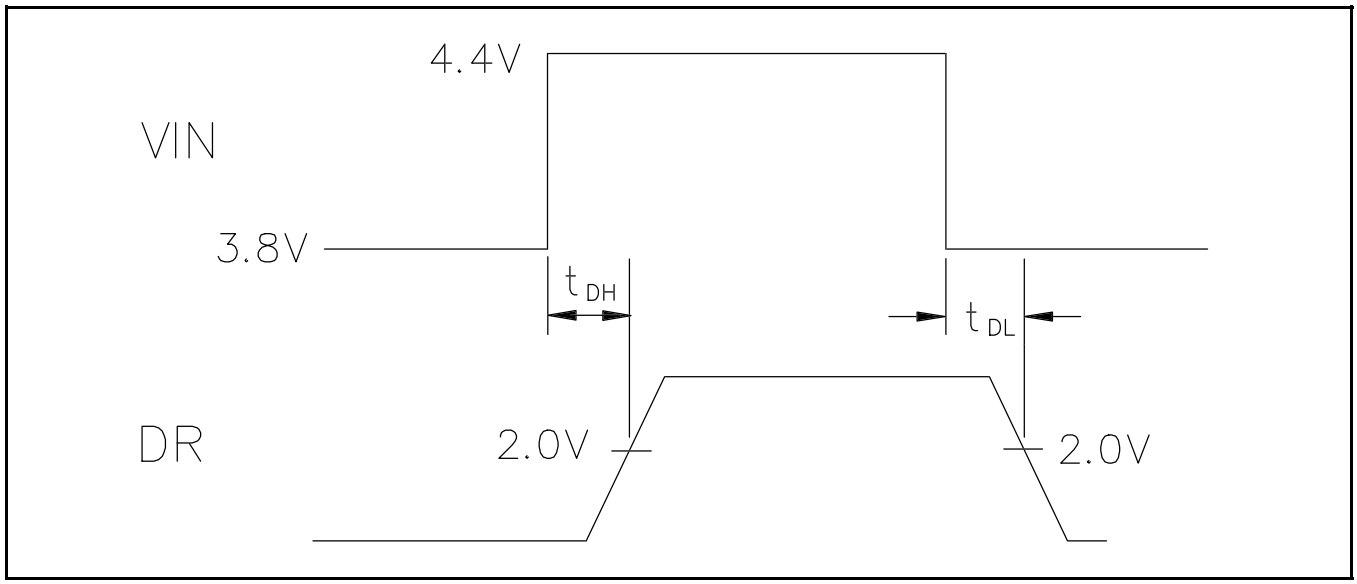
5V DETECT THRESHOLDS



NOTE:
(1) VIN rise and fall times (10% to 90%) to be ≥ 100µs.

TIMING DIAGRAM



NOTE:
(1) VIN rise and fall times (10% to 90%) to be ≤ 100ns.

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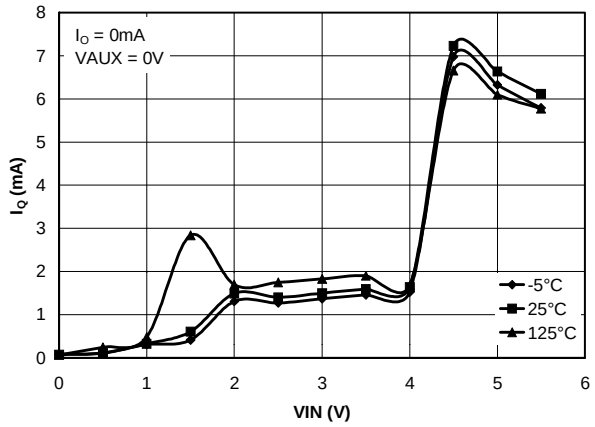
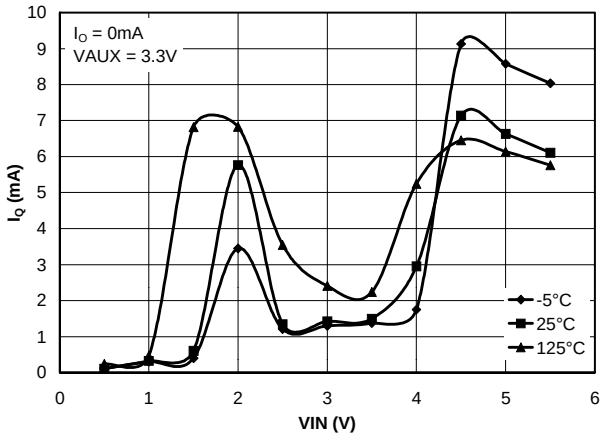
TYPICAL CHARACTERISTICS

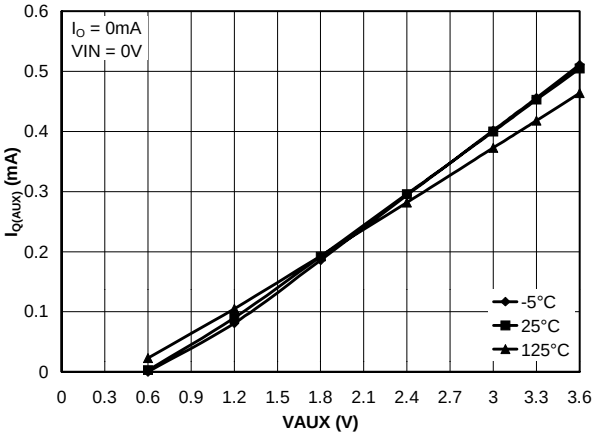
I_Q vs. VIN vs. Junction Temperature



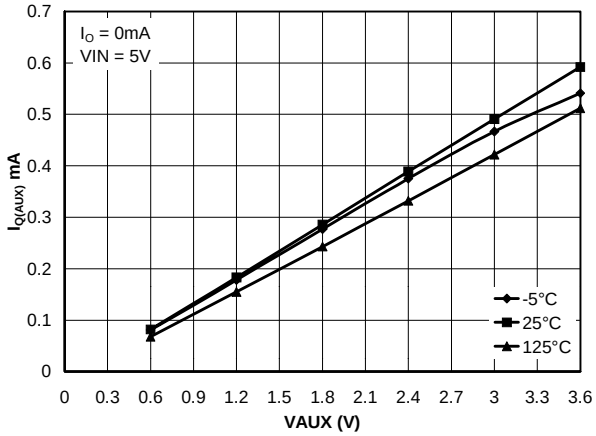
I_Q vs. VIN vs. Junction Temperature



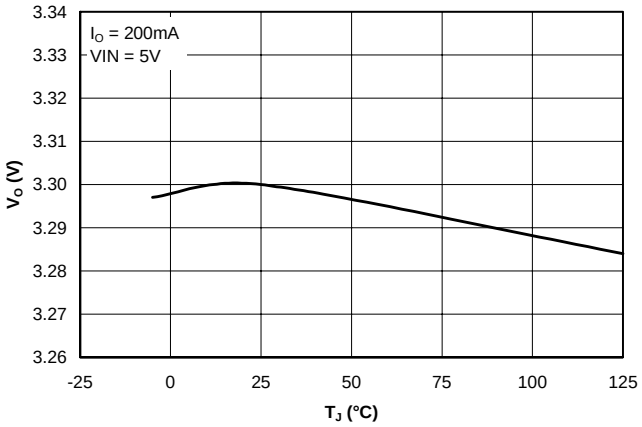
$I_{Q(AUX)}$ vs. VAUX vs. Junction Temperature



$I_{Q(AUX)}$ vs. VAUX vs. Junction Temperature



LDO Output Voltage vs. Junction Temperature



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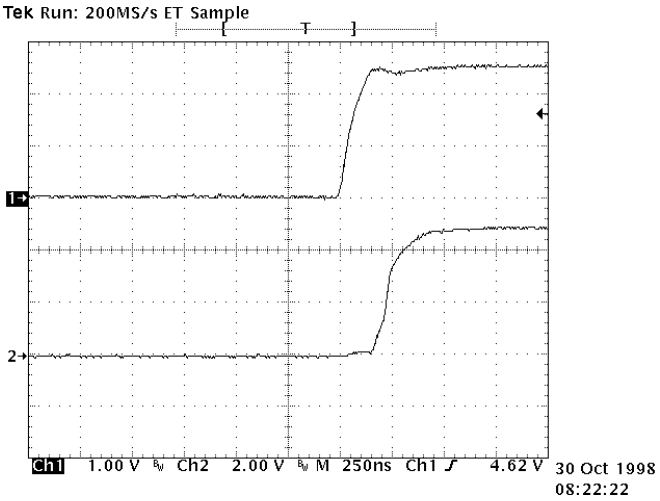
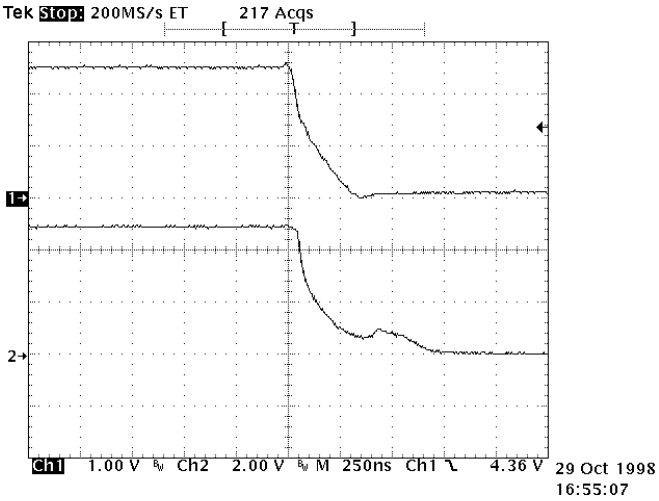
TYPICAL CHARACTERISTICS[1]

Drive High Delay



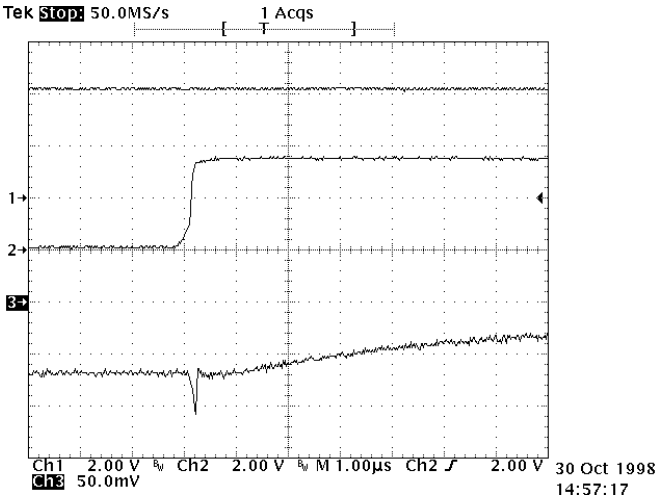
Trace 1: VIN stepping from 3V to 5.5V
Trace 2: DR going high at $V_{TH(HI)}$
t_{DH} < 225ns

Drive Low Delay



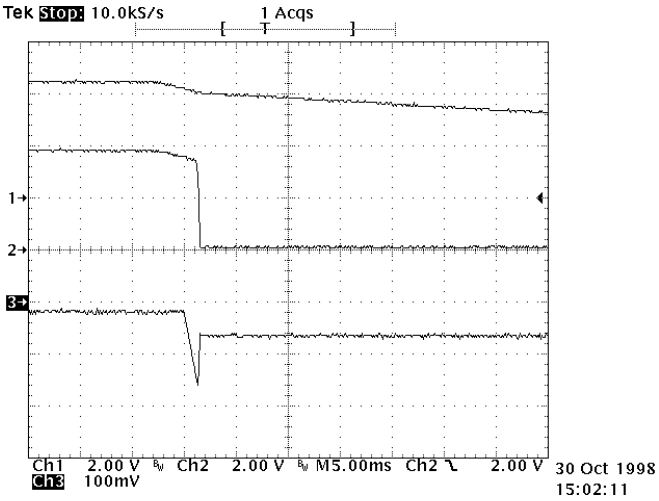
Trace 1: VIN stepping from 5.5V to 3V
Trace 2: DR going low at $V_{TH(LO)}$
t_{DL} < 125ns

VO(min) With VIN Rising[2]



Trace 1: VIN - 3A charging a 1500uF capacitor
Trace 2: DR going high at $V_{TH(HI)}$
Trace 3: VO, offset 3.3V. VO(min) = 3.19V

VO(min) With VIN Falling[2]



Trace 1: VIN - discharging a 1500uF capacitor
Trace 2: DR going low at $V_{TH(LO)}$
Trace 3: VO, offset 3.3V. VO(min) = 3.14V

NOTES:
(1) In Application Circuit on page 2.
(2) I_O = 200mA.

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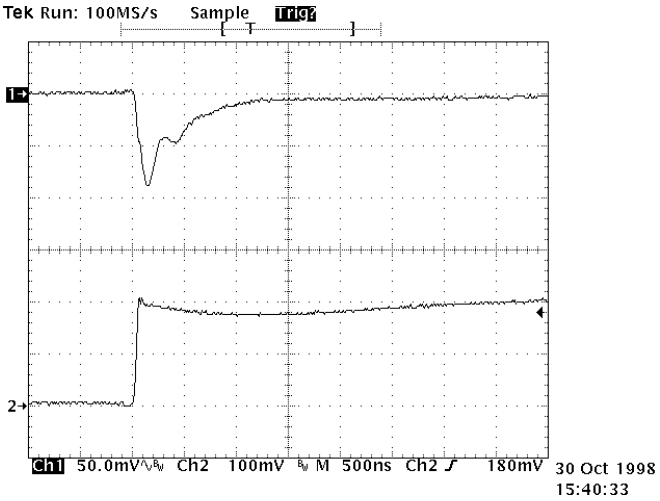
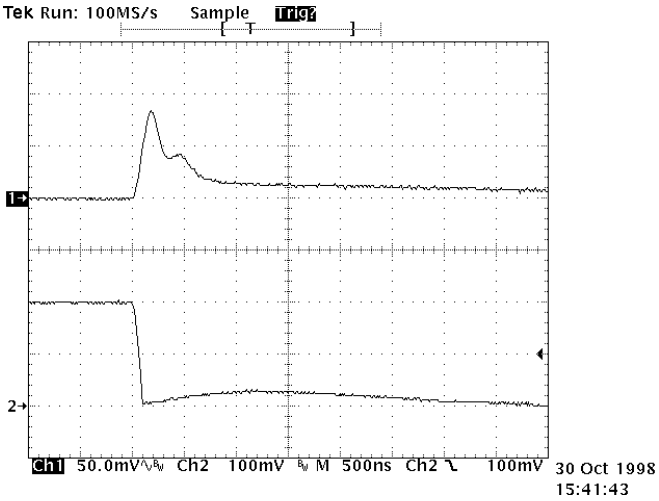
TYPICAL CHARACTERISTICS(1)

Load Transient Response



Trace 1: VO
Trace 2: I_O stepping from 0mA to 200mA

Load Transient Response



Trace 1: VO
Trace 2: I_O stepping from 200mA to 0mA

NOTE:
(1) In Application Circuit on page 2.

APPLICATIONS INFORMATION

Introduction

The SC1531 is intended for applications such as power managed PCI and network interface cards (NICs), where operation from a 3.3V VAUX supply may be required when the 5V supply has been shut down. It provides a very simple, low cost solution that uses very little pcb real estate. During regular operation, 3.3V power for the PCI card is provided by the SC1531's on-board low dropout regulator, generated from the 5V supply. When the 5V supply is removed and 3.3V VAUX is available, the SC1531 connects this supply directly to its output using a tiny SOT-23 external p-channel FET.

Component Selection

Output capacitors - Semtech recommends a minimum bulk capacitance of 4.7µF at the output, along with a 0.1µF ceramic decoupling capacitor. Increasing the bulk capacitance will improve the overall transient response. The device is very tolerant of capacitor value and ESR variations, in fact, any combination of capacitors with C ≥ 4.7µF and ESR < 1Ω is sufficient for stability. This target is easily met using surface mount ceramic or tantalum capacitors.

Input capacitors (5V) - Semtech recommends the use of a 4.7µF ceramic or tantalum capacitor plus a 0.1µF ceramic capacitor at the input. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, input droop due to load transients is reduced, improving load transient response.

Input capacitors (3.3V) - Semtech recommends decoupling this pin with a 0.1µF ceramic capacitor.

P-channel bypass FET - selection of the external FET is determined by two main requirements:
1) the FET has to have a very low gate threshold (typically ~1V) in order to be sufficiently turned on with $V_{GS} \leq 3.3V$.
2) the FET $R_{DS(ON)}$ must be low enough such that:

$$VAUX - (I_{O(MAX)} \bullet R_{DS(ON)}) \geq VO_{(MIN)}$$

Remember that at 125°C, $R_{DS(ON)}$ is generally 1.5x the value at 25°C.

Thermal Considerations

When operating from the 5V supply, the power dissipation in the SC1531 is approximately equal to the product of the output current and the input to output voltage differential:

$$P_D \approx (V_{IN} - V_{OUT}) \bullet I_{OUT}$$

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APPLICATIONS INFORMATION (Cont.)

The absolute worst-case dissipation is given by:

$$P_{D(MAX)} = (VIN_{(MAX)} - VO_{(MIN)}) \bullet I_{O(MAX)} + VAUX_{(MAX)} \bullet I_{Q(AUX)(MAX)}$$

Note that the $VAUX_{(MAX)}$ x $I_{Q(AUX)}$ term does not apply if VAUX is not available.
Inserting VIN = 5.5V, VO = 3.234V, I_O = 200mA, VAUX = 3.6V and $I_{Q(AUX)}$ = 2mA yields:

$$P_{D(MAX)} = 0.46\,W$$

Using this figure, we can calculate the maximum thermal impedance allowable to maintain $T_J \leq 125°C$:

$$R_{TH(J-A)(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{P_{D(MAX)}} = \frac{(125 - 70)}{0.46} = 120°C/W$$

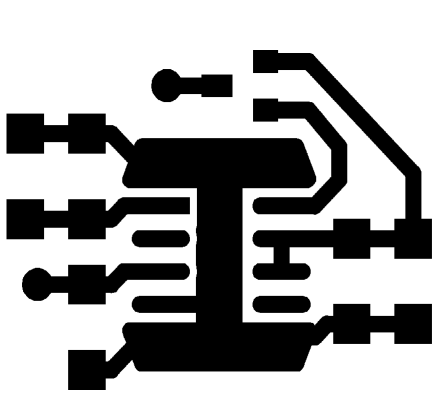
$R_{TH(J-C)(MAX)} = 47°C/W$, therefore $R_{TH(C-A)(MAX)} = 73°C/W$

This is readily achievable using pcb copper area to aid in conducting the heat away from the device (see below).
Heatsinking the bypass FET is not necessary - its power dissipation is given by:

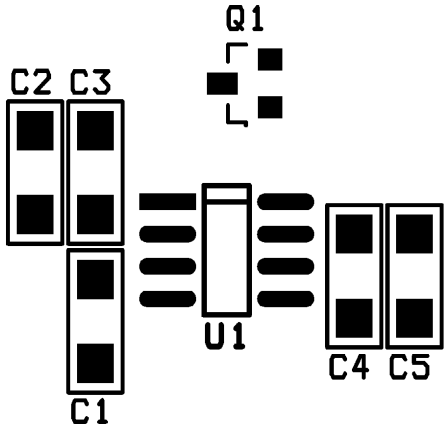
$$P_{D(MAX)} = (I_{O(MAX)})^2 \bullet R_{DS(ON)(MAX)}$$

For I_O = 200mA, and $R_{DS(ON)}$ = 0.6Ω, P_D = 24mW.

Layout Considerations
While layout for linear devices is generally not as critical as for a switching application, careful attention to detail will ensure reliable operation. See below for a sample layout.
1) Attaching the part to a larger copper footprint will enable better heat transfer from the device, especially on PCBs where there are internal ground and power planes.
2) Place the bulk and decoupling capacitors close to the device for optimal transient response.
3) If the SENSE lead is being used, route it to the load using a seperate trace from the main VO path. If it is not being used, connect to pin 7 as shown.
4) The external bypass FET is shown close to the device for convenience only. Since it is not being switched, longer gate drive traces can be used without problem.



Top Copper



Top Silk Screen

Fig. 1: Suggested pcb layout based upon Application Circuit on Page 2.

BILL OF MATERIALS

Qty.	Reference	Part/Description	Vendor	Notes
3	C1, C3, C5	0.1µF ceramic	Various	
2	C2, C4	4.7µF ceramic or tantalum	Various	
1	Q1	MGSF1P02ELT1	Motorola	P-channel, low gate threshold, ≤ 400mΩ
1	U1	SC1531CS	Semtech	

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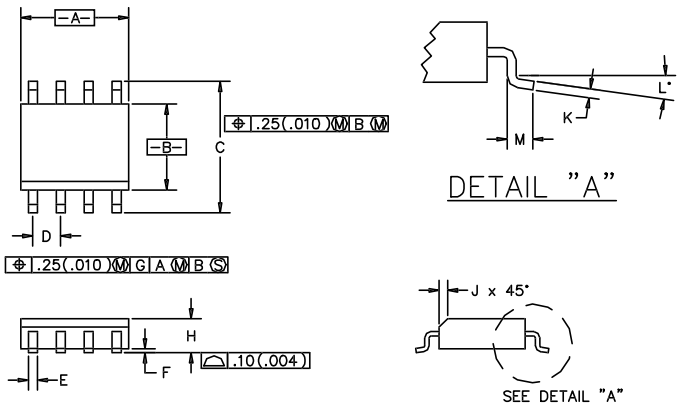
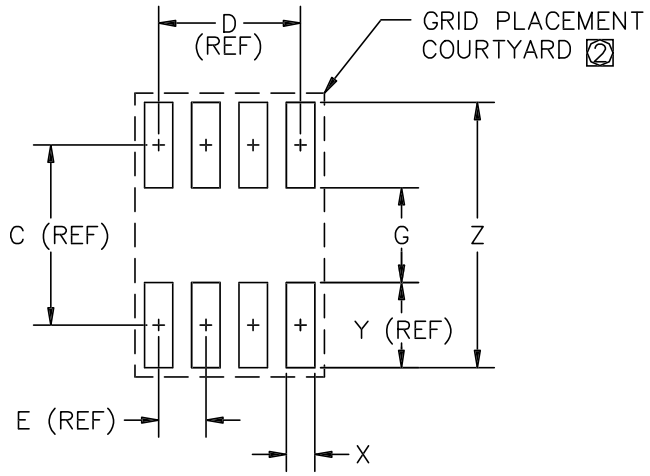
OUTLINE DRAWING



JEDEC
REF: MS-012AA

DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

LAND PATTERN SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS