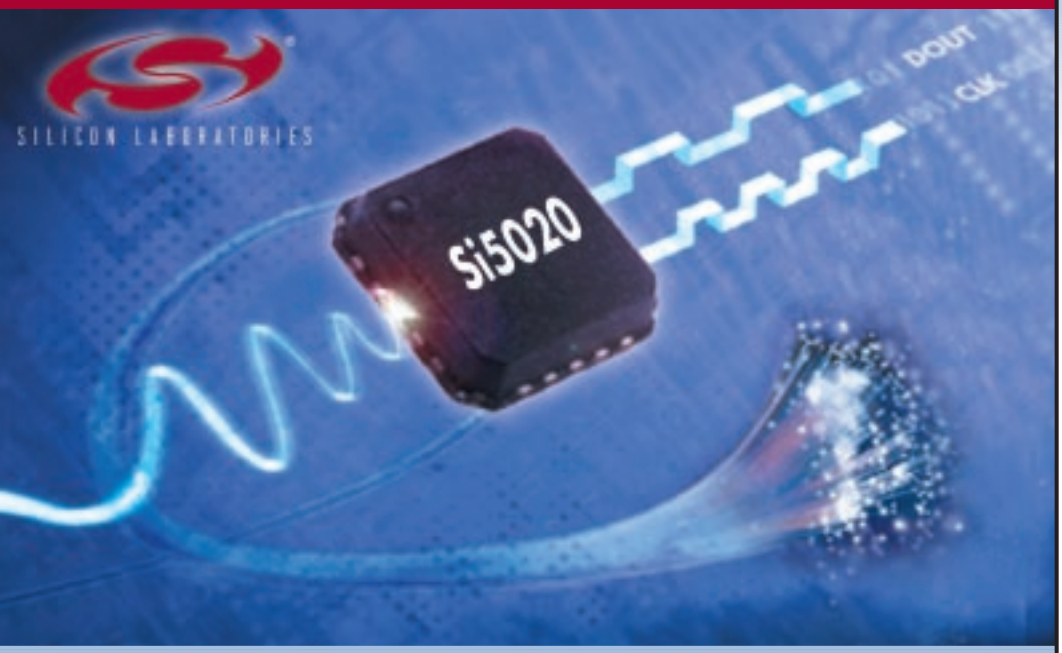
Si5020

MULTI-RATE SONET/SDH CLOCK AND DATA RECOVERY IC FOR OC-3/12/48, STM 1/4/16, GbE, AND 2.7 Gbps APPLICATIONS



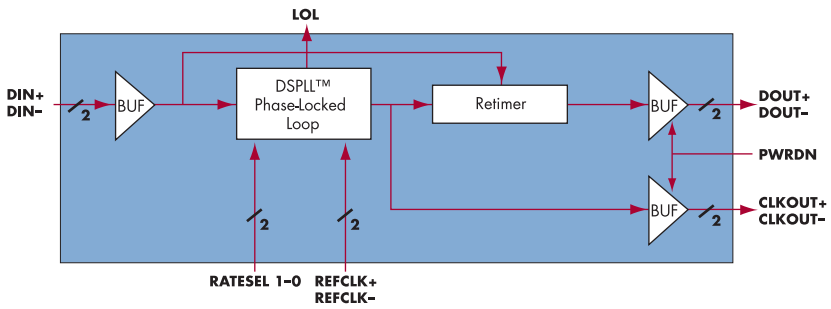
PRODUCT DESCRIPTION

The Si5020 is a fully integrated low-power clock and data recovery (CDR) IC designed for high-speed serial communication systems. It recovers timing information and data from a serial input at OC-3/12/48, STM-1/4/16, or Gigabit Ethernet (GbE) rates. Support for 2.7 Gbps data streams is also provided for OC-48/STM-16 applications that employ forward error correction (FEC).

The Si5020 utilizes Silicon Laboratories' proprietary DSPLL™ technology to eliminate the external loop filter components required by the phase-locked loop in traditional CDR implementations. This improves jitter performance by reducing the device's sensitivity to board-level noise. Application is further simplified by reducing external device configuration via integrated reference clock detection circuitry that automatically configures the device for operation with one of three common reference clock frequencies: 19 MHz, 77 MHz, and 155 MHz.

The Si5020 sets a new standard for small size and low power for high speed CDR ICs. It typically consumes 300 mW from a single 2.5 V supply and comes in a 20-pin micro leaded package (MLP).

Si5020 BLOCK DIAGRAM



FEATURES

- Multi-rate operation: OC-3/12/48, STM-1/4/16, Gigabit Ethernet, and 2.7 Gbps FEC
- Low power: 300 mW (TYP)
- Small footprint: 20-pin MLP, 4 mm x 4 mm outside dimension
- Proprietary DSPLL™ technology eliminates external loop filter components
- Exceeds SONET/SDH jitter specifications
- Automatic detection and configuration for 19, 77, and 155 MHz reference clocks
- Chip power down
- Loss-of-lock indication
- Single 2.5 V supply operation

APPLICATIONS

- SONET/SDH/ATM routers
- Add/drop multiplexers
- Digital cross connects
- SONET/SDH test equipment
- Optical transceiver modules
- SONET/SDH regenerators
- Board-level serial links

PRODUCTBRIEF

THE NEW STANDARD IN SMALL SIZE, LOW POWER, HIGH PERFORMANCE, MULTI-GIGABIT, PHYSICAL LAYER DEVICES.

SILICON LABORATORIES

SMALL SIZE, LOW POWER, INNOVATIVE PLL DESIGN

Industry's Lowest Power: The Si5020 is based on a single supply (2.5 V) design that consumes 50% less power than comparable multi-rate CDRs.

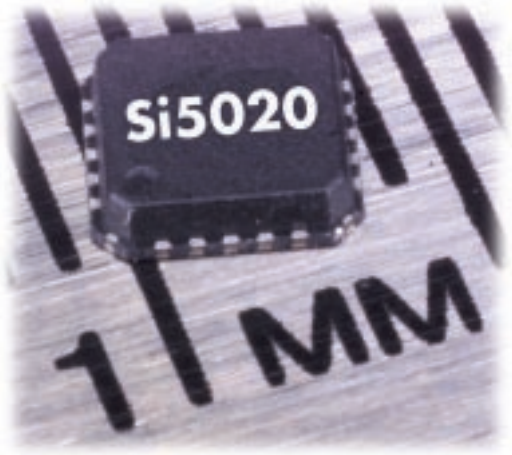
Proprietary DSPLL™ Technology: The phase-locked loop (PLL) within the Si5020 utilizes digital signal processing to eliminate the need for an external loop filter capacitor. By keeping all PLL circuitry internal, sensitive noise entry points are eliminated. This makes the PLL less susceptible to board-level interaction, thus helping to ensure optimal jitter performance over a wide range of board designs.

Fixed Rate Version Available: The Si5018 OC-48/STM-16 CDR with FEC is available for fixed-rate applications from OC-48/STM-16 data rates to 2.7 Gbps.

DEVELOPMENT TOOLS

For quick assessment of device performance, the Si5020-EVB evaluation kit is available. This kit supports a straightforward evaluation of device performance using industry standard test measurement equipment.

5x Smaller / 2x Lower Power



Si5020: 4 mm x 4 mm x 1 mm

INDUSTRY'S SMALLEST FOOTPRINT:

The Si5020 comes in a 20-pin micro leaded package (MLP) that has an outside dimension of 4 mm x 4 mm. This provides the Si5020 with a footprint that is five times smaller than comparable multi-rate CDRs.

EASY-TO-USE DESIGN

The Si5020 incorporates many features that simplify the design effort associated with multi-gigabit per second serial communication links.

For example, proprietary DSPLL technology enables robust operation over a wide range of board designs by eliminating the noise entry point introduced by the external loop filter capacitor found in traditional CDR designs. In addition, having the industry's smallest CDR footprint allows close placement of the Si5020 to the optical/electrical interface thus reducing EMI and noise problems caused by long high-speed PCB traces. To simplify device configuration, the Si5020 automatically detects the frequency of the supplied reference clock and self configures for operation with one of three common reference frequencies: 19, 77, or 155 MHz. Finally, low power consumption supports the trend toward high density designs by reducing the need for large power supplies and increased heat-handling capacity.

CONTACT INFORMATION

SILICON LABORATORIES

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PB:Si5020; REG-5,000-July00

ORDERING INFORMATION

Product	Description
Si5020-KM	Multi-Rate SONET/SDH Clock and Data Recovery IC, -5 to 85°C
Si5020-BM	Multi-Rate SONET/SDH Clock and Data Recovery IC, -40 to 85°C
Si5018-KM	OC-48/STM-16 Clock and Data Recovery IC with FEC, -5 to 85°C
Si5018-BM	OC-48/STM-16 Clock and Data Recovery IC with FEC, -40 to 85°C
Si5020-EVB	Evaluation Board for the Si5020
Si5018-EVB	Evaluation Board for the Si5018