# SONET/SDH/ATM OC-48 4-BIT TRANSCEIVER WITH CDR S3455

## FEATURES

- CMOS 0.18 micron technology
- Complies with Bellcore and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports OC-48 (2488.32 Mbps) with FEC
- Reference frequency of 155.52 MHz to 166.62 MHz
- Interface to LVDS and LVCMOS logic
- 4-bit LVDS data path
- 196 FC-PBGA
- Diagnostic loopback mode
- Supports line timing
- Lock detect
- Signal detect input
- Low jitter LVDS interface
- Internal FIFO to decouple transmit clocks
- Single 1.8 V supply
- Typical power under 1.0 W
- Available in die form

## APPLICATIONS

- Wavelength Division Multiplexing (WDM) equipment
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

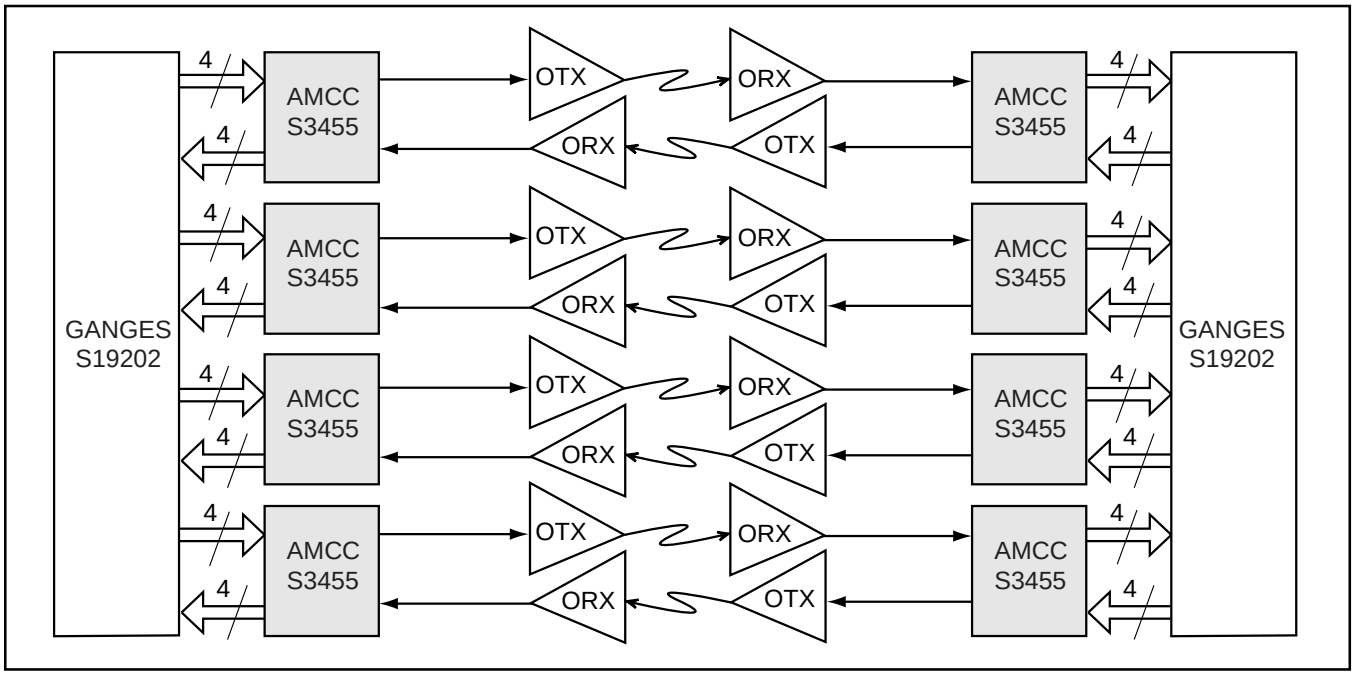
## GENERAL DESCRIPTION

The S3455 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-48 (2.488 Gbps – 2.670 Gbps) interface device. The S3455 receives an OC-48 scrambled Non-Return to Zero (NRZ) signal and recovers the clock from the data. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based WDM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency Phase-Locked Loop (PLL) on the S3455 transceiver chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 MHz (or 166.62 MHz) reference clock in support of existing system clocking schemes.

The low jitter LVDS interface is compliant with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3455 is packaged in a 196 FC-PBGA, offering designers a small package outline. The S3455 is also available in die form.

***Figure 1. System Block Diagram***



## S3455 OVERVIEW

The S3455 transceiver implements SONET/SDH serialization/deserialization, and transmission functions. The block diagram in Figure 2 shows the basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of management of the data stream and clock distribution throughout the front end. Table 1 shows the suggested interface devices for the S3455.

The S3455 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 4-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

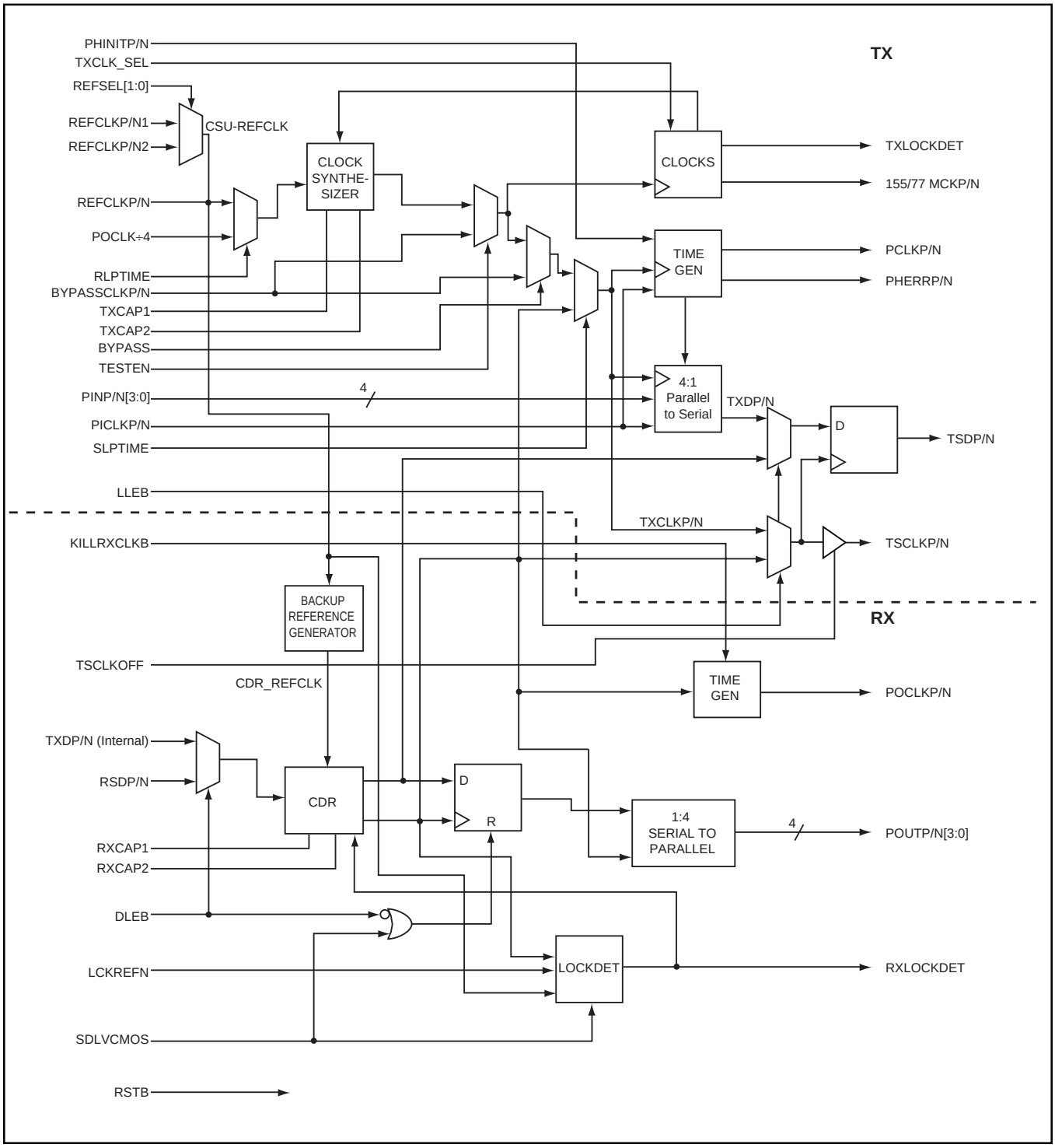
1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. 4-bit parallel output

Internal clocking and control functions are transparent to the user.

***Table 1. Sugggested Interface Devices***

| | | |
|---|---|---|
| AMCC | S19202 | STS-192 POS/ATM SONET/SDH Mapper |

***Figure 2. S3455 Transceiver Functional Block Diagram***



# S3455 TRANSCEIVER FUNCTIONAL DESCRIPTION

## TRANSMITTER OPERATION

The S3455 transceiver chip performs the serialization stage in the processing of a transmit SONET STS-48 data stream. It converts 4-bit parallel data to bit serial format at 2488.32 Mbps (or equivalent FEC rate).

A high-frequency bit clock can be generated from a 155.52 or 166.62 MHz frequency reference by using an integral frequency synthesizer consisting of a Phase-Locked Loop (PLL) circuit with a divider in the loop.

Diagnostic loopback (transmitter to receiver) and line loopback (receiver to transmitter) is provided. See Other Operating Modes.

### Clock Synthesizer

The clock synthesizer, shown in the block diagram in Figure 2, is a monolithic PLL that generates the serial output clock frequency locked to the input Reference Clock (CSU-REFCLK).

The REFCLKP/N1 or REFCLKP/N2 input must be generated from a crystal oscillator which has a frequency accuracy that meets the value stated in Table 7 in order for the Transmit Serial Clock (TSCLK) frequency to have the same accuracy required for operation in a SONET system. The REFCLK must meet the phase noise requirements shown in Figure 11 to meet the jitter generation specifications given in Table 7. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the CSU-REFCLK input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

### Timing Generator

The timing generation function, seen in Figure 2, provides a divide-by-4 rate version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PINP/N[3:0] data from the FIFO to the serial shift register.

The PCLK output is a divide-by-4 rate version of the transmit serial clock. PCLK is intended for use as a divide-by-4 clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3455 device.

The timing generator also produces a feedback reference clock to the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the CSU-REFCLK. The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the internal clock with that of the CSU-REFCLK.

***Table 2. Reference Jitter Limits***

| Operating Mode | Band Width | RMS Jitter |
|---|---|---|
| STS-48 | 12 kHz to 20 MHz | 5 ps |

### Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 2 is comprised of a FIFO and a parallel-to-serial register. The FIFO input latches the data from the PINP/N[3:0] bus on the rising edge of PICLK. The parallel-to-serial register is a loadable shift register which takes its parallel input from the FIFO output.

An internally generated divide-by-4 clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. The serial data is shifted out of the parallel-to-serial register at the TSCLK rate.

## FIFO

A FIFO is added to decouple the internal and external (PICLK) clocks. The internally generated divide-by-4 clock is used to clock out data from the FIFO. Phase Initialization (PHINIT) and Lock Detect (LOCKDET) are used to center or reset the FIFO. The PHINIT and LOCKDET signals will center the FIFO after the third PICLK pulse. This is in order to insure that PICLK is stable. This scheme allows the user to have an infinite PCLK to PICLK delay through the ASIC. Once the FIFO is centered, the PCLK to PICLK delay can have a maximum drift as specified by Table 16.

### FIFO Initialization

The FIFO can be initialized in one of the following three ways:

1. During power up, once the PLL has locked to the reference clock provided on the REFCLKP/N1 or REFCLKP/N2 pins, the LOCKDET will go active and initialize the FIFO.
2. When RSTB goes active, the entire chip is reset. This causes the PLL to go out of lock and thus the LOCKDET goes inactive. When the PLL reacquires the lock, the LOCKDET goes active and initializes the FIFO. Note: PCLK is held in reset when RSTB is active.
3. The user can also initialize the FIFO by raising PHINIT.

During normal operation, the incoming data is passed from the PICLK timing domain to the internally generated divide-by-4 clock domain. Although the frequency of PICLK and the internally generated clock are the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICLK and the internally generated clock. When a potential setup or hold time violation is detected, the phase error becomes active. When Phase Error (PHERR) conditions occur, PHINIT should be activated to recenter the FIFO (at least 2 PCLK periods). This can be done by connecting PHERR to PHINIT. When realignment occurs, up to ten bytes of data will be lost. The user can also take in the PHERR signal, process it and send an output to PHINIT in such a way that idle bytes are lost during the realignment process. PHERR will go inactive when the realignment is complete.

## RECEIVER OPERATION

The S3455 transceiver chip provides the first stage of the digital processing of a receive SONET STS-48 bit-serial stream. It converts the bit-serial 2.488 Gbps (or equivalent FEC rate) data stream into a 4-bit parallel data format. A loopback mode is provided for diagnostic loopback (transmitter to receiver). A line loopback (receiver to transmitter) is also provided.

### Clock Recovery

The S3455 clock recovery device performs the clock recovery function for SONET OC-48 serial data links. The chip extracts the clock from the serial data inputs and provides retimed clock and data outputs. A 155.52 MHz or 166.62 MHz reference clock is used for phase locked loop start up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

The clock recovery generates a clock that is at the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (CDR-REFCLK) that the PLL locks onto when data is lost. If the frequency of the incoming signal varies by a value greater than that stated in Table 7, with respect to CDR-REFCLK, the PLL will be declared out of lock, and the PLL will lock to the reference clock. The assertion of LVCMOS Signal Detect will also cause an out-of-lock condition.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 3.

### Lock Detect

The S3455 contains a lock detect circuit which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by a value greater than that stated in Table 7, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within the values stated in Table 7, the PLL will be declared in lock and the lock detect output will go active. The assertion of SDLVCMOS will also cause an out of lock condition.

### Serial-to-Parallel Converter

The serial-to-parallel converter consists of two 4-bit registers. The first is a serial-in, parallel-out shift register, which performs the serial-to-parallel conversion clocked by the clock recovery block. On the falling edge of the Parallel Output Clock (POCLK), the data in the parallel register is transferred to an output parallel register which drives POUTP/N[3:0].

## OTHER OPERATING MODES

### Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data from the transmitter is routed to the serial-to-parallel block in place of the Receiver Serial Data (RSD). Transmit Serial Data/Transmit Serial Clock (TSD/TSCLK) outputs are active. DLEB takes precedence over SDLVCMOS.

### Line Loopback

The line loopback circuitry selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable (LLEB) input is inactive, it selects the data and clock from the parallel to serial converter block. When LLEB is active, it forces the output data multiplexer to select the data and clock from the RSD and Receive Serial Clock (RSCLK) inputs, and a receive-to-transmit loopback can be established at the serial data rate.

### Loop Timing

In Serial Loop Timing (SLPTIME) mode, the clock synthesizer PLL of the S3455 is bypassed, and the timing of the entire transmitter section is controlled by the Receive Serial Clock, RSCLKP/N. This mode is entered by setting the SLPTIME input to a LVCMOS high level.

In this mode, the CSU-REFCLK input is not used. It should be carefully noted that the internal PLL and CDR PLL continue to operate in this mode, and continue as the source for the 155/77MCK and RSD/RSCLK, and if these signals are being used, the CSU-REFCLK input must be properly driven.

In Reference Loop Timing (RLPTIME) mode, the Parallel Output Clock (POCLK) from the receiver is used as the reference clock to the transmitter. In this mode, CSU-REFCLK input is not used. The 155/77MCK are generated from the POCLK in this operating mode.

## CDR CHARACTERISTICS

### Performance

The S3455 CDR PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used as specified.

### Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 3.

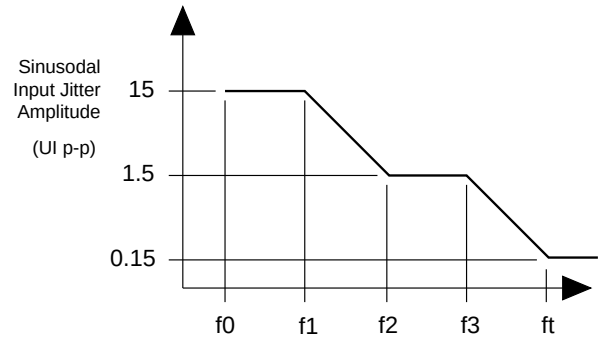
### Jitter Transfer

The jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 4. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 3 be applied.

### Jitter Generation

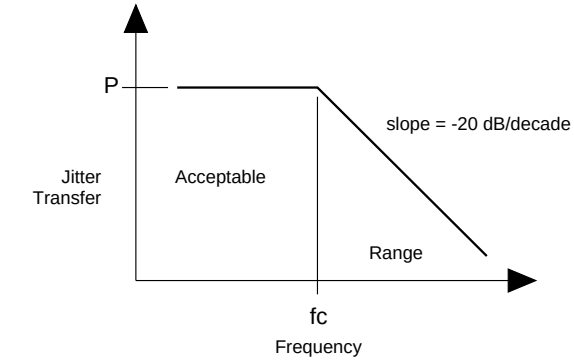
The jitter generation of the serial clock and serial data outputs shall not exceed the value specified in Table 7 when a serial data input with no jitter is presented to the serial data inputs. The REFCLK input must meet the phase noise requirements shown in Figure 11 to meet the jitter generation value specified in Table 7.

***Figure 3. Input Jitter Tolerance Specification***




| OC/STS Level | f0 (Hz) | f1 (Hz) | f2 (Hz) | f3 (kHz) | ft (kHz) |
|---|---|---|---|---|---|
| 48 | 10 | 600 | 6000 | 100 | 1000 |

***Figure 4. Jitter Transfer Specification***




| OC/STS Level[1,2] | fc (kHz) | P (dB) |
|---|---|---|
| 48 | 2000 | 0.1 |

1. Bellcore Specifications: GR-253- CORE, Issue 2, December 1995.
2. ITU-T Recommendations: G.958.

***Table 3. S3455 Transmitter Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| PINP0<br>PINN0<br>PINP1<br>PINN1<br>PINP2<br>PINN2<br>PINP3<br>PINN3 | LVDS | I | L9<br>K9<br>M10<br>N10<br>P9<br>N9<br>N11<br>P11 | Parallel Input Data, aligned to the PICLK parallel input clock. PINP/N[3] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PINP/N[0] is the least significant bit (corresponding to bit 4 of each PCM word, the last bit transmitted). PINP/N[3:0] is sampled on the rising edge of PICLK. Internally terminated. |
| PICLKP<br>PICLKN | LVDS | I | K11<br>L11 | Parallel Input Clock. A divide-by-4, nominally 50% duty cycle input clock, to which PINP/N[3:0] is aligned. PICLK is used to transfer the data on the PINP/N inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PINP/N[3:0]. Internally terminated. |
| TXCAP1<br>TXCAP2 | Analog | I | F14<br>G14 | Transmit Loop Filter Capacitor. The external loop filter capacitor and resistors are connected to these pins. See Figure 19. |
| PHINITP<br>PHINITN | LVDS | I | N8<br>M8 | Phase Initialization. Rising edge will realign internal timing. Internally terminated. |
| TXCLK_SEL | LVCMOS | I | D4 | Transmit Clock Select. Used to select between the 155.52 MHz or 77.76 MHz clock on the 155/77MCKP/N output. A low on TXCLK_SEL selects 155.52 MHz output clock, and a high on TXCLK_SEL selects 77.76 MHz output clock. |
| TSCLKOFF | LVCMOS | I | C11 | Transmit Serial Clock Off. This input should be pulled low in the default mode. When pulled high, it shuts off the TSCLK macro to save power. |
| TSDP<br>TSDN | Diff. CML | O | A8<br>A7 | Transmit Serial Data. Differential CML serial data stream signals, normally connected to an optical transmitter module. |
| TSCLKP<br>TSCLKN | Diff. CML | O | A12<br>A11 | Transmit Serial Clock that can be used to retime the TSD signal. |
| PCLKP<br>PCLKN | LVDS | O | L6<br>K6 | Parallel Clock. A reference clock generated by dividing the internal bit clock by 4. It is normally used to coordinate 4-bit wide transfers between upstream logic and the S3455 device. |
| PHERRP<br>PHERRN | LVDS | O | J8<br>K8 | Phase Error. Active high. Pulses high during each PCLK cycle for which there is a potential setup/hold timing violation between the internal byte clock and PICLK timing domains. |
| TXLOCKDET | LVCMOS | O | K2 | Transmit PLL Lock Detect. Goes High after the PLL has locked to the clock provided on the CSU-REFCLK. TXLOCKDETB is an asynchronous output. |

***Table 4. S3455 Receiver Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| RSDP<br>RSDN | Diff.<br>CML | I | A3<br>A4 | Receive Serial Data stream signals normally connected to an optical receiver module. Internally biased and terminated. |
| SDLVCMOS | LVCMOS | I | C5 | LVCMOS Signal Detect. Active High. A single-ended LVCMOS input to be driven by the external optical receiver module to indicate a loss of received optical power. When LVCMOS is inactive, the data on the POUTP/N[15:0] pins will be internally forced to a constant state (one or zero), and any transition on RSDP/N will be squelched. When LVCMOS is active, data on the RSDP/N pins will be processed normally. |
| RXCAP1<br>RXCAP2 | Analog | I | F1<br>G1 | Receive Loop FIlter Capacitor. The external loop filter capacitor and resistors are connected to these pins. See Figure 19. |
| POUTP0<br>POUTN0<br>POUTP1<br>POUTN1<br>POUTP2<br>POUTN2<br>POUTP3<br>POUTN3 | LVDS | O | N4<br>P4<br>K4<br>L4<br>N5<br>M5<br>P6<br>N6 | Parallel Data Output bus, aligned to the Parallel Output Clock (POCLK). POUTP/N[3] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUTP/N[0] is the least significant bit. POUTP/N[3:0] is updated on the falling edge of POCLK. |
| POCLKP<br>POCLKN | LVDS | O | J5<br>K5 | Parallel Output Clock. A divide-by-4, nominally 50% duty cycle, parallel output clock that is aligned to POUTP/N[3:0] 4-bit parallel output data. POUTP/N[3:0] is updated on the falling edge of POCLK. |
| RXLOCKDET | LVCMOS | O | K1 | Receive PLL Lock Detect. Clock recovery indicator that is set high when the internal clock recovery has locked onto the incoming data stream. RXLOCKDET is an asynchronous output. |
| LCKREFN | LVCMOS | I | D3 | Lock to Reference. Active Low. When active, the serial clock output will be forced to lock to the local reference clock input. |

***Table 5. S3455 Common Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| REFCLKP1<br>REFCLKN1<br>REFCLKP2<br>REFCLKN2 | LVDS | I | K14<br>K13<br>M14<br>M13 | Reference Clocks. Used as the reference for the internal bit clock frequency synthesizer. Internally terminated and biased. REFCLKP/N1 can be connected to 155.52 MHz crystal (for OC-48 non-FEC rate) and REFCLKP/N2 can be connected to a 166.63 MHz crystal (for OC-48 FEC rates). The REFCLKP/N1 and REFCLKP/N2 can be selected by REFSEL[1:0] to switch between the FEC and the non-FEC rates. |
| REFSEL1<br>REFSEL0 | LVCMOS | I | D5<br>C9 | Reference Clock Select. Selects between the REFCLKP/N 1 and REFCLKP/N2. (See Table 18.) |
| DLEB | LVCMOS | I | B5 | Diagnostic Loopback Enable. Active low. Selects diagnostic loopback. When DLEB is inactive, the S3455 device uses the primary data (RSD) input. When active, the S3455 device uses the diagnostic loopback data from the transmitter. TSD/TSCLK is active in DLEB. |
| LLEB | LVCMOS | I | C6 | Line Loopback Enable. Active low. Selects line loopback. When LLEB is active, the S3455 will route the data from the RSD/RSCLK inputs to the TSD/TSCLK outputs. |
| KILLRXCLKB | LVCMOS | I | D11 | Kill Receive Clock Input. Active low. For normal operation, KILLRXCLKB is high. When this input is low, it will force the POCLK output to a logic "0" state. |
| SLPTIME | LVCMOS | I | C4 | Serial Clock Loop Time Select input. Active high. When active, SLPTIME enables the recovered clock from the receive section to be used in place of the synthesized transmit clock. |
| RLPTIME | LVCMOS | I | D12 | Reference Clock Loop Time Select input. Active high. When active, RLPTIME enables POCLK from the receiver to be used as the reference clock input to the transmitter. |
| RSTB | LVCMOS | I | B2 | Master Reset. Reset input for the device. Active low for a duration of five REFCLK cycles. During reset, all clocks are disabled. |
| TESTEN | LVCMOS | I | C2 | Test Enable. Used for production testing. Low for normal operation. |
| 155/77MCKP<br>155/77MCKN | LVDS | O | M1<br>M2 | 155.52/77.76 MHz clock output from the clock synthesizer. |

***Table 5. S3455 Common Pin Assignment and Descriptions (Continued)***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| BYPASSCLKP<br>BYPASSCLKN | Diff.<br>CML | I | C14<br>D14 | Bypass Clock. Provides an alternative serial clock bypassing the internal VCO. Internally biased and terminated. |
| BYPASS | LVCMOS | I | C12 | Active high. Selects between BYPASS clock and the VCO clock. |
| NC | | | L2, L3 | Not Connected. Do not connect these pins to power or ground. |
| VSS | GND | | A1, A14, C3, C8, D8, D10, E8, H11, M12, P2, P14 | Ground (0 V) |
| VSS_RSD | GND | | A5, B4 | Ground (0 V) |
| VSS_TSD | GND | | B6, B8, B9 | Ground (0 V) |
| VSS_BYPASS | GND | | B14, D13 | Ground (0 V) |
| VSS_TSCLK | GND | | B10, B12, B13 | Ground (0 V) |
| VSS_CMOS | GND | | D1, D2, D6 | Ground (0 V) |
| VSS_RX | GND | | E5, E6, E7, F6, F7, G6 | Ground (0 V) |
| VSS_TX | GND | | F8, F9, G7, G8, G9, H7 | Ground (0 V) |
| VSS_LVDS | GND | | H8, H9, J6, J9, K7, L1, L5, L8, L10, L12, M3, M7, N2, P1, P3, P5, P7, P8, P10, P12, P13 | Ground (0 V) |
| VSS_REFCLK | GND | | L14, N14 | Ground (0 V) |
| AVSS_RX | GND | | E1, E2, E3, F2, G2, H1, H2, J1 | Ground (0 V) |
| AVSS_TX | GND | | E13, E14, F13, G13, H13, H14, J14 | Ground (0 V) |

***Table 5. S3455 Common Pin Assignment and Descriptions (Continued)***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| VDD | +1.8 V | | A2, B1, C7, C10, D9 | Power Supply |
| VDD_RSD | +1.8 V | | B3 | Power Supply |
| VDD_TSD | +1.8 V | | A6, A9, B7 | Power Supply |
| VDD_BYPASS | +1.8 V | | C13 | Power Supply |
| VDD_TSCLK | +1.8 V | | A10, A13, B11 | Power Supply |
| VDD_CMOS | +1.8 V | | C1, D7 | Power Supply |
| VDD_RX | +1.8 V | | F4, F5, G5, H4, H5, H6 | Power Supply |
| VDD_TX | +1.8 V | | E9, E10, F10, F11, G10, G11 | Power Supply |
| VDD_LVDS | +1.8 V | | H10, J4, J7, J10, J11, K3, K10, K12, L7, M4, M6, M9, M11, N1, N3, N7, N12 | Power Supply |
| AVDD_RX | +1.8 V | | E4, F3, G3, G4, H3, J2, J3 | Power Supply |
| AVDD_TX | +1.8 V | | E11, E12, F12, G12, H12, J12, J13 | Power Supply |
| VDD_REFCLK | +1.8 V | | L13, N13 | Power Supply |

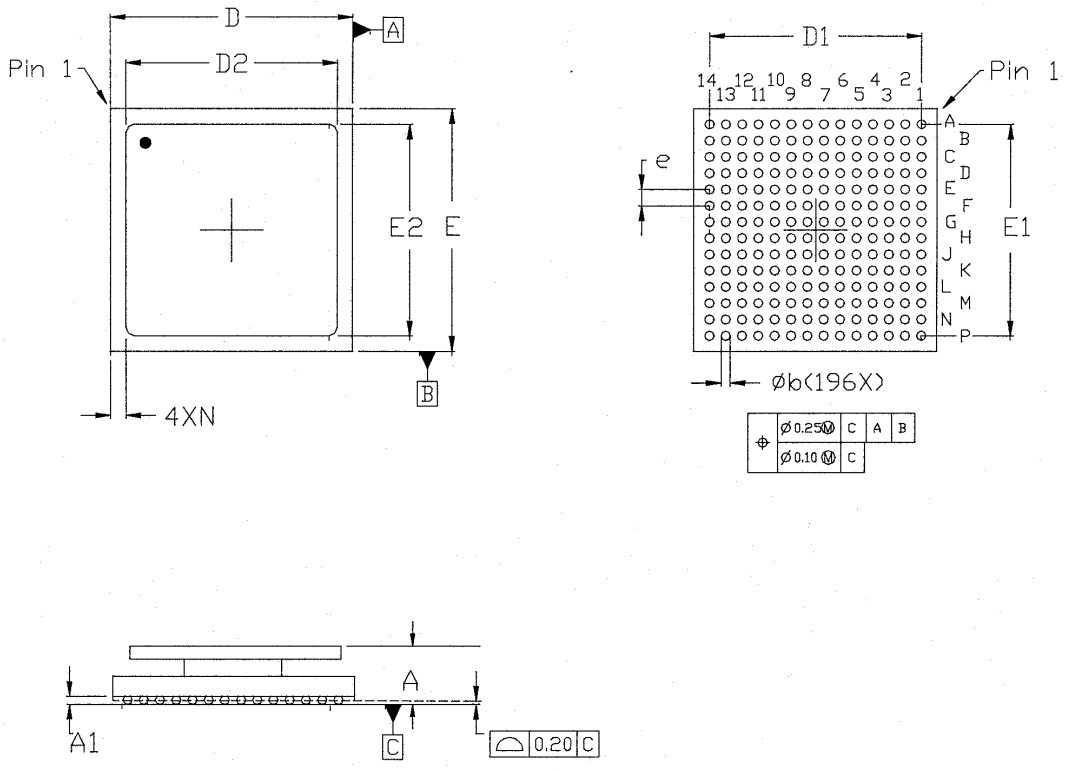
***Figure 5. S3455 Pinout BottomView***

| | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | VDD_ TSCLK | TSCLKP | TSCLKN | VDD_ TSCLK | VDD_TSD | TSDP | TSDN | VDD_TSD | VSS_RSD | RSDN | RSDP | VDD | VSS |
| B | VSS_ BYPASS | VSS_ TSCLK | VSS_ TSCLK | VDD_ TSCLK | VSS_ TSCLK | VSS_TSD | VSS_TSD | VDD_TSD | VSS_TSD | DLEB | VSS_RSD | VDD_RSD | RSTB | VDD |
| C | BYPASS-CLKP | VDD_ BYPASS | BYPASS | TSCLK-OFF | VDD | REFSEL0 | VSS | VDD | LLEB | SDLV CMOS | SLPTIME | VSS | TESTEN | VDD_ CMOS |
| D | BYPASS-CLKN | VSS_ BYPASS | RLP-TIME | KILLRX-CLKB | VSS | VDD | VSS | VDD_ CMOS | VSS_ CMOS | REFSEL1 | TXCLK_ SEL | LCKREFN | VSS_ CMOS | VSS_ CMOS |
| E | AVSS_TX | AVSS_TX | AVDD_TX | AVDD_TX | VDD_TX | VDD_TX | VSS | VSS_RX | VSS_RX | VSS_RX | AVDD_RX | AVSS_RX | AVSS_RX | AVSS_RX |
| F | TXCAP1 | AVSS_TX | AVDD_TX | VDD_TX | VDD_TX | VSS_TX | VSS_TX | VSS_RX | VSS_RX | VDD_RX | VDD_RX | AVDD_RX | AVSS_RX | RXCAP1 |
| G | TXCAP2 | AVSS_TX | AVDD_TX | VDD_TX | VDD_TX | VSS_TX | VSS_TX | VSS_TX | VSS_RX | VDD_RX | AVDD_RX | AVDD_RX | AVSS_RX | RXCAP2 |
| H | AVSS_TX | AVSS_TX | AVDD_TX | VSS | VDD_ LVDS | VSS_ LVDS | VSS_ LVDS | VSS_TX | VDD_RX | VDD_RX | VDD_RX | AVDD_RX | AVSS_RX | AVSS_RX |
| J | AVSS_TX | AVDD_TX | AVDD_TX | VDD_ LVDS | VDD_ LVDS | VSS_ LVDS | PHERRP | VDD_ LVDS | VSS_ LVDS | POCLKP | VDD_ LVDS | AVDD_RX | AVDD_RX | AVSS_RX |
| K | REFCLKP1 | REFCLKN1 | VDD_ LVDS | PICLKP | VDD_ LVDS | PINN0 | PHERRN | VSS_ LVDS | PCLKN | POCLKN | POUTP1 | VDD_ LVDS | TXLOCK-DET | RXLOCK-DET |
| L | VSS_ REFCLK | VDD_ REFCLK | VSS_ LVDS | PICLKN | VSS_ LVDS | PINP0 | VSS_ LVDS | VDD_ LVDS | PCLKP | VSS_ LVDS | POUTN1 | NC | NC | VSS_ LVDS |
| M | REFCLKP2 | REFCLKN2 | VSS | VDD_ LVDS | PINP1 | VDD_ LVDS | PHINITN | VSS_ LVDS | VDD_ LVDS | POUTN2 | VDD-LVDS | VSS_ LVDS | 155/77 MCKN | 155/77 MCKP |
| N | VSS_ REFCLK | VDD_ REFCLK | VDD_ LVDS | PINP3 | PINN1 | PINN2 | PHINITP | VDD_ LVDS | POUTN3 | POUTP2 | POUTP0 | VDD_ LVDS | VSS_ LVDS | VDD_ LVDS |
| P | VSS | VSS_ LVDS | VSS_ LVDS | PINN3 | VSS_ LVDS | PINP2 | VSS_ LVDS | VSS_ LVDS | POUTP3 | VSS_ LVDS | POUTN0 | VSS_ LVDS | VSS | VSS_ LVDS |

***Figure 6. S3455 Pinout Top View***

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VSS | VDD | RSDP | RSDN | VSS_RSD | VDD_TSD | TSDN | TSDP | VDD_TSD | VDD_ TSCLK | TSCLKN | TSCLKP | VDD_ TSCLK | VSS | A |
| VDD | RSTB | VDD_RSD | VSS_RSD | DLEB | VSS_TSD | VDD_TSD | VSS_TSD | VSS_TSD | VSS_ TSCLK | VDD_ TSCLK | VSS_ TSCLK | VSS_ TSCLK | VSS_ BYPASS | B |
| VDD_ CMOS | TESTEN | VSS | SLPTIME | SDLV CMOS | LLEB | VDD | VSS | REFSEL0 | VDD | TSCLK-OFF | BYPASS | VDD_ BYPASS | BYPASS-CLKP | C |
| VSS_ CMOS | VSS_ CMOS | LCKREFN | TXCLK_ SEL | REFSEL1 | VSS_ CMOS | VDD_ CMOS | VSS | VDD | VSS | KILLRX-CLKB | RLP-TIME | VSS_ BYPASS | BYPASS-CLKN | D |
| AVSS_RX | AVSS_RX | AVSS_RX | AVDD_RX | VSS_RX | VSS_RX | VSS_RX | VSS | VDD_TX | VDD_TX | AVDD_TX | AVDD_TX | AVSS_TX | AVSS_TX | E |
| RXCAP1 | AVSS_RX | AVDD_RX | VDD_RX | VDD_RX | VSS_RX | VSS_RX | VSS_TX | VSS_TX | VDD_TX | VDD_TX | AVDD_TX | AVSS_TX | TXCAP1 | F |
| RXCAP2 | AVSS_RX | AVDD_RX | AVDD_RX | VDD_RX | VSS_RX | VSS_TX | VSS_TX | VSS_TX | VDD_TX | VDD_TX | AVDD_TX | AVSS_TX | TXCAP2 | G |
| AVSS_RX | AVSS_RX | AVDD_RX | VDD_RX | VDD_RX | VDD_RX | VSS_TX | VSS_ LVDS | VSS_ LVDS | VDD_ LVDS | VSS | AVDD_TX | AVSS_TX | AVSS_TX | H |
| AVSS_RX | AVDD_RX | AVDD_RX | VDD_ LVDS | POCLKP | VSS_ LVDS | VDD_ LVDS | PHERRP | VSS_ LVDS | VDD_ LVDS | VDD_ LVDS | AVDD_TX | AVDD_TX | AVSS_TX | J |
| RXLOCK-DET | TXLOCK-DET | VDD_ LVDS | POUTP1 | POCLKN | PCLKN | VSS_ LVDS | PHERRN | PINN0 | VDD_ LVDS | PICLKP | VDD_ LVDS | REFCLKN1 | REFCLKP1 | K |
| VSS_ LVDS | NC | NC | POUTN1 | VSS_ LVDS | PCLKP | VDD_ LVDS | VSS_ LVDS | PINP0 | VSS_ LVDS | PICLKN | VSS_ LVDS | VDD_ REFCLK | VSS_ REFCLK | L |
| 155/77 MCKP | 155/77 MCKN | VSS_ LVDS | VDD-LVDS | POUTN2 | VDD_ LVDS | VSS_ LVDS | PHINITN | VDD_ LVDS | PINP1 | VDD_ LVDS | VSS | REFCLKN2 | REFCLKP2 | M |
| VDD_ LVDS | VSS_ LVDS | VDD_ LVDS | POUTP0 | POUTP2 | POUTN3 | VDD_ LVDS | PHINITP | PINN2 | PINN1 | PINP3 | VDD_ LVDS | VDD_ REFCLK | VSS_ REFCLK | N |
| VSS_ LVDS | VSS | VSS_ LVDS | POUTN0 | VSS_ LVDS | POUTP3 | VSS_ LVDS | VSS_ LVDS | PINP2 | VSS_ LVDS | PINN3 | VSS_ LVDS | VSS_ LVDS | VSS | P |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

***Figure 7. Package Drawing***




DIMENSIONS (are in millimeters)

| UNIT | $A_1$ | A | D | $D_1$ | $D_2$ | E | $E_1$ | $E_2$ | b | e | N |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MIN | 0.40 | | 14.80 | 12.90 | 12.80 | 14.80 | 12.90 | 12.80 | 0.50 | 1.00 BSC. | 0.75 |
| NOM | 0.50 | | 15.00 | 13.00 | 13.00 | 15.00 | 13.00 | 13.00 | 0.60 | | 1.00 |
| MAX | 0.60 | 2.97 | 15.20 | 13.10 | 13.20 | 15.20 | 13.10 | 13.20 | 0.70 | | 1.25 |

***Table 6. Thermal Management***

| Device | Max Package Power | Θja |
|---|---|---|
| S3455 | 1.25 W | 34.0˚ C/W – Still Air |

Note: The S3455 requires 200 LFMP airflow for an industrial operating temperature of 85°C/W. No airflow or heatsink is required for a commercial operating temperature of 70°C.

***Table 7. Performance Specifications***

| Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| VCO Frequency CSU and CDR | 2.488 | | 2.67 | GHz | |
| Jitter Generation (CSU) | | | 0.007 | UI (rms) | Note: Output jitter measured at SONET operating rate using appropriate filter, rms jitter, in lock. |
| Reference Clock (REFCLKP/N1 or REFCLKP/N2) Frequency Tolerance | -100 | | +100 | ppm | ± 20 is required to meet SONET output frequency specification. |
| Reference Clock (REFCLKP/N1 or REFCLKP/N2) Input Duty Cycle | 45 | | 55 | % | |
| Reference Clock (REFCLKP/N1 or REFCLKP/N2) Rise and Fall Times | | | 1.5 | ns | 10% to 90% of amplitude. |
| Acquisition Time (CDR) 155.52 MHz CDR_REFCLK | | | 250 | µsec | Minimum transition density of 20%. Guaranteed but not tested. With device already powered up and valid ref. clk. |
| Frequency difference at which the PLL goes out of lock (CDR_REFCLK compared to the divided down VCO clock) - CDR | 450 | 600 | 770 | ppm | Guaranteed but not tested. |
| Frequency difference at which the receive PLL goes into lock (CDR_REFCLK compared to the divided down VCO clock) - CDR | 220 | 300 | 390 | ppm | Guaranteed but not tested. |
| Jitter Generation (CDR) with VCO locked to SERDATIP/N | | | 0.01 | UI (rms) | Note: This mode is valid in the SLPTIME, RLPTIME and LLEB mode only. |
| (REFCLKP/N1/REFCLKP/N2) to PCLK Delay | | | 6.43 | ns | Guaranteed but not tested. |
| RSTB to TXLOCKDET Delay | | | 500 | µs | Guaranteed but not tested. |
| Bit Latency - Number of clock cycles after PINP/N[X] appears at TSDP/N | | | 20 | REFCLK Cycles | Guaranteed but not tested. |

***Table 8. Jitter Tolerance Specifications***

| Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| Jitter Tolerance<br>STS-48 | 0.4 | 0.5 | | UI | 1 MHz < f < 20 MHz<br>Data Pattern = $2^7$-1 PRBS |

***Table 9. Absolute Maximum Ratings***

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Storage Temperature | -65 | | 150 | ˚C |
| Voltage on 1.8 Volt Power pins with respect to GND | -0.2 | | +2.0 | V |
| Voltage on any LVDS Input Pin | 0 | | VDD_LVDS | V |

**ESD Ratings**

The S3455 is rated to the following voltages based on the human body model:

1. All pins are rated above 1000 V.

***Table 10. Recommended Operating Conditions***

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Ambient Temperature Under Bias[1] | -40 | | 85 | ˚C |
| Voltage on 1.8 Volt Power planes with respect to GND | 1.71 | 1.8 | 1.89 | V |
| Voltage on any LVDS Input Pin | 0 | | VDD_LVDS | V |
| Voltage on any LVCMOS Input Pin | 0 | | VDD_CMOS | V |
| 1.8 Volts Supply Current | | 555 | 700 | mA |

1. 200 LFMP airflow is required for an industrial operating temperature of 85°C/W. No airflow is required for a commercial operating temperature of 70°C.

***Table 11. LVCMOS Input/Output DC Characteristics***

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | VDD_CMOS -0.4 | | | V | |
| $V_{IL}$ | Input Low Voltage | | | 0.4 | V | |
| $I_{IH}$ | Input High Current | | | 15 | µA | |
| $I_{IL}$ | Input Low Current | | | 15 | µA | |
| $V_{OH}$ | Output High Voltage | VDD_CMOS -0.2 | | | V | IOH = -200 µA |
| $V_{OL}$ | Output Low Voltage | | | 0.2 | V | IOL = 200 µA |

***Table 12. LVDS Input DC Characteristics***

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | 0.775 | | 1.42 | V | |
| $V_{IH}$ | Input High Voltage | 0.96 | | 1.80 | V | |
| $V_{ICM}$ | Receiver Common Mode Range | 0.90 | 1.25 | 1.56 | V | |
| $V_{INSINGLE}$ | Single Ended Input Voltage Swing | 200 | | 650 | mV | |
| $V_{INDIFF}$ | Differential Input Voltage Swing | 400 | | 1300 | mV | |

***Table 13. LVDS Output DC Characteristics***

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | 1.16 | | 1.60 | V | 100 Ω line to line |
| $V_{OL}$ | Output Low Voltage | 0.81 | | 1.20 | V | 100 Ω line to line |
| $\Delta V_{OUTSINGLE}$ | Single Ended Output Voltage Swing | 250 | | 520 | mV | 100 Ω line to line |
| $V_{OS}$ | Output Offset Voltage | 1.00 | | 1.37 | V | 100 Ω line to line |

***Table 14. Differential CML Output DC Characteristics***

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ (CLOCK) | CML Output High Voltage. | VDD_ TSCLK -0.45 | | VDD_ TSCLK -0.25 | V | |
| $V_{OL}$ (CLOCK) | CML Output Low Voltage. | VDD_ TSCLK -1.15 | | VDD_ TSCLK -0.73 | V | |
| $\Delta V_{OUTDIFF}$ (CLOCK) | CML Serial Output Differential Voltage Swing | 800 | | 1400 | mV | 100 Ω line-to-line. See Figure 12. |
| $\Delta V_{OUTSINGLE}$ (CLOCK) | CML Serial Output Single-Ended Voltage Swing | 400 | | 700 | mV | 100 Ω line-to-line. See Figure 12. |
| $V_{OH}$ (DATA) | CML Output High Voltage. | VDD_ TSD -0.45 | | VDD_ TSD -0.25 | V | |
| $V_{OL}$ (DATA) | CML Output Low Voltage. | VDD_ TSD -1.15 | | VDD_ TSD -0.73 | V | |
| $\Delta V_{OUTDIFF}$ (DATA) | CML Serial Output Differential Voltage Swing | 800 | | 1400 | mV | 100 Ω line-to-line. See Figure 12. |
| $\Delta V_{OUTSINGLE}$ (DATA) | CML Serial Output Single-Ended Voltage Swing | 400 | | 700 | mV | 100 Ω line-to-line. See Figure 12. |

***Table 15. CML Input DC Characteristics***

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $\Delta V_{INDIFF}$ | Differential Input Voltage Swing | 300 | | 1600 | mV | See Figure 12. |
| $\Delta V_{INSINGLE}$ | Single-Ended Input Voltage Swing | 150 | | 800 | mV | See Figure 12. |
| $R_{DIFF}$ | Differential Input Resistance | 80 | 100 | 120 | Ω | |

***Table 16. Transmitter AC Timing Characteristics***

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| | TSCLK Frequency | 2.488 | 2.67 | GHz |
| | TSCLK Duty Cycle | 45 | 55 | % |
| | TSCLK Duty Cycle Distortion w.r.t. RSCLK or BYPASSCLK (In SLPTIME, LLEB or BYPASS modes) | | 5.0 | % |
| | PICLK Duty Cycle | 35 | 65 | % |
| $tS_{PIN}$ | PINP/N[3:0] Setup Time w.r.t. PICLK | 200 | | ps |
| $tH_{PIN}$ | PINP/N[3:0] Hold Time w.r.t. PICLK | 200 | | ps |
| $tS_{TSD}$ | TSD Setup Time w.r.t. TSCLK Rising | 120 | | ps |
| $tH_{TSD}$ | TSD Hold Time w.r.t. TSCLK Rising | 120 | | ps |
| | PCLK to PICLK drift after FIFO is centered | | 2 | ns |
| | PCLK Duty Cycle | 45 | 55 | % |
| | TSD/TSCLK Rise and Fall Time | | 120 | ps |

***Figure 8. Transmitter Input Timing[1]***

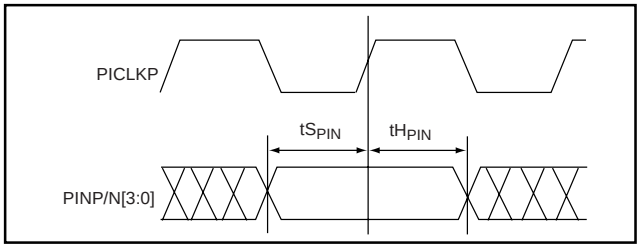
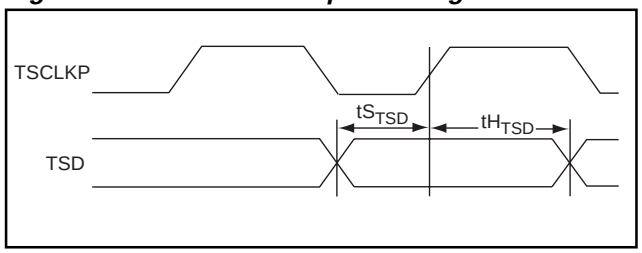



***Figure 9. Transmitter Output Timing[1]***



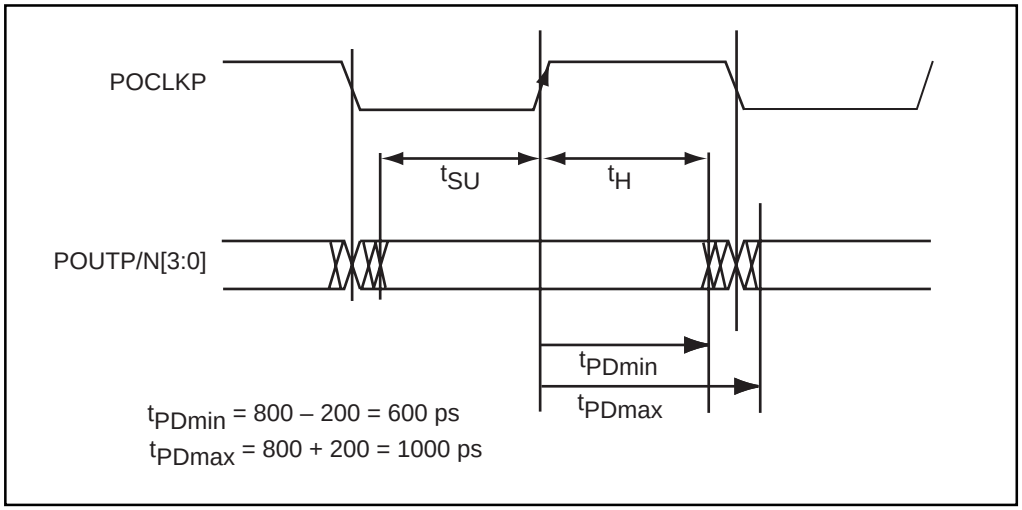

Notes on Timing:

1. Timing is measured from the crossover point of the clock to the crossover point of the data.

***Table 17. AC Receiver Timing Characteristics***

| Parameter | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| | POCLKP/N | 45 | | 55 | % | 100 Ω line-to-line. |
| | POCLKP/N Rise Time | 100 | | 300 | ps | 20%-80%, 100 Ω line-to-line. |
| | POUTP/N Rise Time | 100 | | 300 | | |
| | POCLKP/N Fall Time | 100 | | 300 | ps | 20%-80%, 100 Ω line-to-line. |
| | POUTP/N Fall Time | 100 | | 300 | | |
| $t_{PD}$ | POUTP/N Delay from POCLKP/N | 600 | | 1000 | ps | See Figure 10. |
| $t_{SU}$ | POUTP/N[3:0] Set-Up Time w.r.t. POCLK | 600 | | | ps | See Figure 10. |
| $t_H$ | POUTP/N[3:0] Hold Time w.r.t. POCLK | 600 | | | ps | See Figure 10. |

***Figure 10. Parallel Data Output Delay from POCLK[1]***




Notes on Timing:

1. Timing is measured from the crossover point of the clock to the crossover point of the data.

***Table 18. Reference Clock Select Modes***

| REFSEL1 | REFSEL0 | CSU-REFCLK Frequency | CDR-REFCLK Frequency | Mode |
|---|---|---|---|---|
| 0 | 0 | CSU_REFCLK = REFCLKP/N1 = 155.52 MHz | CDR_REFCLK = REFCLKP/N1 = 155.52 MHz | Non-FEC In<br>Non-FEC Out<br>REFCLKP/N2 not used |
| 0 | 1 | CSU_REFCLK = REFCLKP/N1 = 155.52 MHz | CDR_REFCLK = REFCLKP/N2 = 166.62 MHz | FEC In<br>Non-FEC Out |
| 1 | 0 | CSU_REFCLKP/N = REFCLKP/N2 = 166.62 MHz | CDR_REFCLK = REFCLKP/N1 = 155.52 MHz | Non-FEC In<br>FEC Out |
| 1 | 1 | CSU_REFCLKP/N = REFCLKP/N2 = 166.62 MHz | CDR_REFCLK = REFCLKP/N2 = 166.62 MHz | FEC In<br>FEC Out<br>REFCLKP/N1 not used |

***Figure 11. S3455 155.52 MHz REFCLK Phase Noise Limit***

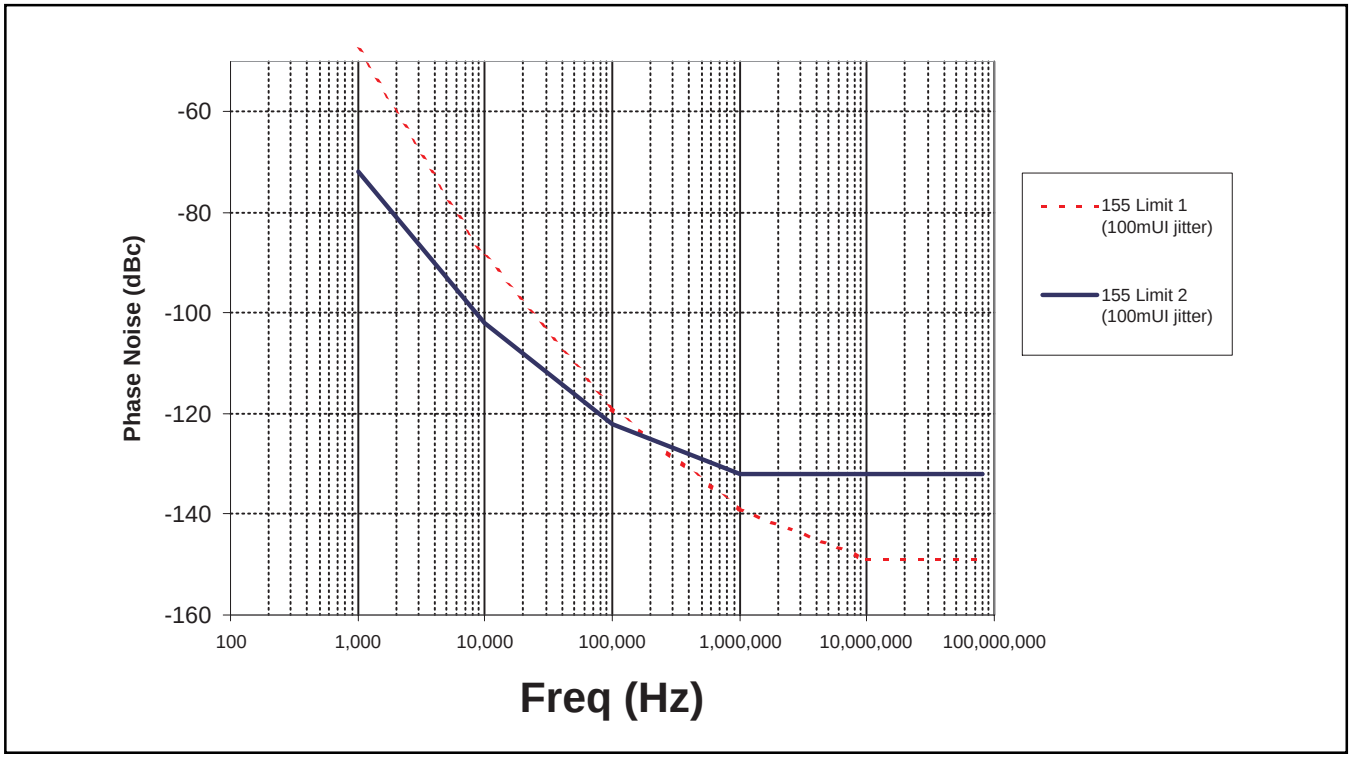
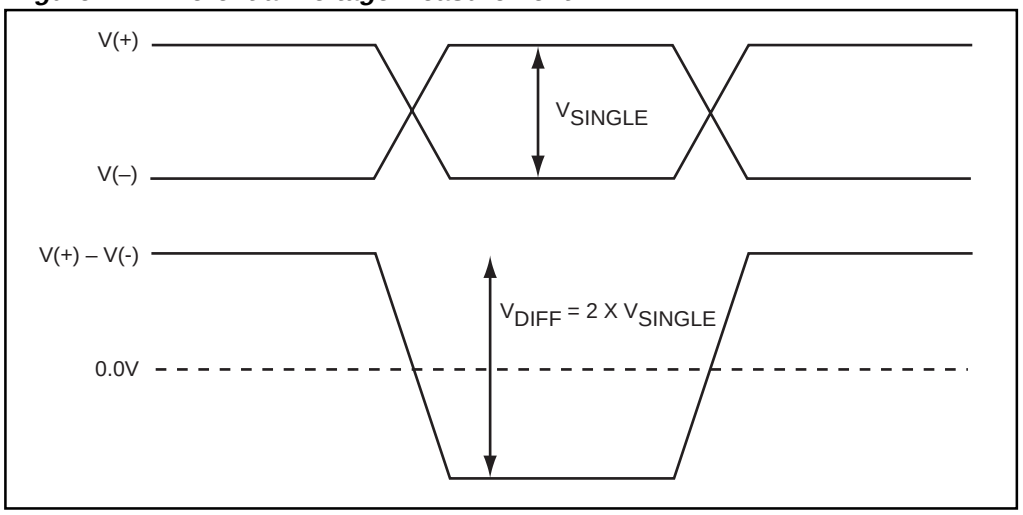
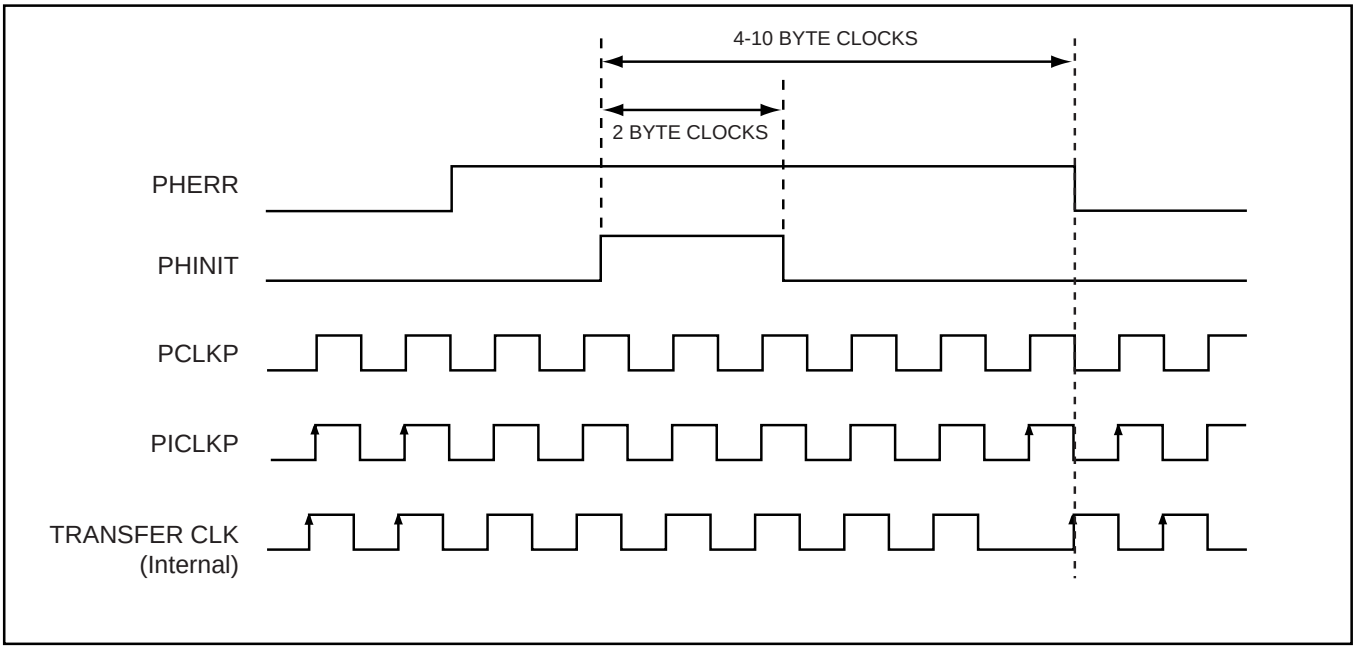


***Figure 12. Differential Voltage Measurement***




Note: V(+) – V(-) is the algebraic difference of the input signals.

***Figure 13. Phase Adjust Timing[1]***




1. 1 byte clock = 622.08 MHz

***Figure 14. Differential CML Output to +5 V/+3.3 V PECL Input AC Coupled Termination***

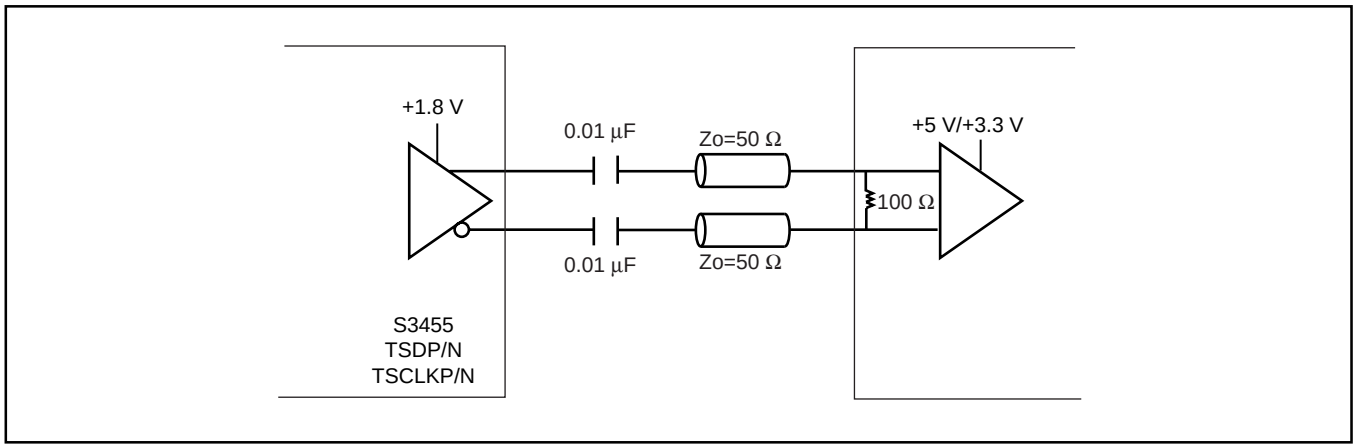



***Figure 15. LVDS Driver to LVDS Input Termination***

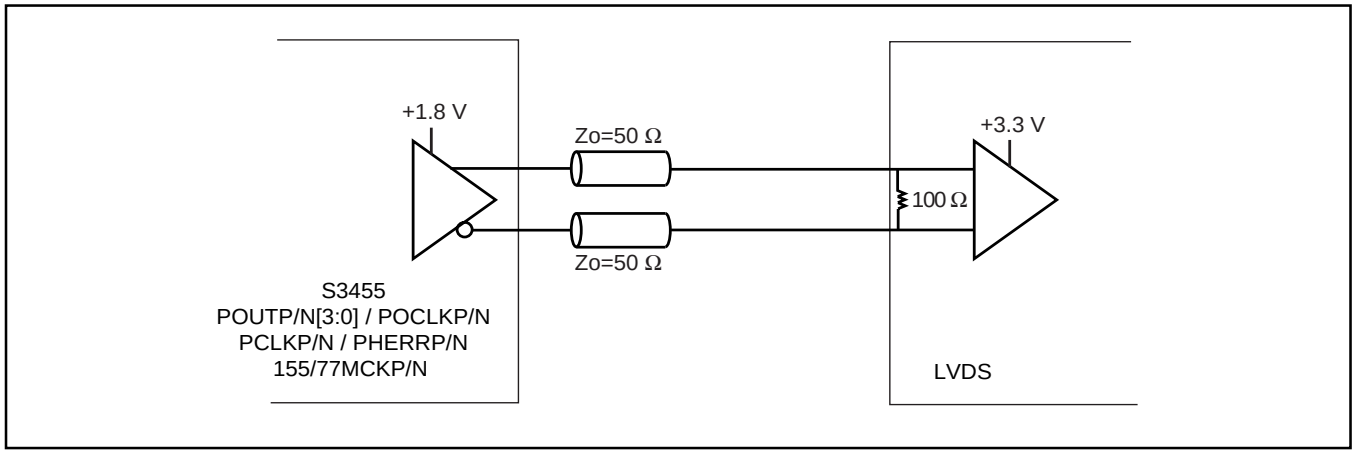



***Figure 16. +5 V Differential PECL Driver to S3455 Differential CML Input AC Coupled Termination***

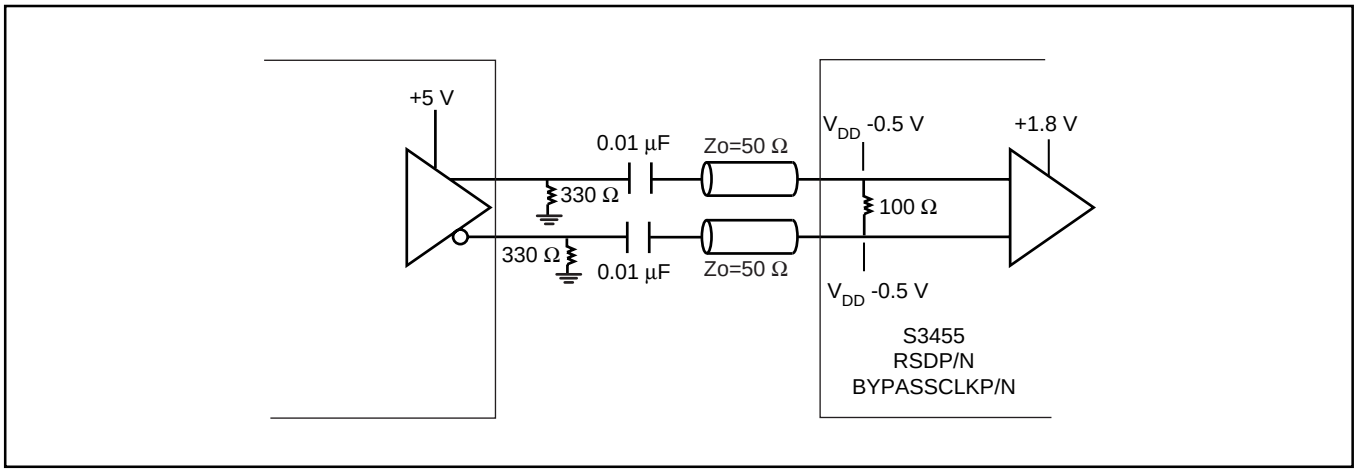


***Figure 17. +5 V/+3.3 V Differential PECL Driver to S3455 LVDS Reference Clock Input AC Coupled Termination***

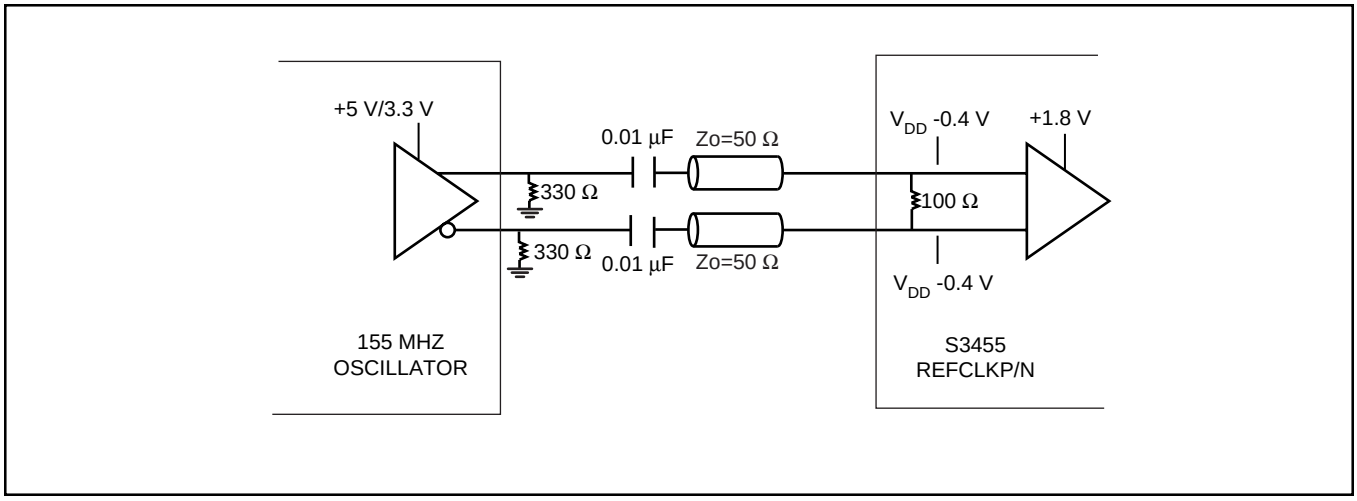



***Figure 18. LVDS Driver to S3455 LVDS Inputs***

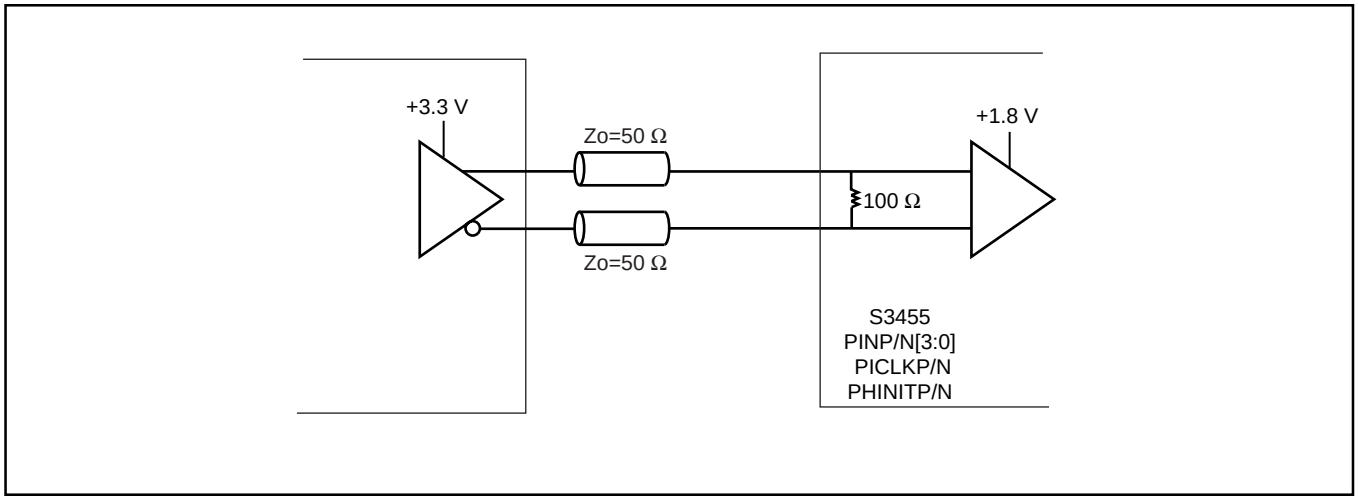
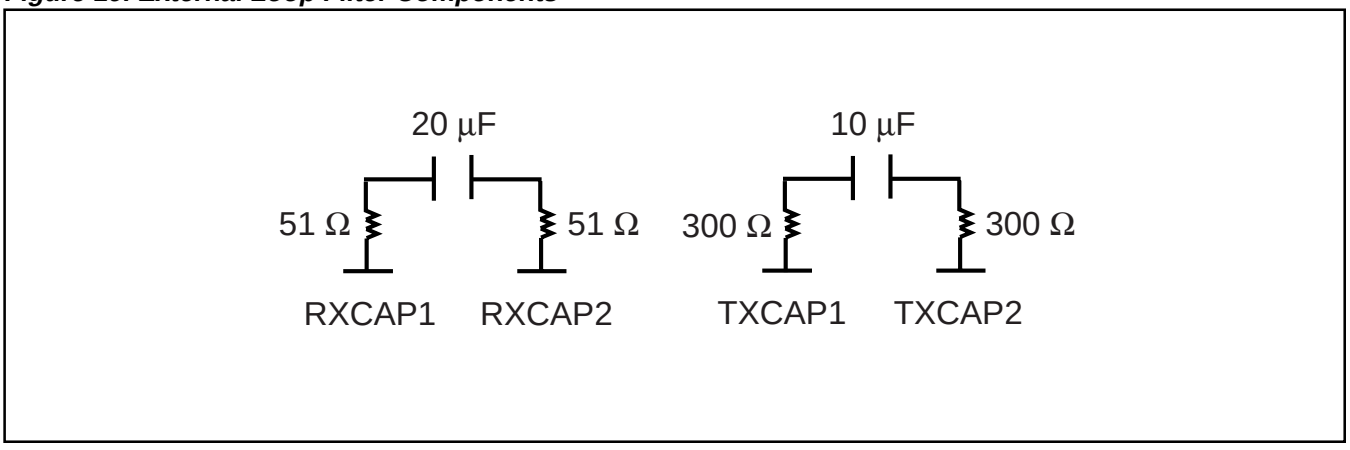
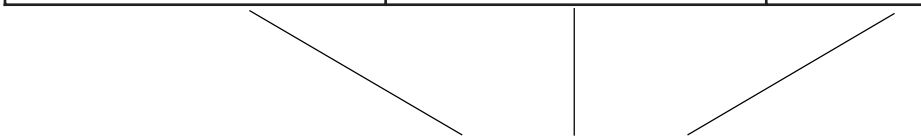



***Figure 19. External Loop Filter Components***



***Ordering Information***

| PREFIX | DEVICE | PACKAGE |
|---|---|---|
| S – Integrated Circuit | 3455 | PB - 196PBGA |



X Prefix

XXXX Part No.

XX Package (S3455 PB)

**Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121**
**Phone: (858) 450-9333 • (800) 755-2622 • Fax: (858) 450-9885**
**http://www.amcc.com**



D145/R1084