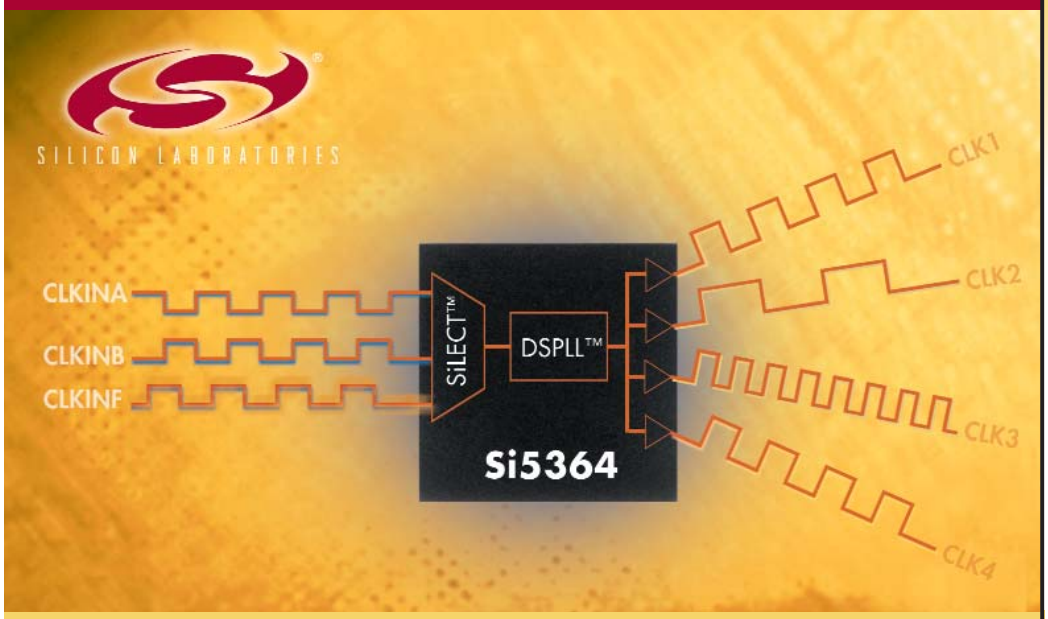
# Si5364

## PRECISION SONET/SDH PORT CARD CLOCK IC

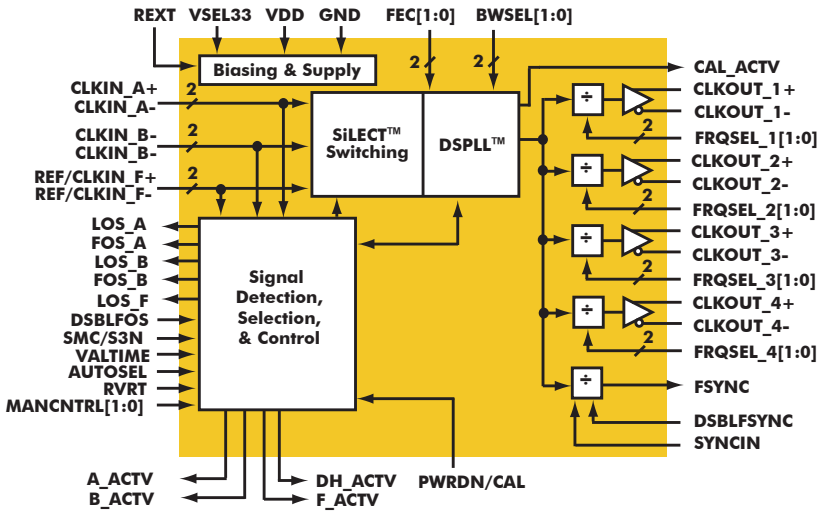



## PRODUCT DESCRIPTION

The Si5364 is a complete solution for ultra-low jitter high-speed clock generation and distribution in precision clocking applications such as OC-192/OC-48 SONET/SDH line/port cards. This device phase locks to one of three reference inputs in the range of 19.44 MHz and generates four synchronous clock outputs that can be independently configured for operation in the 19, 155, or 622 MHz range (1x, 8x and 32x input clock). Silicon Laboratories' DSPLL™ technology provides all phase-locked loop (PLL) functionality with unparalleled performance while eliminating external loop filter components, providing programmable loop parameters, and simplifying design. The on-chip reference monitoring and SiLECT™ clock switching functions support Stratum 2/3/3E and SMC compatible clock switching with excellent output phase transient characteristics. FEC rates are supported with selectable 15/14 or 14/15 scaling of the clock multiplication ratios.

The Si5364 establishes a new standard in performance and integration for ultra-low jitter clock generation. It operates from a single 3.3 V or 2.5 V supply over the industrial temperature range (–40 °C to 85 °C).

## Si5364 BLOCK DIAGRAM




## FEATURES

- Ultra-low jitter clock outputs with jitter generation as low as 0.25 ps (RMS)
- Jitter attenuation with programmable PLL bandwidth (100 Hz, 800 Hz and 6.4 kHz)
- Four programmable clock outputs at 19, 155 or 622 MHz
- Up to three switchable clock inputs
- Automatically or manually controlled hitless switching between clock inputs
- Revertive/non-revertive switching
- Stratum 2, 3, 3E and SMC compatible input clock switching
- No external components (other than a resistor and standard bypassing)
- Digital hold for loss-of-input clock
- Loss-of-signal and frequency offset alarms for each clock input
- Support for 15/14 and 14/15 FEC clock scaling
- 8 kHz frame sync output
- 3.3 V or 2.5 V operation

## APPLICATIONS

- SONET/SDH line/port cards
- Core switches
- Digital cross connects
- Terabit routers

## PRODUCT BRIEF

**THE NEW STANDARD IN ULTRA LOW JITTER CLOCK GENERATION DEVICES**

SILICON LABORATORIES

# Si5364 PRECISION SONET/SDH PORT CARD CLOCK IC

## INNOVATIVE PLL DESIGN, HITLESS SWITCHING SUPPORT, SMALL SIZE

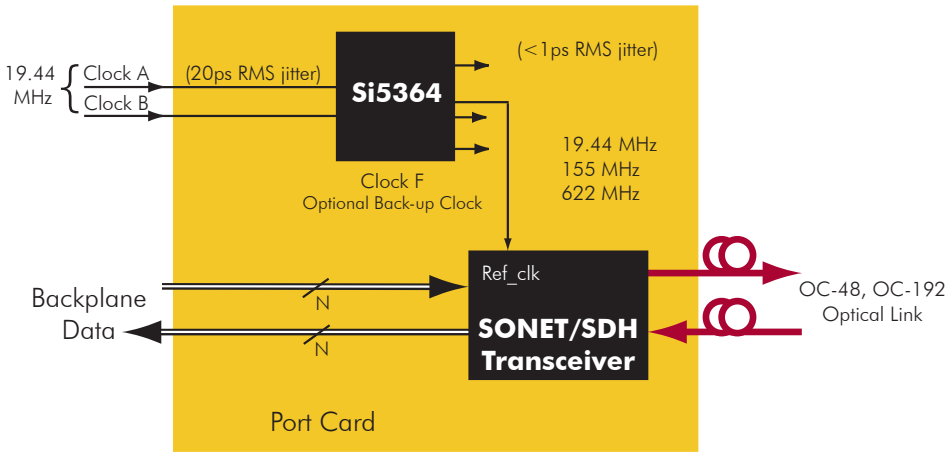
**Ultra Low Jitter:**
The Si5364 produces four ultra-low jitter clocks with typical jitter generation that is better than 0.70 ps (RMS) for OC-48 applications and 0.25 ps (RMS) for OC-192.

**Jitter Attenuation:**
The Si5364 provides selectable PLL bandwidths so that high input clock jitter can be attenuated without degrading output performance. Available loop bandwidth settings are 100 Hz, 800 Hz and 6.4 kHz.

**SiLECT™ Hitless Switching:**
The Si5364 provides reference monitoring and clock switching that significantly exceed Stratum 2/3/3E and SMC requirements. The SiLECT switching technology absorbs the phase offset between the clock inputs to prevent any phase transients on the output clock when switching occurs.

**Small Size:**
The Si5364 provides a 20x space savings compared to the high performance discrete or module based solutions it competes against. These implementations require at least 4 square inches of board space compared with the Si5364's 0.2 square inch footprint.

**Patented DSPLL™ Technology:**
The PLL within the Si5364 utilizes digital signal processing to provide superior jitter performance while keeping all PLL circuitry, including loop filter components, internal to the device. This makes the PLL less susceptible to board level noise sources improving overall jitter performance.




## SIMPLIFIES CLOCK GENERATION AND DISTRIBUTION

The Si5364 is single chip solution for hitless switching and clock generation that is capable of producing the ultra-low jitter reference clocks required by OC-48 and OC-192 physical layer devices.

The Si5364 uses Silicon Laboratories' second generation DSPLL technology to produce low jitter clocks that meet or exceed the performance of the best discrete analog PLL implementations based on expensive crystal or SAW based VCOs. The performance gains provided by this approach are achieved by using digital signal processing techniques to move portions of the analog PLL into the digital domain. This results in a single chip solution that is one twentieth the size of today's existing discrete or module based implementations. This dramatically simplifies board layout while eliminating the sensitive noise entry points present in discrete solutions.

The Si5364 also uses Silicon Laboratories' proprietary SiLECT technology to provide the Stratum 2/3/3E and SMC compliant "hitless" clock switching function required on optical port cards. This technology eliminates output clock phase transients introduced when switching between primary and secondary input timing references. Continuous monitoring of the input timing references is provided with support for both revertive, non-revertive, or manual switching.

## ORDERING INFORMATION

| Product | Description |
|---|---|
| Si5364-BM | SONET/SDH Precision Port Card Clock IC |
| **Data Sheets** | |
| Si5364-DS | Si5364 Data Sheet |
| Si5364-EVB-DS | Si5364 Evaluation Board Data Sheet |
| **Evaluation Boards** | |
| Si5364-EVB | Si5364 Evaluation Board |

## CONTACT INFORMATION

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