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SDC-960A

Integrated Digital Demodulator/Decoder

General Description

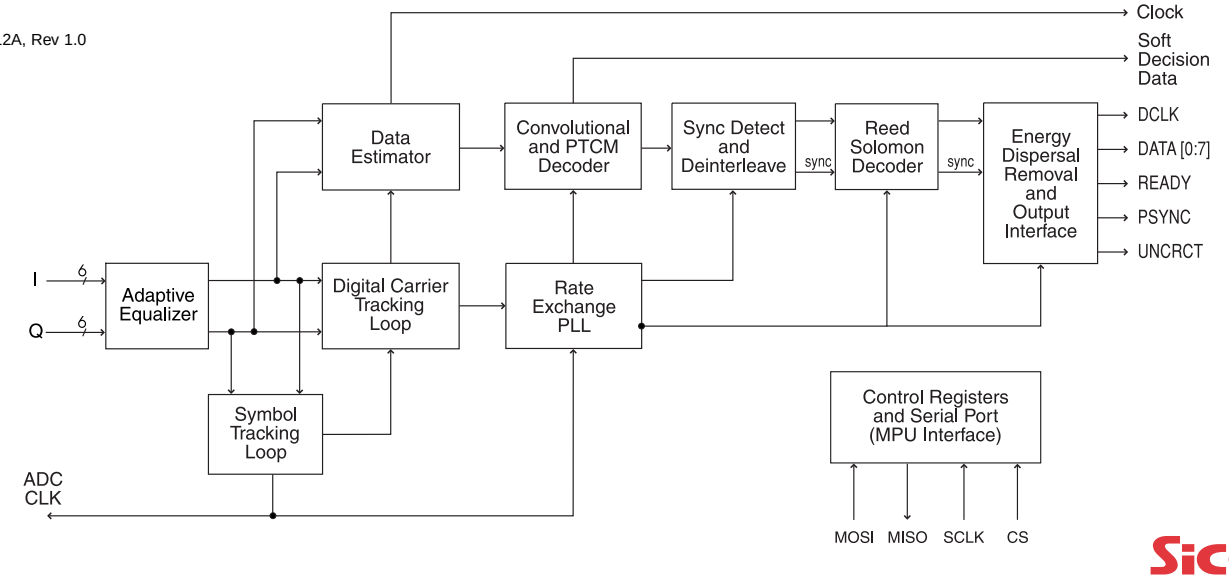
The SDC-960A is an integrated multi-modulation demodulator with forward error correction (FEC) that is fully compliant with the European Digital Video Broadcasting Standard, EN-300-421. It provides complete demodulation and decoding for useful data rates up to 155.52 Mbps (STS-3) using symbol rates up to 68 Mbaud. It is built on an advanced CMOS process, and optimized for high performance and low cost in broadband digital wireless receiver applications, including digital broadcast satellite receivers.

Integrated on the SDC-960A are a digital demodulator, complete with a digital carrier recovery loop and a complete symbol timing synchronization circuit, a convolutional inner decoder, a deinterleaver, and a (204,188) Reed-Solomon outer decoder. The demodulator supports QPSK, 8PSK, and 16QAM. In 8PSK and 16QAM modes, the SDC-960A demodulates pragmatic trellis-coded modulation (PTCM). The SDC-960A includes all necessary synchronization, MPEG2 sync byte recognition, deinterleaving, and energy dispersal removal functions for a complete single-chip demodulation and decoding solution, without any extra decoder logic or external memory.

Features

- 155.52 Mbps (STS-3) maximum useful bit rate
- Multiple modulation formats: QPSK, 8PSK, 16QAM
- QPSK mode is EN-300-421 compliant and meets all DVB satellite receiver requirements
- Convolutional decoder with on-chip puncturing support for all DVB code rates; {1/2, 2/3, 3/4, 5/6, 7/8}
- Rate 5/6 rotationally-invariant PTCM for 8PSK
- Rate 3/4 rotationally-invariant PTCM for 16QAM
- Convolutional deinterleaver with on-chip memory and automatic sync
- Reed-Solomon (204,188) code complies with EN-300-421
- DVB EN 300 421 energy dispersal removal
- Integrated timing and carrier recovery
- Channel error monitoring
- MPEG2 sync byte recognition
- Uncorrectable block output indicator
- 128 pin PQFP package
- 2.0W max power consumption

Block Diagram



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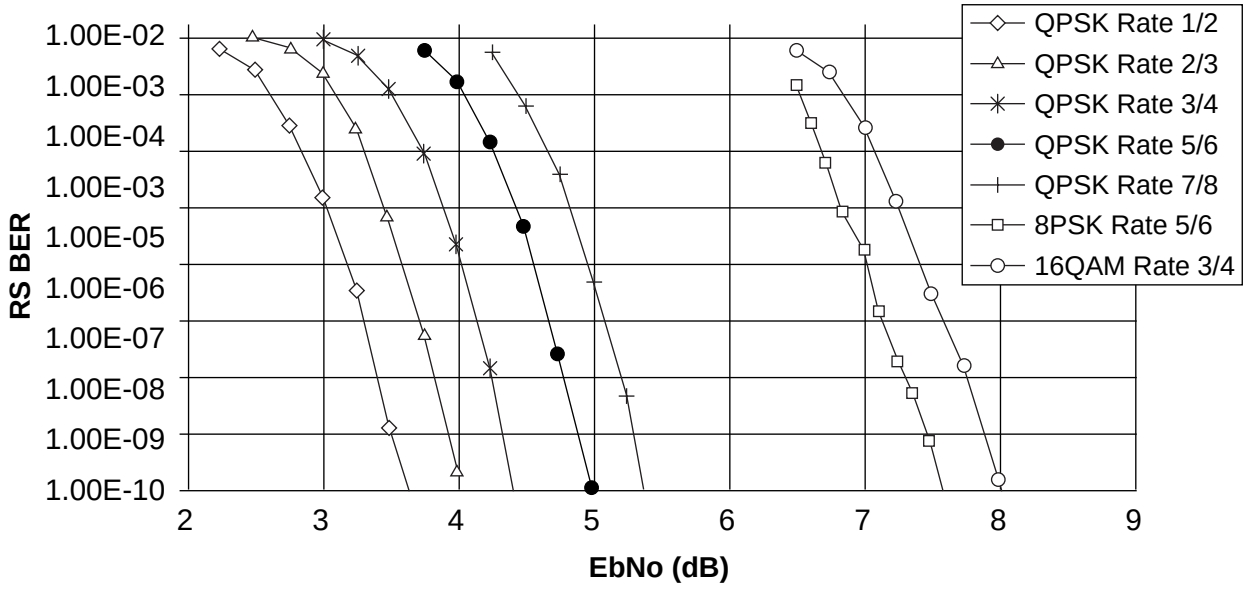
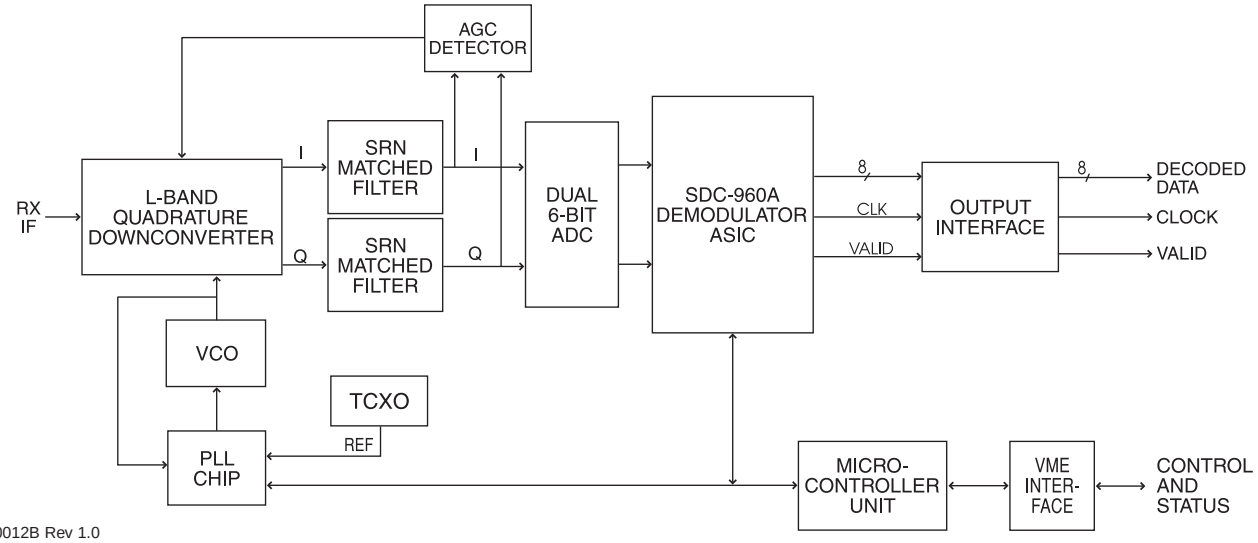
Performance

Performance at the output of the Reed-Solomon decoder. BER performance of $2x10^{-4}$ is required to provide quasi-error free data at the Reed-Solomon decoder output.

Doc 314-A0012C Rev 1.0



Typical Application



Doc 314-A0012B Rev 1.0

Functional Description

The SDC-960A accepts dual 6-bit digitized baseband data from inphase and quadrature channels. The demodulator section of the SDC-960A contains a digital carrier tracking loop, for removal of residual carrier frequency, as well as a complete bit sync loop, including the VCO. Only passive external components are required for the loop filter. The bit sync loop can acquire and track sym/s rates ranging from 5 Mbaud to 68 Mbaud. The SDC-960A contains a high-performance demodulator capable of demodulating QPSK, 8PSK, and 16QAM, as well as a concatenated FEC decoder comprising punctured convolutional (QPSK mode) or PTCM (8PSK and 16QAM modes) decoding, sync decoding and convolutional deinterleaving, Reed-Solomon decoding, energy dispersal removal, and MPEG sync byte decoding. It is designed for full compliance with the ETSI channel coding and modulation standard EN 300 421 on Digital Broadcasting Systems for Television, Sound, and Data Services operating in fixed satellite service (FSS) and broadcast satellite service (BSS) bands.

Demodulator

The demodulator generates symbol timing clock error estimates, performs final carrier recovery, and provides 3-bit soft decision samples to the convolutional decoder. The demodulator integrates both symbol timing and carrier recovery functions on SDC-960A, using a completely integrated digital phase-locked loop for final carrier removal and data extraction. A patented tracking loop pre-processor architecture enables the demodulator to provide fully demodulated soft-decision data using only one sample per symbol from the inphase and quadrature A/D converters, greatly reducing the cost and complexity of providing sampled-data inputs from A/D converters. The SDC-960A symbol timing clock error estimation circuit controls an internal VCO via an external loop filter capacitor for a completely integrated means of generating all clocks necessary for demodulation and decoding.

Convolutional/PTCM Decoder

The convolutional/PTCM decoder performs the first level of error-protection decoding. It is based on the rate 1/2 constraint-length 7 convolutional decoder engine using the polynomials 171_{OCT} and 133_{OCT}, and includes depuncturing logic for decoding at rates {1/2, 2/3, 3/4, 5/6, and 7/8}. The convolutional decoder generates full synchronization information for initialization to the correct code rate and puncture pattern, as well as internal node synchronization and resolution of the demodulator $\pi/2$ phase ambiguity. The decoder accommodates a rate-5/6 rotationally-invariant PTCM code in 8PSK mode, and a rate-3/4 PTCM code in 16QAM mode.

Sync Decoder and Convolutional Deinterleaver

The sync byte decoder detects a periodic sync byte that occurs at 204-byte intervals in the received RS-encoded data stream, provides this synchronization information to the deinterleaver, and recovers the π phase ambiguity of the QPSK demodulator that is not detectable by the convolutional decoder. The sync byte can be programmed, and uses the MPEG2 sync byte (47_h) as a default. The convolutional deinterleaver randomizes error bursts at the output of the inner (convolutional) decoder in order to improve the burst error correction capability of the outer (Reed-Solomon) decoder. The interleaver is composed of 12 branches of FIFO memory, with depth of M x j, where M is 17 and j is the deinterleaver branch index (j=0,...,11).

Reed-Solomon Decoder

The Reed-Solomon decoder is designed to decode the DVB-specified shortened Reed-Solomon (204,188) code, and corrects up to 8 byte-errors in each block of 204 data bytes, which may consist of an MPEG2 transport packet and sync byte. The decoder produces an uncorrectable block output indicator if there are more than 8 byte errors in a received block of 204 bytes. When running in MPEG2 mode, the SDC-960A will set the MPEG TEI bit on uncorrectable packets.

Along with the data and clock outputs, the SDC-960A provides three status lines – UNCRCT, PSYNC, and READY. When the UNCRCT output is low the chip has not performed Reed-Solomon correction on that block. When the chip starts sending a new packet it asserts PSYNC, indicating that the sync byte is currently on the data bus. READY is high for corrected data, low for Reed-Solomon parity bytes.

The Reed–Solomon Encoder is designed to encode the DVB–specified shortened Reed-Solomon (204,188) code which can correct up to 8 byte–errors per received codeword. The code is defined over the finite field GF(2^8), using the primitive polynomial

$$p(x) = x^8+x^4+x^3+x^2+1$$

and the code generator polynomial

$$g(x) = \prod_{i=0}^{15}(x-\alpha^i)$$

Energy Dispersal Removal and Sync Byte Decoder

This block removes the energy dispersal data randomization applied to the data to comply with ITU Radio Regulations and provide an adequate binary transition density and performs final decoding on the sync byte (removal of sync byte inversion).

Rate-Exchange PLL

This block generates the depuncture clock rates necessary in QPSK mode for inserting erasures into the demodulator I/Q soft-decision output data streams prior to decoding by the convolutional decoder. The circuit automatically generates the required clock rate, based on specification through the processor interface of inner code rate and modulation type.

Digital Carrier Tracking Loop

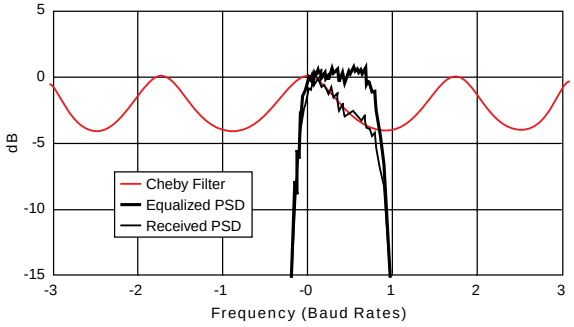
The SDC-960A digital carrier tracking loop has a set of programmable loop bandwidths to support acquisition and tracking across a wide range of symbol rates. It is a completely digital loop, so no external components are required. The loop is a standard second-order type II loop. The loop bandwidth may be changed dynamically, so a wide loop bandwidth may be programmed for acquisition mode, to acquire large frequency offsets or to provide faster acquisition. After initial acquisition, a narrower loop bandwidth may be programmed for tracking mode to provide reduced-jitter performance. In addition, the loop supports a choice of either low-side or high-side down-conversion, as well as a jitter mode, which is used to change the operation of the Carrier Lock Detect circuit to allow measurement of the carrier jitter.

Symbol Tracking Loop

The SDC-960A contains all circuits necessary for a complete symbol-timing synchronization loop, with the exception of the passive loop filter components. The loop is programmed in reference mode to generate a VCO frequency within 0.1% of the expected symbol rate; after this reference frequency is attained, control of the loop is transferred to tracking mode, from which time the loop autonomously acquires and tracks the symbol clock frequency. The loop bandwidth can be changed dynamically to provide separate acquisition and tracking modes. The SDC-960A is configured to support external VCO, charge pump and reference backups.

Equalizer

The SDC-960A contains an adaptive equalizer at its input that removes distortion prior to final carrier removal and symbol synchronization. The equalizer taps may be programmed through the processor interface, or the equalizer may be operated adaptively by programming the adaptation target and an adaptation gain value. The tap coefficients are complex values. Initial values may be programmed through the processor interface prior to enabling the adaptation process.



Doc 314-A0012D Rev 1.0

The SDC-960A adaptive equalizer is particularly useful in removing slope distortion effects due to the input preselector filter. The figure shows the slope-distortion mitigation provided by the equalizer when a 7-pole Chebyshev preselector filter is used; this filter has 4 dB peak-peak ripple. The equalizer output power spectral density is plotted for comparison to the equalizer input power spectral density, and clearly shows that without the equalizer the signal has almost 5 dB of variation across the passband.

Microcontroller Interface

The SDC-960A uses a serial peripheral interface (SPI). This interface allows the device to be programmed from a microcontroller unit equipped with an SPI module. The interface uses 4 pins: 1) the master out, slave in (MOSI) pin for writing data input; 2) the master in, slave out (MISO) pin for reading data output; 3) the serial clock (SCLK) pin; and 4) an active-low chip select (nSEL).