SM7060

Programmable Digital Modulator ASIC

Applications

Satellite Communication Systems

- Broadband VSAT Systems
- Integrated MPEG Encoders/Modulators
- Multimedia Terminals

Terrestrial Wireless Communication Systems

- Point-to-Point FDM Digital Radios
- Point-to-Multipoint Base Station Sectors
- Point-to-Multipoint Customer Premise Equipment (CPE)

Description

SiCOM's SM7060 is a programmable digital modulator ASIC which supports continuous-wave, and burst modes of operation with QPSK, 8PSK, and nQAM (n=16, 32, 64, 128, 256) modulation formats. The SM7060 accepts byte-wide TTL data at clock rates up to 60 MHz, applies Energy Dispersal and Reed-Solomon Error Correction Coding, Convolutional Interleaving, Symbol Generation, Pulse Shaping, Transmitter Linearization, Interpolation, Modulation, Digital Tuning, Inverse Sinc Correction, and produces I/Q baseband outputs or an IF sampled data stream output. The SM7060 uses a 16 bit parallel interface for initial loading of RAMs, register set up, control, and monitoring.

The SM7060 is packaged in a 352 pin ball grid array and includes an IEEE 1149.1 JTAG test interface. SiCOM offers standard and custom application-specific modulator reference designs for the SM7060 modulator ASIC.

SiCOM's SM7060 Programmable Digital Modulator ASIC

- A **universal modulator solution** that supports variable data rates up to 60 Mbaud
- A **flexible solution** which is fully programmable for operation over a wide range of link conditions
- An **integrated solution** with features that reduce system-level wireless link cost

Features	Benefits
Fully Programmable Operation: Selectable Modulation (QPSK, 8PSK, nQAM: n=16, 32, 64, 128, 256) with baud rates up to 60 MBaud	Supports a wide range of DVB, ETSI, and FCC broadband RF link requirements.
Selectable Error Correction Coding (PTCM, Convolutional Interleaving, Reed-Solomon) and Rotational Invariance (FRI, PRI, NRI)	Provides coding flexibility to optimize wireless link capacity and performance.
Pre-Equalization, Pre-Distortion, Constellation Parameters	Compensates for amplitude and group delay characteristics of the RF transmitter.
Pulse Shaping	Roll-off factor can be selected for bit rate and service requirements.
Burst Mode Interface	Interfaces with a variety of media access controllers.
Digital Linearizer	Linearization of non-linear amplifiers to reduce system cost and power consumption.
DVB Compatible	Fully compliant with EN 300 421 and EN 301 210 for ETSI DVB and DSNG applications.
JTAG Test Interface	Integrated testing for volume production
352 Pin Ball Grid Array Package	High level of functionality in a low power dissipation surface mount package

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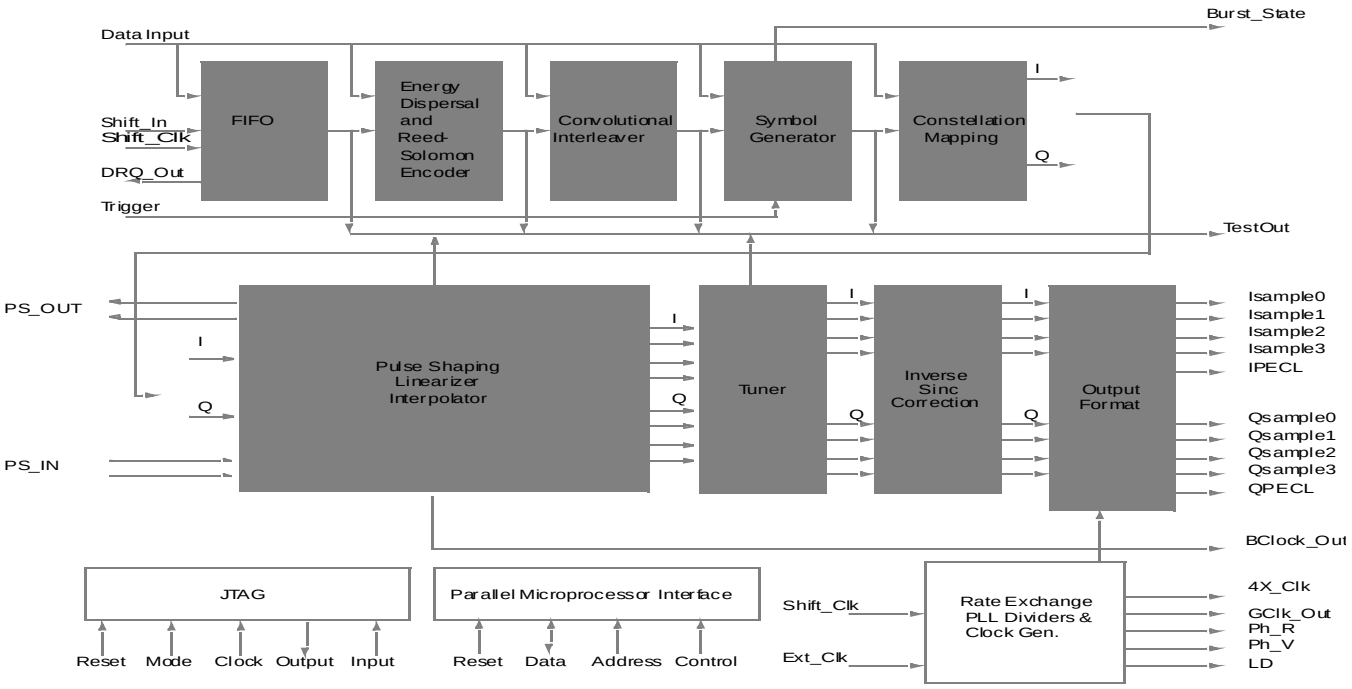

The Block Diagram depicts the SM7060 functional modules. Data input to the SM7060 is first processed by the FIFO which serves as an elastic buffer between the data source and the ASIC. The Energy Dispersal and Reed-Solomon Encoder processes data and sync signals from the FIFO and uses an ETSI specified PRN sequence synchronized to every 8th sync byte to scramble the incoming bytes via an XOR operation. After the scrambler, the data passes through an (N,N-16) R/S Encoder which adds 16 parity bytes to every N-Byte block of message bytes, with N being programmable with a range of 50<N<255. The R/S Encoder supports a variety of operating modes to efficiently process data blocks. The SM7060 supports off-chip burst formatting to interface with a variety of media access controllers.

The Convolutional Interleaver rearranges the time ordering of bytes within and between adjacent blocks. The Interleaver characteristics are programmable with up to I=16 branches of FIFO memory. The Symbol Generator accepts byte wide data, parses it into appropriately sized bit-chunks, and applies differential, convolutional, or pragmatic-trellis coding as programmed. RAM is programmed with a lookup table which translates the output of the Symbol Generator into two 8-bit data streams which drive the I and Q lines of the Pulse Shaping module. The RAM is loaded from the Microprocessor Interface and is dual-port with separate write and read address buses so that writing may be performed at any time.

The Pulse Shaping module is programmable with alpha range 0.10<alpha<0.50 and includes External I/O which allows it to support external pulse shaping or other external modifications to the data stream. The Linearizer performs a nonlinear mapping of complex samples based on an estimate of the complex magnitude of each I/Q pair. The Interpolator converts input data samples at 2X the Baud Rate into output data samples of at least 4X the Baud Rate or greater depending upon the programming of the Interpolation NCO. In order to support Offset QPSK, an OQPSK delay block shifts either the I or Q channels by ½ baud.

The Tuner performs a complex rotation of input data samples at the same output sample rate with a phase angle generated by a NCO. The NCO phase, frequency, and frequency rate are programmable to allow precise control of output signal characteristics. The Output Formatting module formats the 4 I/Q data pairs and includes MUX's and PECL outputs to directly drive high speed, low cost DACs .

The Rate Exchange and Clock Generation module operates in conjunction with external circuits to generate the necessary CLK/SHIFT_IN ratio and also selects the proper clocks for the desired mode of operation. The Microprocessor Interface consists of a 16-bit parallel interface for the internal status/control bus for initial loading of RAMs, initial register setup, ASIC control and monitoring.

Ordering Information

ASIC	Reference Design	Selectable Modulation
SM7060	SM37030	QPSK, 8PSK, 16QAM (all DVB Code Rates)

Consult SiCOM for availability of additional Reference Designs

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