CMOS 2-WIRED SERIAL EEPROM S-24CV64A

The S-24CV64A is a 2-wired, low power and wide range operation 64k-bit EEPROM organized as 8192 words × 8 bits.
Page write and sequential read are available.
Wide package line up makes the S-24CV6A best for any application from consumer electronics to communication devices.

■ Features

- Low power consumption
  - Standby: 5.0 µA Max. (V_{CC}=5.5 V)
  - Read: 0.8 mA Max. (V_{CC}=5.5 V)
- Operating voltage range
  - Read: 1.8 to 5.5 V
  - Write: 2.5 to 5.5 V
- Page write
  - 32 bytes/ page
- Sequential read
- Endurance: 10^5 cycles/word
- Data retention: 10 years
- Write protection area: 100 %

■ Pin Assignment

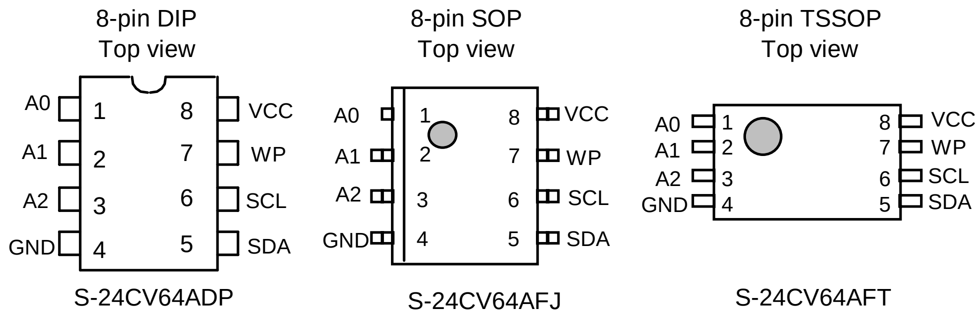

Figure 1

■ Pin Functions

Table 1

Name	Pin Number	Function
A0	1	Slave address input
A1	2	Slave address input
A2	3	Slave address input
GND	4	Ground
SDA	5	Serial data input/output
SCL	6	Serial clock input
WP	7	Write protection input Connected to Vcc: Protection valid Connected to GND: Protection invalid
VCC	8	Power supply

This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to SII is indispensable .

■ Block diagram

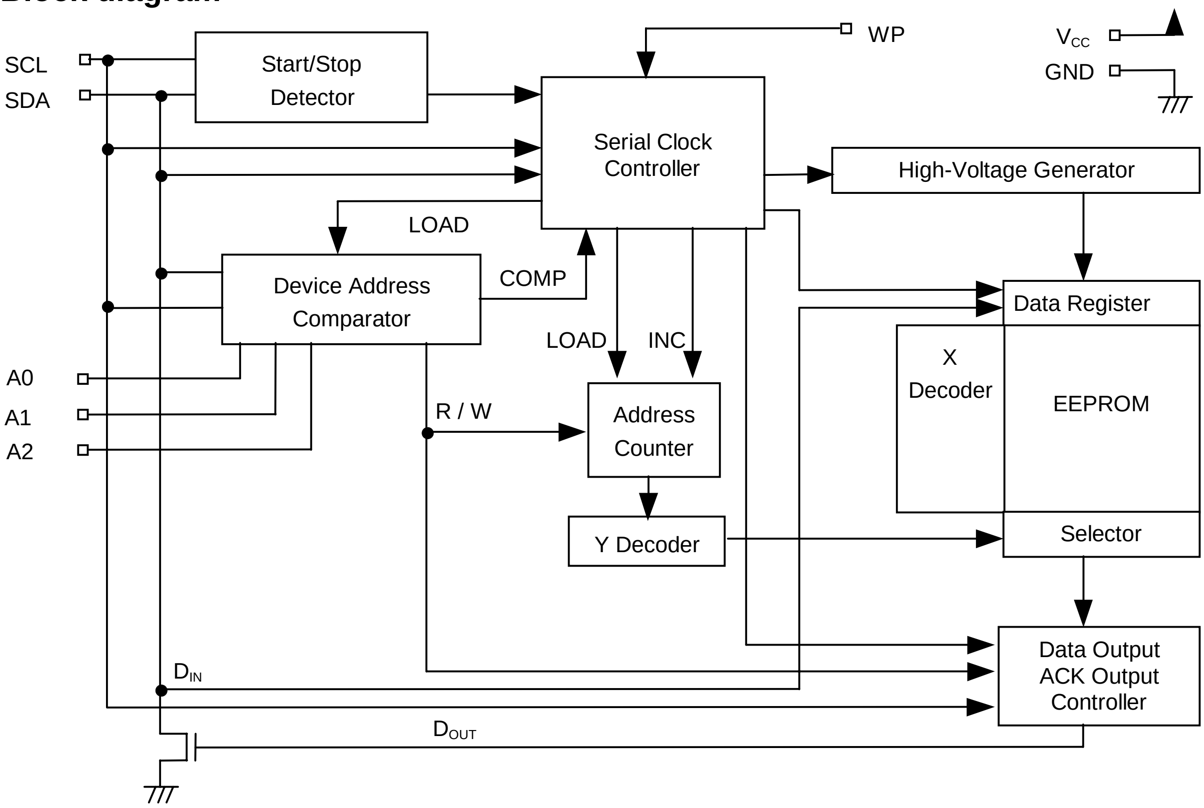

Figure 2

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to +95	°C
Storage temperature	T_{stg}	-65 to +150	°C

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation	1.8	—	5.5	V
		Write Operation	2.5	—	5.5	V
High level input voltage	V_{IH}	V_{CC}=2.5 to 5.5V	0.7×V_{CC}	—	V_{CC}	V
		V_{CC}=1.8 to 2.5V	0.8×V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}	V_{CC}=2.5 to 5.5V	0.0	—	0.3×V_{CC}	V
		V_{CC}=1.8 to 2.5V	0.0	—	0.2×V_{CC}	V
Operating temperature	T_{opr}	—	-40	—	+85	°C

■ Pin Capacitance

Table 4

(Ta=25°C, f=1.0 MHz, V_{CC}=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0 V (SCL, A0, A1, A2, WP)	—	—	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0 V (SDA)	—	—	10	pF

■ Endurance

Table 5

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^5	—	—	cycles/word

■ DC Electrical Characteristics

Table 6

Parameter	Symbol	V_{CC}=4.5 V to 5.5 V f=400 KHz			V_{CC}=2.5 to 4.5 V f=100 KHz			V_{CC}=1.8 to 2.5 V f=100 KHz			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	—	—	0.8	—	—	0.5	—	—	0.3	mA
Current consumption (PROGRAM)	I_{CC2}	—	—	4.0	—	—	3.0	—	—	—	mA

Table 7

Parameter	Symbol	Conditions	V_{CC}=4.5 V to 5.5 V			V_{CC}=1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	V_{IN}=V_{CC} or GND	—	—	5.0	—	—	3.0	µA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	µA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	µA
Low level output voltage	V_{OL}	I_{OL}=3.2 mA	—	—	0.4	—	—	—	V
		I_{OL}=1.5 mA	—	—	0.3	—	—	0.3	V
Current address hold voltage	V_{AH}	I_{OL}=100 µA	1.5	—	5.5	1.5	—	4.5	V

■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	$0.1\times V_{CC}$ to $0.9\times V_{CC}$
Input pulse rising/falling time	20 ns
Output judgment voltage	$0.5\times V_{CC}$
Output load	100 pF+ Pullup resistance 1.0 kΩ

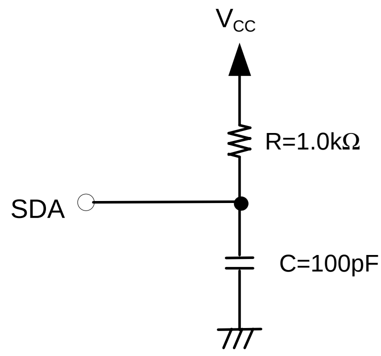

Figure 3 Output Load Circuit

Table 9

Parameter	Symbol	V_{CC}=4.5V to 5.5V			V_{CC}=1.8V to 4.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	—	400	0	—	100	kHz
SCL clock time "L"	t_{LOW}	1.0	—	—	4.7	—	—	µs
SCL clock time"H"	t_{HIGH}	0.9	—	—	4.0	—	—	µs
SDA output delay time	t_{AA}	0.1	—	0.9	0.3	—	3.5	µs
SDA output hold time	t_{DH}	50	—	—	100	—	—	ns
Start condition setup time	$t_{SU.STA}$	0.6	—	—	4.7	—	—	µs
Start condition hold time	$t_{HD.STA}$	0.6	—	—	4.0	—	—	µs
Data input setup time	$t_{SU.DAT}$	100	—	—	200	—	—	µs
Data input hold time	$t_{HD.DAT}$	0	—	—	0	—	—	µs
Stop condition setup time	$t_{SU.STO}$	0.6	—	—	4.7	—	—	µs
SCL · SDA rising time	t_R	—	—	0.3	—	—	1.0	µs
SCL · SDA falling time	t_F	—	—	0.3	—	—	0.3	µs
Bus release time	t_{BUF}	1.3	—	—	4.7	—	—	µs
Noise suppression time	t_I	—	—	50		—	100	µs

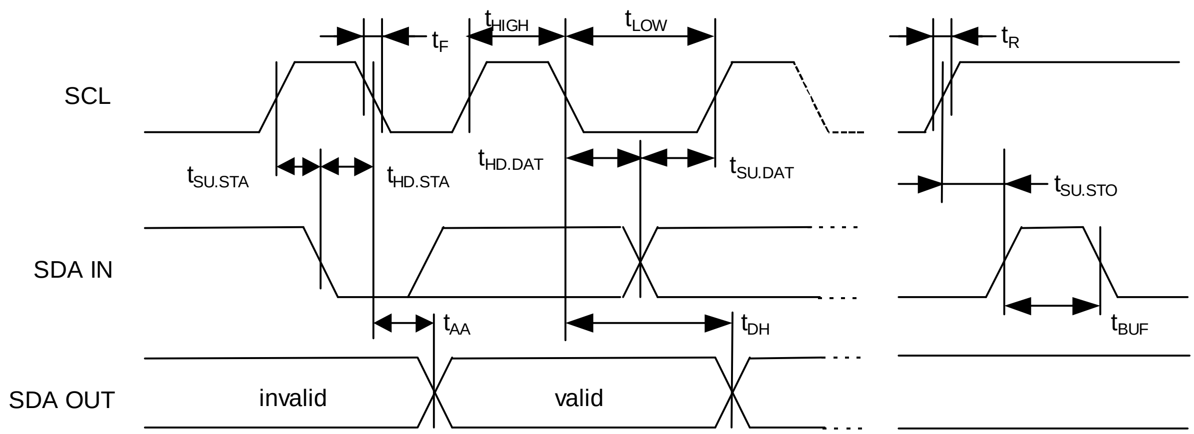

Figure 4 Bus Timing

Table 10

Item	Symbol	Min.	Typ.	Max	Unit
Write time	t_{WR}	-	7.0	10.0	ms

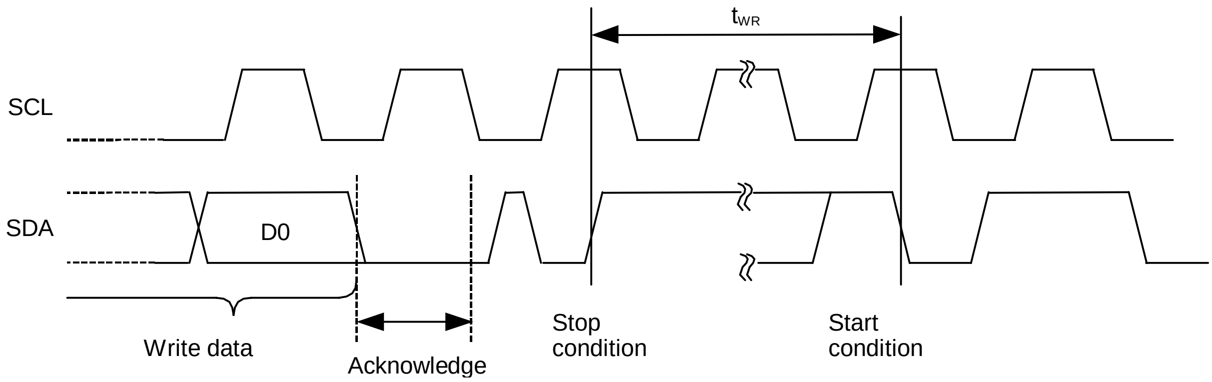

Figure 5 Write Cycle Timing

■ Pin Functions

1. **Address Input Pins (A0, A1, and A2)**
   Slave address is assigned by connecting pins A0, A1, and A2 to the GND or to the V_{CC}, respectively. One of the 8 different slave addresses can be assigned to the S-24CV64A by the combination of pins A0, A1, and A2. The given slave address, which is compared with the slave address transmitted from the master device, is used to select the one among the multiple devices connected to the bus. The address input pins should be connected to the GND or to the V_{CC} .

2. **SDA (Serial Data Input/Output) Pin**
   The SDA pin is used for bi-directional transmission of serial data. It consists of a signal input pin and an Nch open-drain output pin.
   The SDA line is usually pulled up to the V_{CC}, and OR-wired with other open-drain or open-collector output devices.

3. **SCL (Serial Clock Input) Pin**
   The SCL pin is used for serial clock input. Since signals are processed at the rising or falling edge of the SCL clock input signal, attention should be paid to the rising time and falling time to conform to the specifications.

4. **WP Pin**
   Write protection is enabled by connecting the WP pin to the V_{CC}. When there is no need for write protection, connect the pin to the GND.

■ Operation

1. Start Condition

Start is identified by a high to low transition of the SDA line while the SCL line is stable at high.
Every operation begins from a start condition.

2. Stop Condition

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high.
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the EEPROM initiates a write cycle.

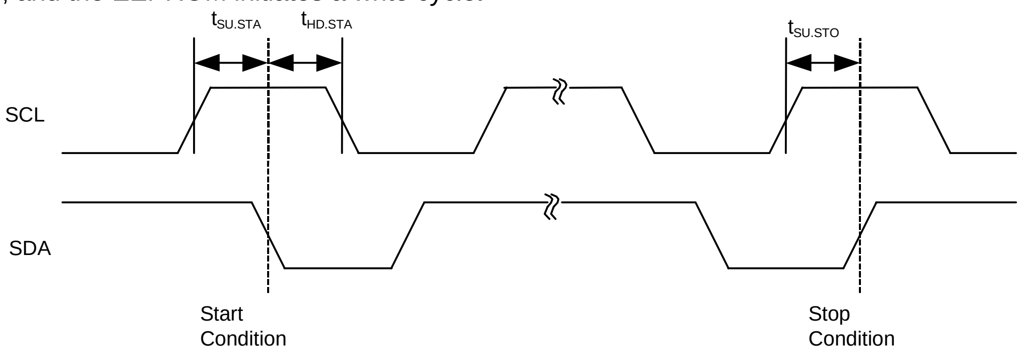

Figure 6 Start/Stop Conditions

3. Data Transmission

Changing the SDA line while the SCL line is low, data is transmitted.
Changing the SDA line while the SCL line is high, a start or stop condition is recognized.

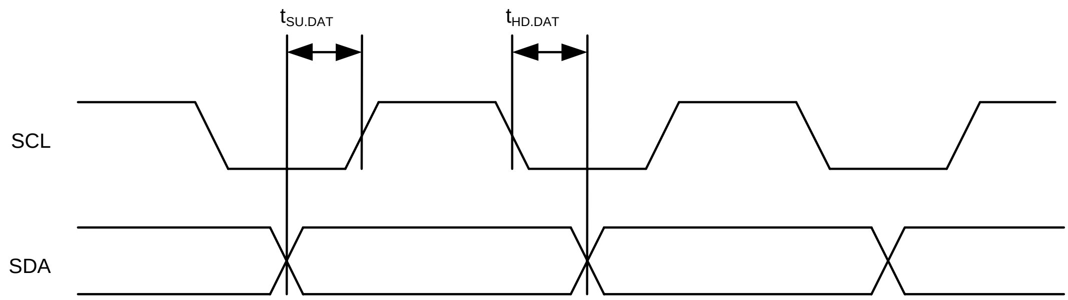

Figure 7 Data Transmission Timing

4. Acknowledge

The unit of data transmission is 8 bits. Uring the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When a internal write cycle is in progress, the device does not generate an acknowledge.

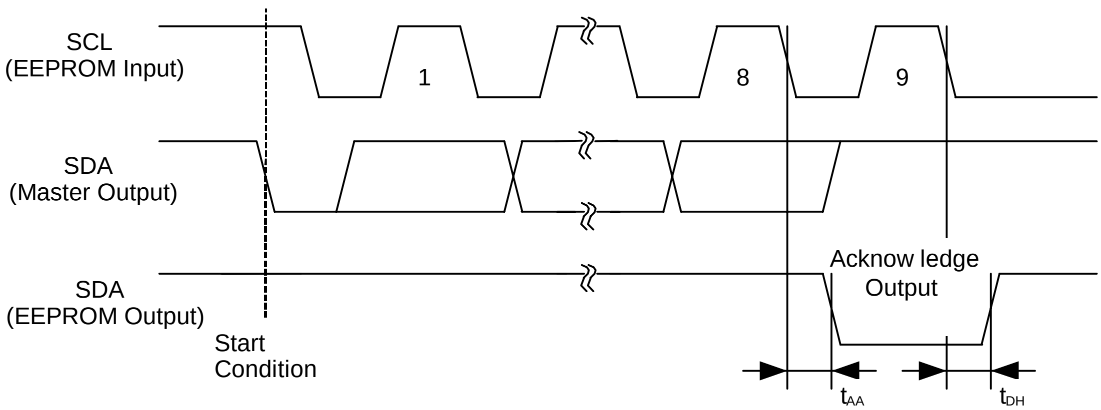

Figure 8 Acknowledge Output Timing

5. Device Addressing

To start communication, the master device on the system generates a start condition to the bus line. Next, the master device sends 7-bit device address and a 1-bit read/write instruction code onto the SDA bus.
The 4 most significant bits of the device address are called the "Device Code," and are fixed to "1010." Successive 3 bits are called the "Slave Address." These 3 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins P0, P1 and P2. When the comparison result matches, the slave device reponds with an acknowledge during the 9th clock cycle.

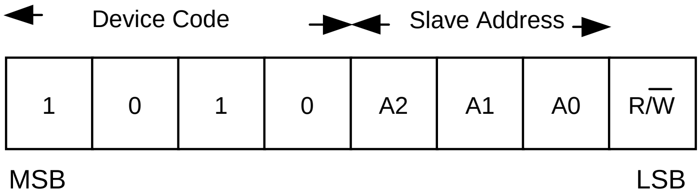

Figure 9 Device Address

6. Write

6.1 Byte Write

When the master sends a 7-bit device address and a 1-bit read/write instruction code set to "0", following a start condition, the EEPROM acknowledges it. The EEPROM then receives an 8-bit upper word address and reponds with an aknowledge. Next the EEPROM receives an 8-bit lower word address and reponds with an aknowledge.
After the EEPROM receives 8-bit write data and reponds with an aknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.
During the write cycle all operations are forbidden and no acknowledge is generated.

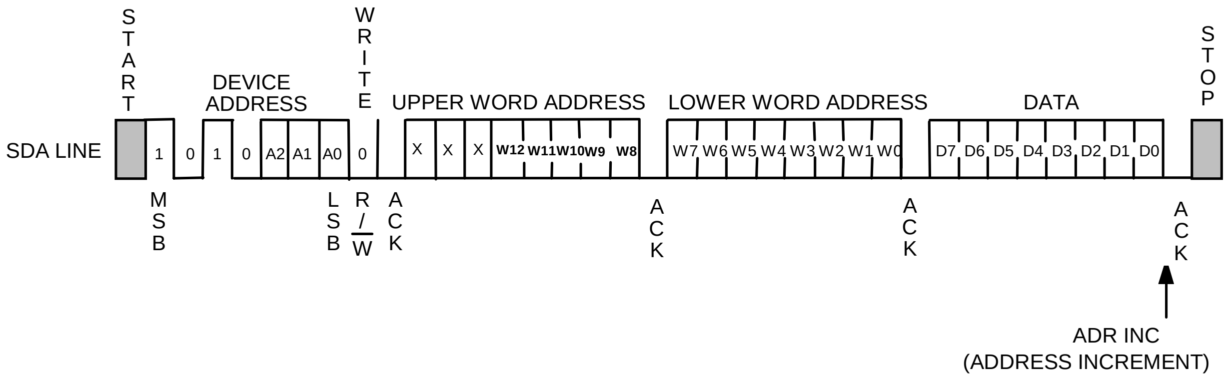

Figure 10 Byte Write

6.2 Page Write

The page write mode allows up to 32 bytes to be written in a single write operation in the S-24CV64A.
Basic data transmission procedure is the same as that in the "Byte Write." But instead of generrating a stop condition, the master transmitts 8-bit write data up to 32 bytes before the page write.

When the EEPROM receives a 7-bit device address and a 1-bit read/write instruction code set to "0", following a start condition, it generates an acknowledge. Then the EEPROM receives an 8-bit upper word address, and reponds with an aknowledge. Next the EEPROM receives an 8-bit lower word address and reponds with an aknowledge. After the EEPROM receives 8-bit write data and reponds with an aknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. The EEPROM repeats reception of 8-bit write data and generation of acknowledge in succession. The EEPROM can receive as many write data as the maximum page size.

Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.

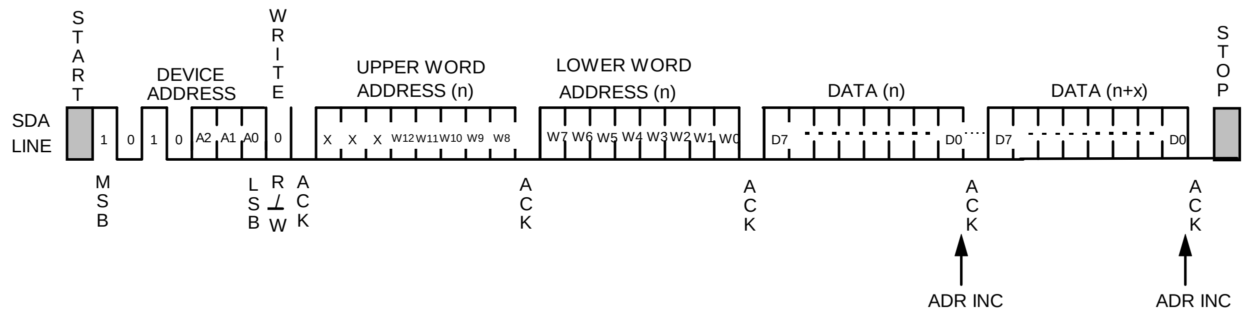

Figure 11 Page Write

The lower 5 bits of the word address are automatically incremented every time when the EEPROM receives 8-bit write data. If the size of the write data exceeds 32 bytes, the upper 8 bits of the word address remain unchanged, and the lower 5 bits are rolled over and previously received data will be overwritten.

6.3 Acknowledge Polling

Acknowledge polling is used to know the completion of the write cycle in the EEPROM.
After the EEPROM receives a stop condition and once starts the write cycle, all operations are forbidden and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in the EEPROM by detecting a response from the slave device after transmitting the start condition, the device address and the read/write instruction code to the EEPROM, namely to the slave devices.
That is, if the EEPROM does not generate an acknowledge, the write cycle is in progress and if the EEPROM generates an acknowledge, the write cycle has been completed.
It is recommended to use the read instruction "1" as the read/write instruction code transmitted by the master device.

6.4 Write Protection

Write protection is available in the S-24CV64A. When the WP pin is connected to V_{CC}, write operation to memory area is forbidden at all. Even the writing is forbidden, the EEPROM does not respond to a signal transmitted by the master device during the time of writing (t_{WR}), since the control circuit inside the IC operates.
When the WP pin is connected to GND, the write protection is invalid, and write operation in all memory area is available. There is no need for using write protection, the WP pin should be connected to GND.
The write protection is valid in the operating voltage range.

7. Read

7.1 Current Address Read

Either in writing or in reading the EEPROM holds the last accessed memory address, internally incremented by one. The memory address is maintained as long as the power voltage is higher than the current address hold voltage V_{AH}.
The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in the EEPROM. This is called "Current Address Read."
In the following the address counter in the EEPROM is assumed to be n.
When the EEPROM receives a 7-bit device address and a 1-bit read/write instruction code set to “1” following a start condition, it responds with an acknowledge.
Next an 8-bit data at the address "n" is sent from the EEPROM synchronous to the SCL clock. The address counter is incremented at the falling edge of the SCL clock for the 8th bit data, and the content of the address counter becomes n+1.
The master device has to not acknowledge the 8-bit data and terminates the reading with a stop condition.

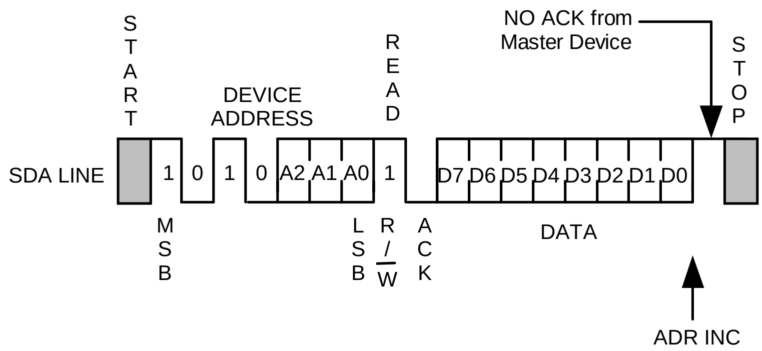

Figure 12 Current Address Read

Attention should be paid to the following point on the recognition of the address pointer in the EEPROM. In the read operation the memory address counter in the EEPROM is automatically incremented at every falling edge of the SCL clock for the 8th bit of the output data. In the write operation, on the other hand, the 8-bit upper address is left unchanged and is not incremented at the falling edge of the SCL clock for the 8th bit of the received data.

7.2 Random Read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the memory address into the address counter.
When the EEPROM receives a 7-bit device address and a 1-bit read/write instruction code set to "0" following a start condition, it reponds with an acknowledge. The EEPROM then receives an 8-bit upper word address and reponds with an acknowledge. Next the EEPROM then receives an 8-bit lower word address and reponds with an acknowledge. The memory address is loaded to the address counter in the EEPROM by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in a byte write and in a page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when the EEPROM receives a 7-bit device address and a 1-bit read/write instruction code set to "1," following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from the EEPROM in synchronous to the SCL clock. The master device has to not acknowledge and terminates the reading with a stop condition.

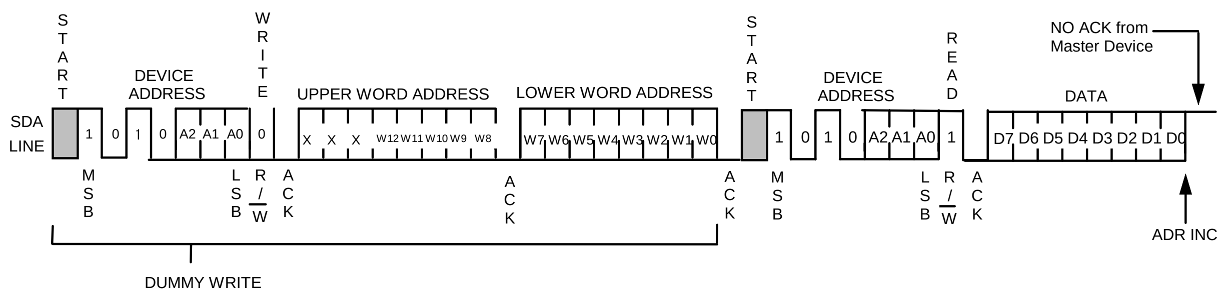

Figure 13 Random Read

7.3 Sequential Read

When the EEPROM receives a 7-bit device address and a 1-bit read/write instruction code set to "1" following a start condition both in current and random read operations, it responds with an acknowledge. An 8-bit data is then sent from the EEPROM synchronous to the SCL clock and the address counter is automatically incremented at the falling edge of the SCL clock for the 8th bit data.
When the master device responds with an acknowlidge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in the EEPROM incremented and makes it possible to read data in succession. This is called "Sequential Read."
The master device has not acknowledge and terminates the reading with a stop condition.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first memory address.

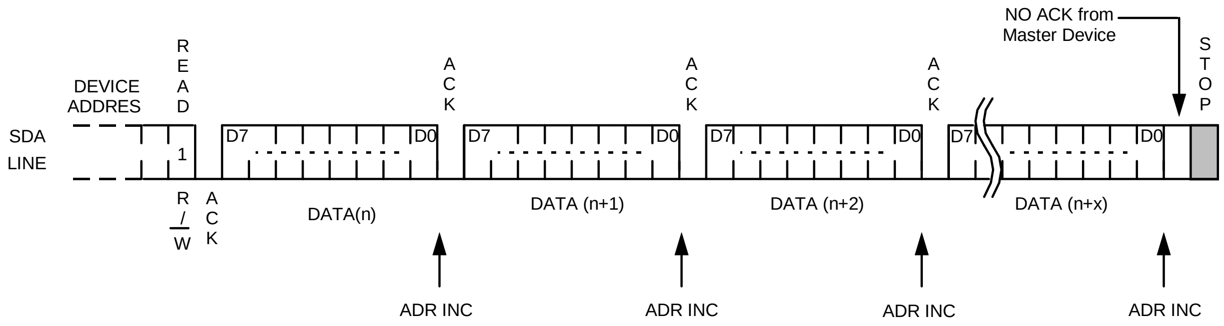

Figure 14 Sequential Read

8. Address Increment Timing

The timing for the automatic address increment is the falling edge of the SCL clock for the 8th bit of the read data in read operation and the the falling edge of the SCL clock for the 8th bit of the received data in write operation. (See figures 15 and 16.)

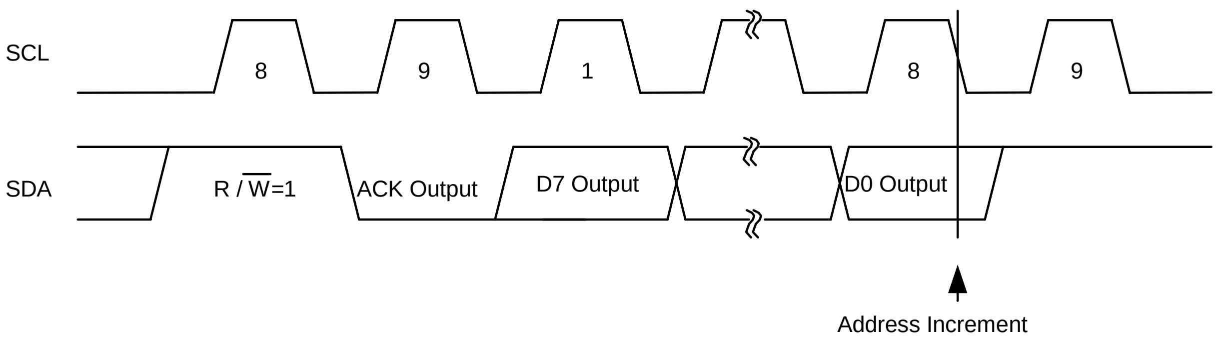

Figure 15 Address Increment Timing in Reading

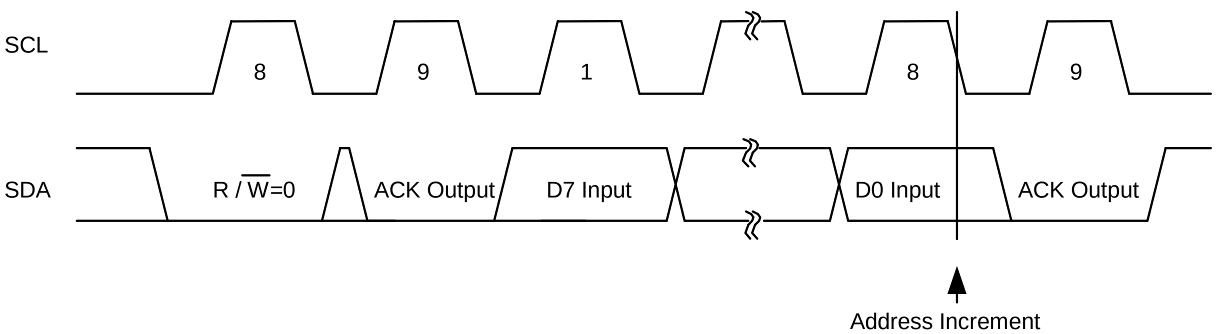

Figure 16 Address Increment Timing in Writing

■ Precautions

Generally, an EEPROM may cause a malfunction by the operation in low voltage range induced by power ON/OFF. The S-24CV16A initializes itself by the power on clear circuit at power on.
Attention should be paid to the followings so as to operate the power on clear circuit correctly, otherwise malfunction may occur.

1. All input and output pins should be connected to V_{CC} or GND level so as not to be floating.
2. Raise the power voltage up to the operation voltage from 0 V without staying at middle range.
3. Raising speed of the power voltage should be faster than 40 ms/V.
4. Power off interval before power on should be longer than 100 ms.

■ I^2C Bus License

Purchase of I^2C components of Seiko Instruments Inc., conveys a license under the Philips I^2C Patent. Rights to use these components in an I^2C system, is granted provided that the system conforms to the I^2C Standard Specification as defined by Philips.
Please note that a product or a system incorporating this IC may infringe upon the Philips I^2C Patent Rights depending upon its configuration. In the event of such infringement Seiko Instruments Inc., shall not bear any responsibility for any matters with regard to and arising from such patent infringement.