

### POWER MANAGEMENT

#### Description

SC2442 is a high performance dual buck converter controller that can be configured for a variety of synchronous buck applications where efficiency is most important. Both converters are synchronized to prevent beat frequencies. The dual buck converters are also operated out of phase reducing input ripple, allowing for fewer input capacitors.

High frequency operation up to 1 MHz reduces the size of output inductors and capacitors. The controller has separate power pins for both VCC and GND to improve noise immunity. The VCC supplies can be regulated to 7V using an external PNP transistor. Other features include: bootstrapping for high side drive supplies, asynchronous mode start up, power up sequencing to prevent latch-ups, individual soft start for each convertor, bootstrapped drivers for high side N-channel MOSFETs, input side current sensing, dual mode current limit with hiccup, enable and external frequency synchronization.

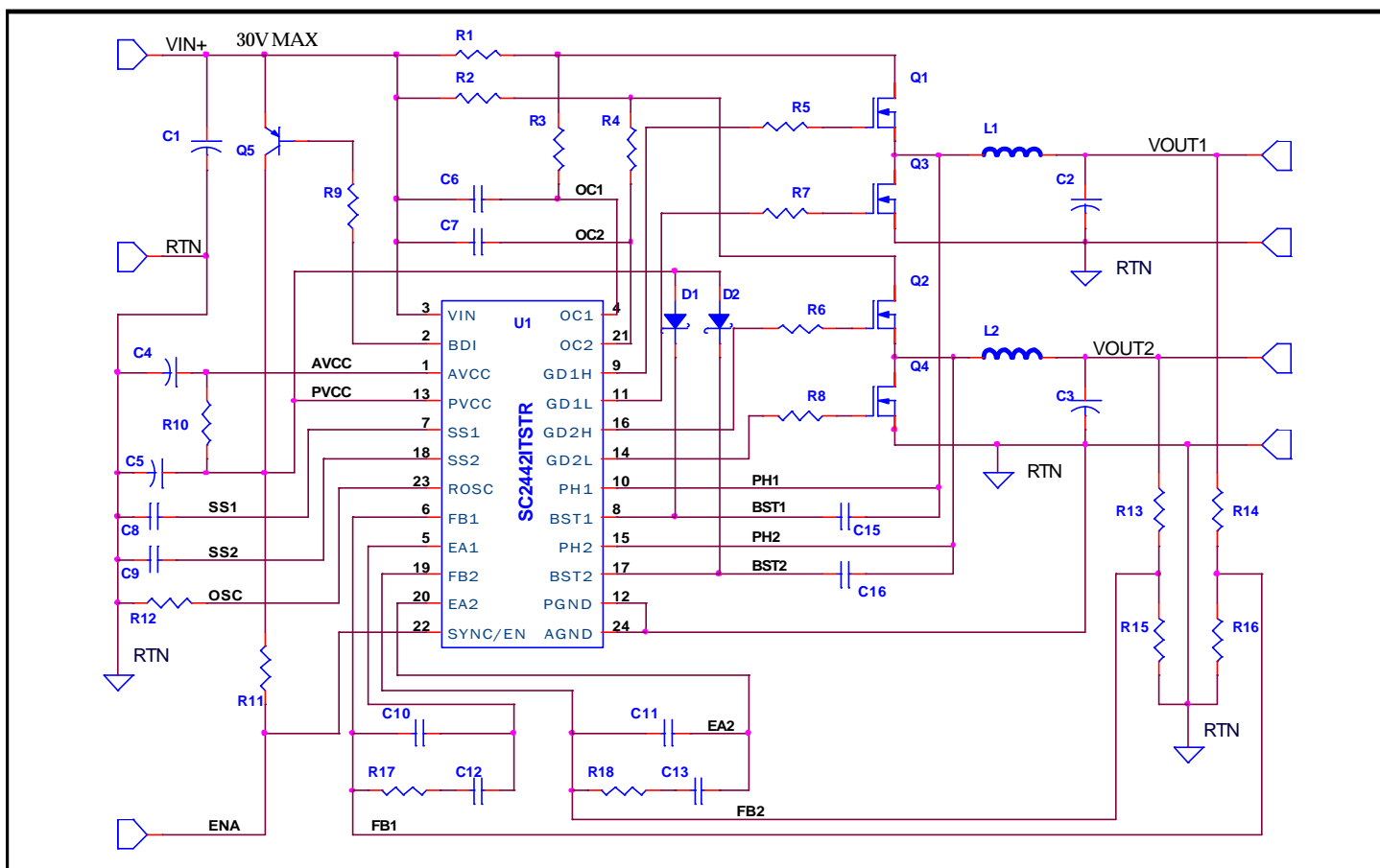
#### Features

- ◆ Dual output controller
- ◆ Asynchronous start up mode
- ◆ Power up sequencing to prevent latch-ups
- ◆ Out of phase operation for low input ripple
- ◆ Over current protection
- ◆ Output down to 0.75V
- ◆ Wide input range, 4.5 to 30V
- ◆ Vcc regulator with external PNP transistor
- ◆ Programmable frequency up to 1MHz
- ◆ Two synchronous bucks for high efficiency at high current
- ◆ -40 to +125 Deg C operating temperature
- ◆ Small package TSSOP-24

#### Applications

- ◆ Point of load converter applications
- ◆ DSL applications with multiple output voltages
- ◆ Power management for mixed signal applications
- ◆ Cable modems and set top boxes.

#### Typical Application Circuit



## POWER MANAGEMENT

### Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction.  
Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
BST1, BST2 to PGND	$V_{BST1}, V_{BST2}$	38	V
VIN to PGND	VIN	30	V
BDI to PGND	$V_{BDI}$	VIN	V
OC1 and OC2 to VIN	$VIN - V_{OC1}, VIN - V_{OC2}$	-0.3 to +0.5	V
PVCC, AVCC to PGND	PVCC, AVCC	8	V
BST1 to PH1, BST2 to PH2 GD1H to PH1, GD2H to PH2		-0.3 to 8	V
GD1L, GD2L to PGND		-0.3 to PVCC	V
PGND to AGND		±0.3	V
PH1, PH2 -ve swing wrt PGND (for 100 nS)	$V_{PH1}, V_{PH2}$	-1	V
All Other Pins to AGND		-0.3 to AVCC	V
Junction Temperature		-40 to +125	°C
Storage Temperature Range		-60 to +150	°C
Lead Temperature (Soldering) 10 Sec.		260	°C

### Electrical Characteristics

Unless specified:  $T_A = T_J = -40$  to  $125^{\circ}\text{C}$ , VIN = 24V,  $V_{CC} = 7\text{V}$ ,  $f_c = 500\text{KHz}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Undervoltage Lockout</b>						
Start Threshold	$V_{UVLO}$	AVCC rising	4.5	4.6	4.75	V
UVLO Hysteresis	$V_{HYST}$	AVCC falling		0.15		V
<b>Power Supply</b>						
Operating Current	$I_{QSC}$	No load, SYNC/EN = Low		8	13	mA
AVCC/PVCC Regulated	AVCC, PVCC	VIN > 8V	6.7	7.0	7.3	V
BDI Drive Current	$I_{BDI}$	VIN > AVCC + 2V	3	5		mA

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### Electrical Characteristics (Cont.)

Unless specified:  $T_A = T_J = -40$  to  $125^\circ\text{C}$ ,  $V_{IN} = 24\text{V}$ ,  $V_{CC} = 7\text{V}$ ,  $f_c = 500\text{KHz}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Soft Start</b>						
Charging Current	$I_{SS1}, I_{SS2}$		7	10	13	$\mu\text{A}$
Discharge Current	$I_{SS1}, I_{SS2}$		-1	-2	-4	$\mu\text{A}$
<b>Error Amplifier</b>						
Voltage Feedback Reference	$V_{FB1}, V_{FB2}$		0.735	0.750	0.765	V
Input Bias Current	$I_{EABIAS}$			500		nA
Open Loop Gain <sup>(1)</sup>	$G_{DC}$			70		dB
Unity Gain Bandwidth <sup>(1)</sup>	GBW			3		MHz
Output Source/Sink Current				2		mA
Output Slew Rate <sup>(1)</sup>				1		V/ $\mu\text{S}$
PWM to Output Delay <sup>(1)</sup>				80		nS
<b>Oscillator</b>						
Frequency Range	Fc		0.1		1	MHz
Clock Frequency	Fc	ROSC = 60K	440	500	560	KHz
Oscillator Peak Voltage <sup>(1)</sup>		Internal		3.0		V
Oscillator Valley Voltage <sup>(1)</sup>		Internal		1.5		V
<b>Sync/Enable Input</b>						
Enable Threshold Voltage	$V_{SYEN}$	SYNC/EN pin Voltage rising	1.8	2.0		V
Disable Threshold Voltage	$V_{SYEN}$	SYNC/EN pin Voltage falling		0.8	1.0	V
Disable Low to Shut Down Delay <sup>(1)</sup>		SYNC/EN pin < 0.8V		50		nS
Sync Input High Level	$V_{SYEN}$			TTL		V
Sync Input Low Level	$V_{SYEN}$			TTL		V
<b>Current Limit</b>						
OC1, OC2 Current Limit Sense	$V_{OC1}, V_{OC2}$		-80	-105	-125	mV
Feedback Threshold for Hiccup	$V_{FB1}, V_{FB2}$		0.450	0.525	0.610	V
OC Sense to Drive Turn Off Delay <sup>(1)</sup>	$T_{OCDLY}$			80		nS

## POWER MANAGEMENT

### Electrical Characteristics (Cont.)

Unless specified:  $T_A = T_J = -40$  to  $125^\circ\text{C}$ ,  $V_{IN} = 24\text{V}$ ,  $V_{CC} = 7\text{V}$ ,  $f_c = 500\text{KHz}$

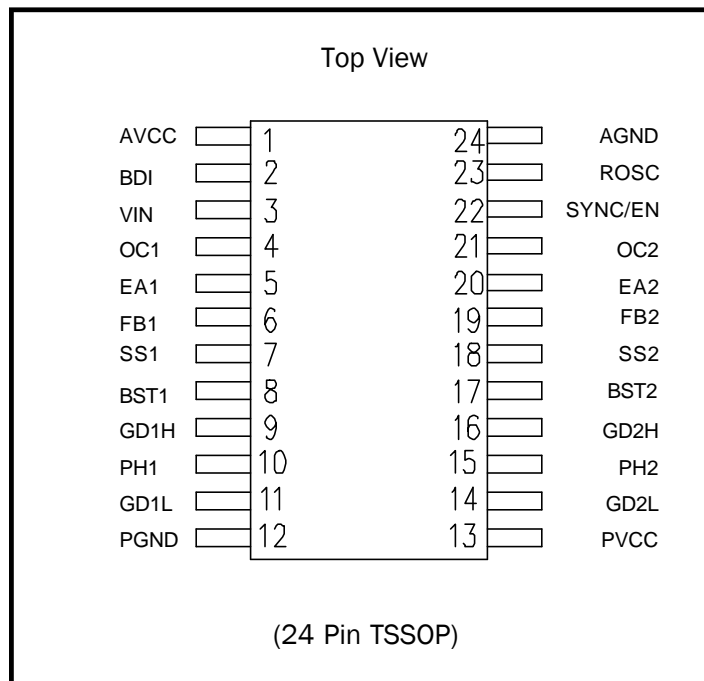
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Gate Drive Outputs</b>						
High Side Gate Drive <sup>(1)</sup>	$I_{GDH+}, I_{GDH-}$	Source/Sink		$\pm 0.5$		A
Low Side Gate Drive <sup>(1)</sup>	$I_{GDL+}, I_{GDL-}$	Source/Sink		$\pm 0.5$		A
Gate Drive Rise Time	$T_{RISE}$	$C_{OUT} = 1000 \text{ pF}$		30		nS
Gate Drive Fall Time	$T_{FALL}$	$C_{OUT} = 1000 \text{ pF}$		30		nS
Maximum Duty Cycle	Dmax	For PWM1 and PWM2	85	94		%
Minimum Duty Cycle	Dmin	For PWM1 and PWM2		0		%
Dead Time Between Gate Drives	$T_{DEAD}$			100		nS

#### NOTES:

(1) Guaranteed by design, not tested in production

(2) This device is sensitive to ESD. Use of standard ESD handling precautions is required.

### Pin Configuration



### Ordering Information

Part Number	Package	Temp. Range ( $T_A$ )
SC2442ITSTR	TSSOP-24	$-40^\circ\text{C}$ to $+125^\circ\text{C}$

#### Note:

Only available in tape and reel packaging. A reel contains 2500 devices.

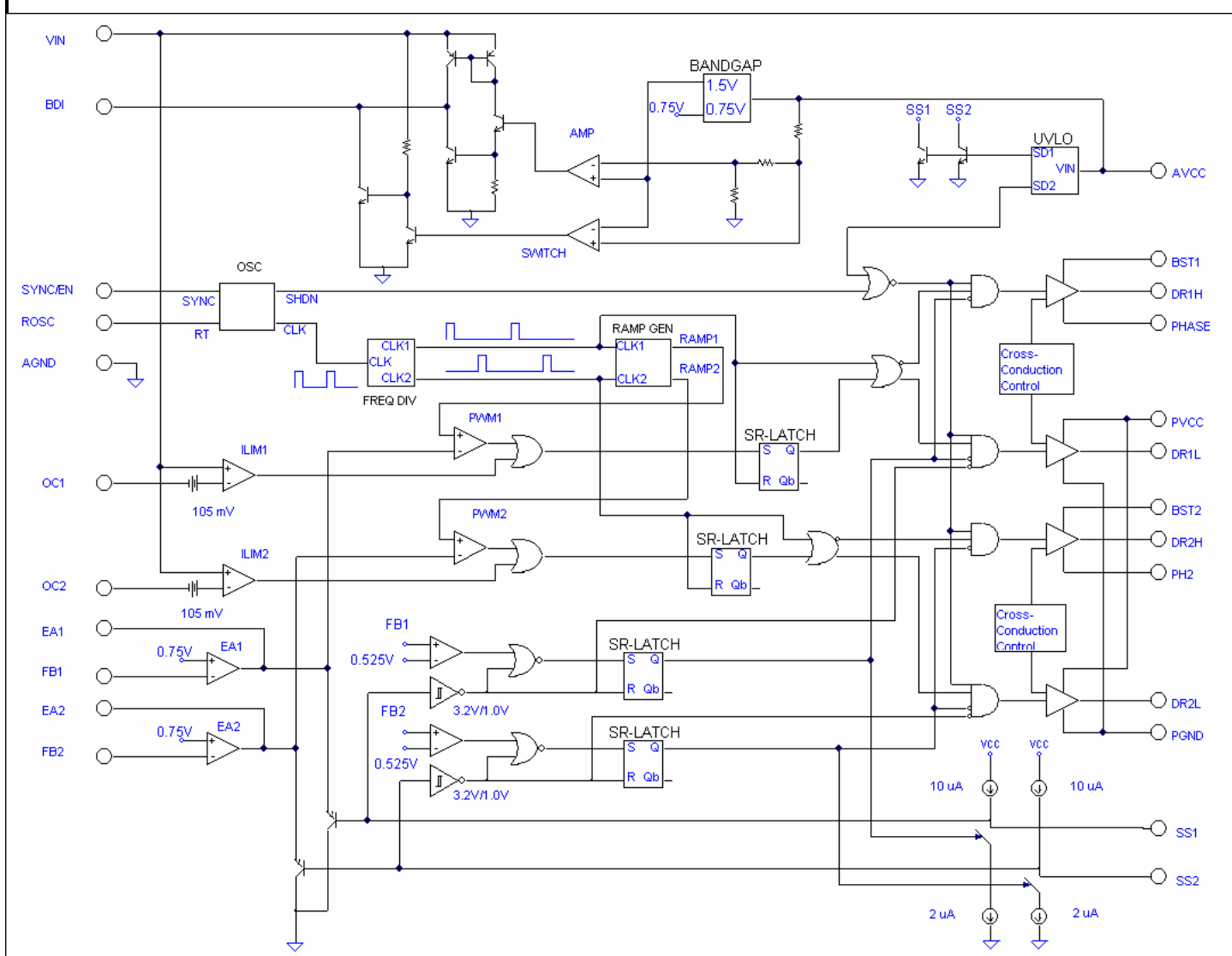
## POWER MANAGEMENT

### Pin Descriptions

Pin #	Pin Name	Pin Function
1	AVCC	Supply voltage for analog circuit. Regulated by the BDI pin to 7V from VIN using an external PNP transistor.
2	BDI	Base drive for AVCC/PVCC regulator.
3	VIN	Input supply voltage. Maximum is 30V.
4	OC1	High side current sense for VOUT1. Threshold is 100 mV.
5	EA1	Error amplifier output for compensation for the VOUT1.
6	FB1	Feedback input for the VOUT1.
7	SS1	Soft start pin for VOUT1. A capacitor to AGND sets the soft start period.
8	BST1	Boost capacitor connection for the VOUT1 high side gate drive. Connect an external capacitor and a diode as shown in the Typical Application Circuit.
9	GD1H	Gate drive for the high side MOSFET of VOUT1. 180 degrees out of phase with GD2H.
10	PH1	Switching node for VOUT1 external inductor connection.
11	GD1L	Gate drive for low side MOSFET of VOUT1.
12	PGND	Power ground for gate drive return currents.
13	PVCC	Supply voltage for output drivers.
14	GD2L	Gate drive for low side MOSFET of VOUT2.
15	PH2	Switching node for VOUT2 external inductor connection.
16	GD2H	Gate drive for the high side MOSFET of VOUT2. 180 degrees out of phase with GD1H.
17	BST2	Boost capacitor connection for the VOUT2 high side gate drive. Connect an external capacitor and a diode as shown in the Typical Application Circuit.
18	SS2	Soft start pin for VOUT2. A capacitor to AGND sets the soft start period.
19	FB2	Feedback input for the VOUT2.
20	EA2	Error amplifier output for compensation for the VOUT2.
21	OC2	High side current sense for VOUT2. Threshold is 100 mV.
22	SYNC/EN	Oscillator synchronization and PWM Enable pin.
23	ROSC	Oscillator frequency programming pin. Connect a resistor to AGND to set clock frequency.
24	AGND	Analog signal ground.

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## Block Diagram



**POWER MANAGEMENT****Application Information****Undervoltage Lockout**

The undervoltage lockout circuitry monitors the AVCC pin. During undervoltage lockout all output drives are turned off and both SS pins are discharged to ground. Typically, for AVCC increasing, normal operation will not occur until AVCC reaches 4.6V. For AVCC falling, undervoltage lockout will not occur until AVCC falls below 4.5V.

**Voltage Regulator**

Using an external PNP transistor as shown in the Typical Applications Circuit, the SC2442 provide a regulated AVCC supply. The same AVCC with adequate filtering can be connected to PVCC to provide power for the output drives. The AVCC is regulated at 7V typical which provides optimum drive for most low Voltage power MOSFETs. The BDI pin will provide at least 3 mA to regulate the external PNP.

For VIN voltages below 8V, the PNP pass transistor will always be operating in saturation and it is recommended to connect VIN directly to AVCC and PVCC so long as maximum input voltage is below 8V. The BDI pin may be left unconnected. Alternately if an additional supply <8V is available in addition to VIN, it can be used for separate powering both the VCCs.

**Soft Start and Hiccup Mode**

The SC2442 controller utilises asynchronous start up to provide glitch free output rise times. During start up, the SS1 and SS2 pins are held low and the gate drive signals are also pulled low. Once AVCC reaches 4.6V and above, the SS capacitors are charged by a 10  $\mu$ A internal current source. The error amplifier outputs are clamped by the respective SSx voltages. As the SSx pin voltage goes above the oscillator valley voltage of 1.5V, the high-side driver will begin switching. The low-side driver will not begin switching until the SSx voltage has reached 3.3V.

During normal operation, the SC2442 will enter hiccup mode if the SS pin voltage is above 3.3V and the FB pin voltage is below 0.525V (70% of 0.750V). If this occurs the GDxH and GDxL signals will go low and the SS pin will begin to sink 2  $\mu$ A. The 2  $\mu$ A of sink current will slowly discharge the SS capacitor until its voltage reaches 1V, which will trigger the SS pin to begin sourcing 10  $\mu$ A. The convertor will operate in the asynchronous mode during hiccup.

**Sync and Enable**

When the SYNC/EN pin is pulled below 1V, all output drives are turned off and both SS pins are discharged to ground. When the SYNC/EN pin is pulled high above 1.8V, normal operation occurs. When an external clock signal is applied that is marginally higher in frequency to that set by the ROSC resistor, the internal oscillator will synchronize to this signal. The external signal should have TTL compatible transition.

**Operating Frequency**

The operating frequency is set by a resistor from ROSC pin to AGND. ROSC sets the clock frequency  $F_c$  that is twice the operating frequency of each convertor. The clock frequency is given by

$$F_c = 30,000 / \text{ROSC}$$

$F_c$  is in kHz and ROSC is in kOhm.

**Current Limiting**

The SC2442 provides cycle-by-cycle current limiting by sensing the current in the input line. A non inductive resistor should be used for precise current sensing and limiting. When the voltage drop across a sense resistor in the input line exceeds 105 mV, the PWM pulse is latched off and is not reset until the next clock cycle. Overcurrent condition affects only the high side driver. An RC filter should be placed across the sense resistor as shown in the Typical Application Circuit to reduce noise due to turn-on spikes. The filter capacitor should be connected between VIN and respective OCx pins for proper filtering. Typically a ceramic or similar low esr capacitor is placed between the current sense resistor and the switching circuit. If this capacitor value is large, it can significantly distort the current feedback waveform across the sense resistors. This should be taken into account while designing the overcurrent protection circuit.

**Gate Drive Considerations**

The SC2442 provides high side gate drive with bootstrapping as shown in the Typical Application Circuit. A ceramic capacitor is recommended between each BSTx pin to the corresponding Phase Node. Each gate drive can source and sink a minimum of 0.5A current with 100 nS dead time between transistions to prevent shoot throughs.

Fig 1) Application Circuit for 5V to 3.3V/1.8V Low Power Dual Synchronous Buck Convertor

Fig 2) Input and output rise times with full load



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## Application Information (Contd)

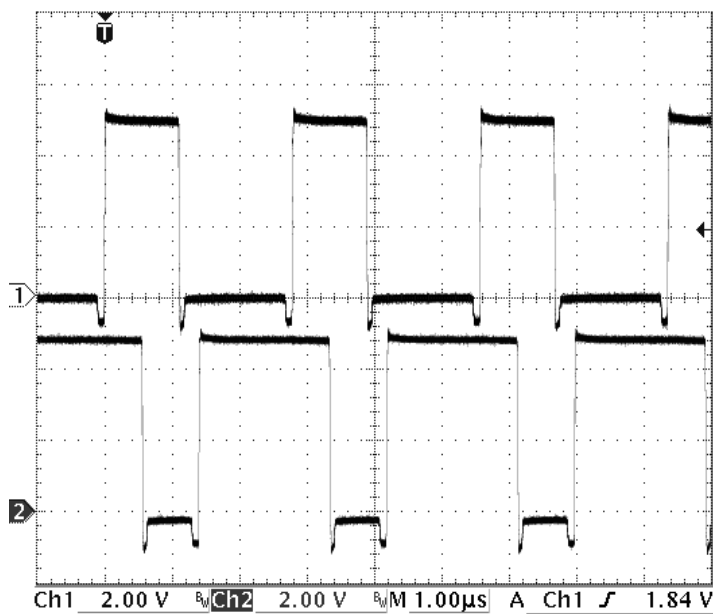


Fig 3) Switching waveforms at Phase Node with full load.  
Top trace: 1.8V/1A Bottom trace: 3.3V/0.6A

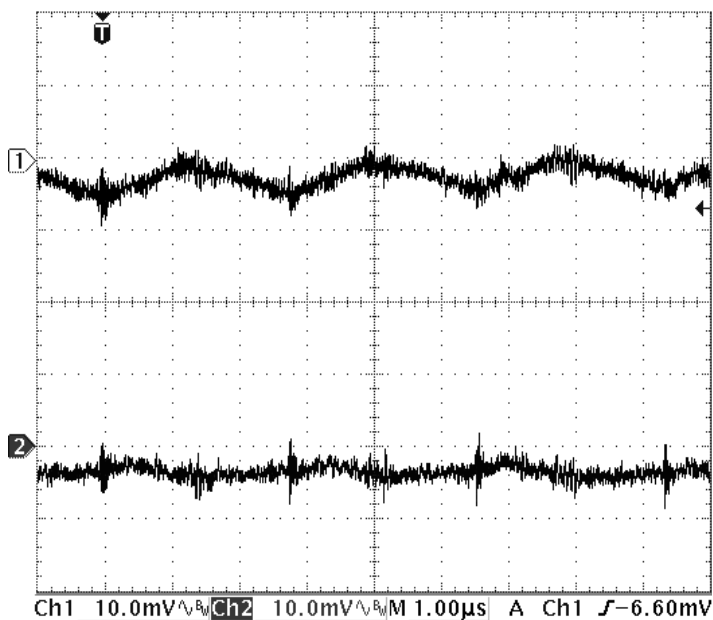


Fig 4) Output ripple and noise at full load  
Top trace: 3.3V Output Bottom trace: 1.8V Output

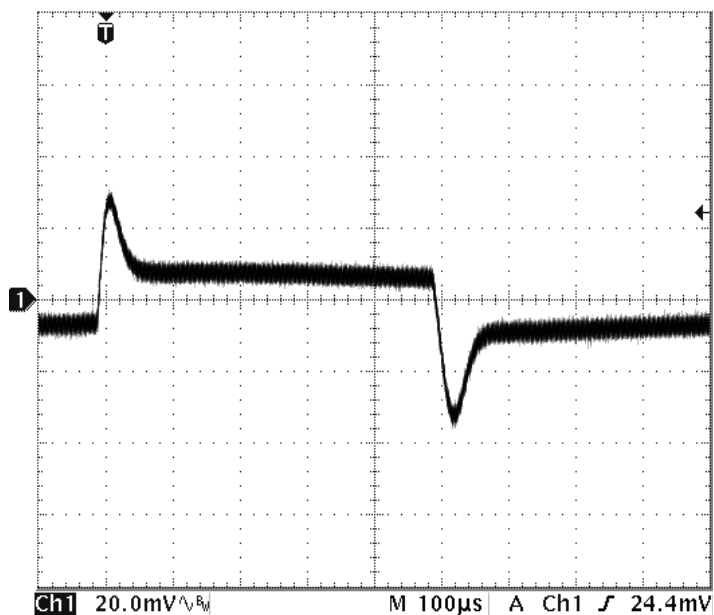


Fig 5) 1.8V Transient response for 10% to 100% step load

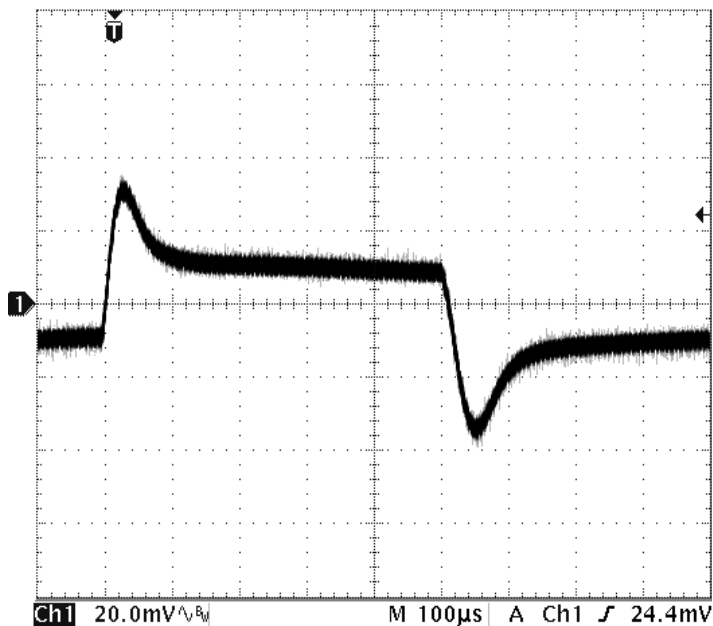
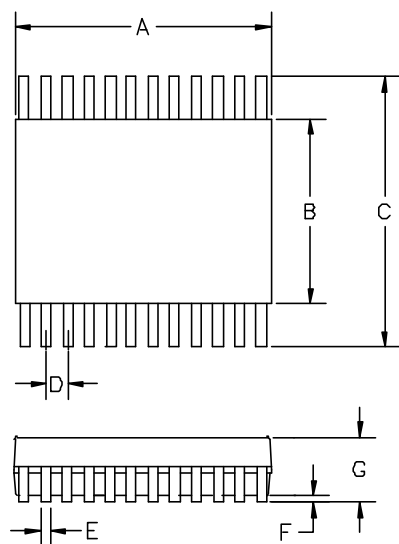


Fig 6) 3.3V Transient response for 10% to 100% step load

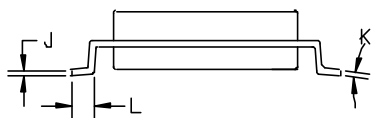
## POWER MANAGEMENT

### Outline Drawing - TSSOP-24



DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3031	.3110	7.70	7.90	②
B	.169	.177	4.30	4.50	②
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0020	.0060	.05	.15	—
G		.047		1.20	—
J	.0035	.0079	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

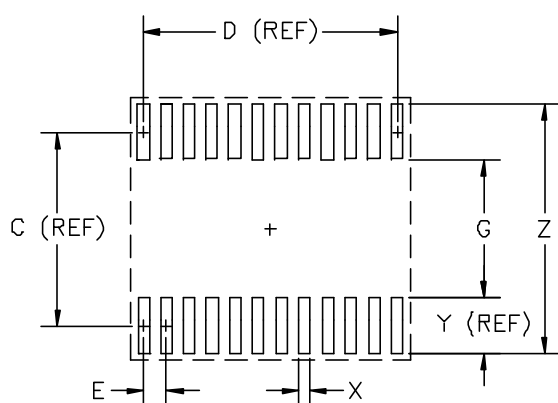
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② DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

① CONTROLLING DIMENSIONS: MILLIMETERS.

### Land Pattern - TSSOP-24



DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.218	—	5.53	REF
D	—	.282	—	7.15	REF
E	—	.026	—	0.65	BSC
G	.155	—	3.947	—	—
X	—	.013	—	0.323	REF
Y	—	.062	—	1.583	—
Z	—	.280	—	7.113	—

② GRID PLACEMENT COURTYARD IS 16 X 15 ELEMENTS (8mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

① CONTROLLING DIMENSIONS: MILLIMETERS.

### Contact Information

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