

RHINE

STS-48 POS/ATM SONET MAPPER

ADVANCED SUMMARY DATASHEET

Features

- Provides a SONET/SDH STS-48/STM-16, 4 STS-12/STM-4, or 16 STS-3/STM-1 line interfaces.
- STS-48/STM-16 data stream supports a single STS-48c/AU-4-16c, or any valid combination of STS-12c/AU-4-4c and/or STS-3c/AU-4 SONET/SDH payloads.
- Each STS-12/STM-4 data stream supports a single STS-12c/AU-4-4c or 4 STS-3c/AU-4 SONET/SDH payloads.
- Each STS-3/STM-1 data stream supports a single STS-3c/AU-4 SONET/SDH payload.
- Provides full-duplex mapping of ATM cells or packets in each payload tributary.
- Terminates/generates SONET/SDH section, line, and path layers with transport/section E1, E2, F1, and DCC overhead interfaces in both transmit and receive directions.
- Optional path switching configuration for STS-12 or STS-3c UPSR, or other applications that require redundancy. Optional software control of this function.
- APS port to support protection-switching configurations between 2 RHINE devices.
- 16-bit, bus interface at 155 MHz for STS-48/STM-16 mode, or serial interfaces operating at 622/155 MHz for STS-12/3 (STM-4/1) modes on the line side.
- 32-bit, parallel interface (FlexBus-3™) operating at 100 MHz on the system side.
- .25 micron, 2.5V core, and 3.3V tolerant I/O.

- Packaged in a 624 Pin CBGA.

The S4804 is a highly-integrated VLSI device that provides full-duplex mapping of packets or ATM cells to SONET/SDH payloads. It provides support for both uni-directional and bi-directional rings.

The S4804 provides full section, line, and path overhead processing, and supports framing, scrambling/descrambling, alarm signal insertion/detection, and bit-interleaved parity (B1/B2/B3) processing.

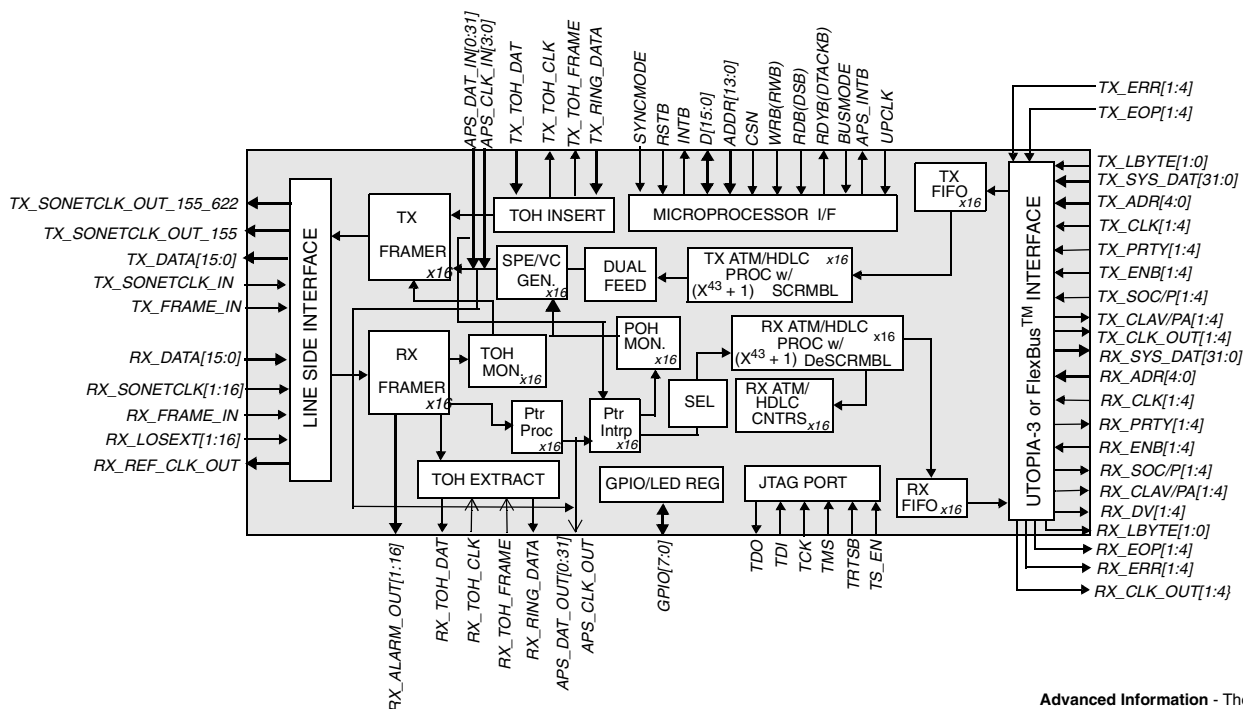
The S4804 is SONET/SDH standards compliant with Bellcore GR-253, ITU G.707, ITU-T 432.1, ANSI T1.105 -1995, and IETF RFCs 1619/1661/1662.

A general purpose 8-bit or 16-bit microprocessor interface is provided for control and monitoring. The interface supports both Intel™ and Motorola™ type microprocessors, and is capable of operating in either an interrupt-driven or polled-mode configuration. In addition, a standard 5 signal IEEE 1149.1 JTAG Test Port is provided for Boundary Scan test purposes.

Applications

- ATM switches
- Packet over SONET Routers and Switches
- SONET/SDH Add Drop Multiplexers, Terminal Multiplexers, and Digital Cross Connects
- Test equipment

S4804 Block Diagram



Advanced Information - The information contained in this document is about a product in its design phase and is subject to change without notice at any time. All features described herein are design goals. Contact AMCC for updates to this document and the latest product status.

S4804 STS-48 POS/ATM SONET MAPPER**ADVANCED SUMMARY DATASHEET****Overview and Applications****SONET Processing**

The S4804 implements SONET/SDH processing and full-duplex ATM/packet-mapping functions for STS-48/STM-16, STS-12/STM-4, or STS-3/STM-1 data streams. It can support either a single STS-48c/AU-4-16c or any valid combination of STS-12c/AU-4-4c or STS-3c/AU-4 signals within an STS-48/STM-16. The S4804 also supports 4 STS-12/STM-4 signals (each containing a single STS-12c/AU-4-4c or 4 STS-3c/AU-4), or 16 STS-3c/STM-1 signals each containing an STS-3c/AU-4. A TOH/SOH interface provides direct add/drop capability for E1, E2, F1, and both Section and Line DCC channels. The S4804 also includes a clear channel mode that enables the direct transmission of system payload from the system interface to the line-side interface.

On the transmit side, the S4804 generates section, line, and path overhead. It performs framing pattern insertion (A1, A2), scrambling, alarm-signal insertion, and generates section, line, and path Bit Interleaved Parity (B1/B2/B3) for far-end performance monitoring.

On the receive side, the S4804 processes section, line, and path overhead. It performs framing (A1, A2), descrambling, alarm detection, pointer processing, Bit Interleaved Parity monitoring (B1/B2/B3), and error-count accumulation for performance monitoring.

ATM Processing

When configured for ATM cell processing, the S4804's transmit ATM processor(s) will perform all necessary cell processing as defined by ATM UNI3.1, ITU-T I.432.1, and I.432.2.

HDLC Processing

When configured for POS mode, the S4804's HDLC processor(s) provides HDLC packet processing as defined by IETF RFCs 1619 and 1662. In addition, the S4804 optionally performs scrambling ($X^{43}+1$), either pre-HDLC or post-HDLC processing.

Redundancy Features

For any of its multi-line interface configurations, the S4804 provides redundancy functionality on a per-path basis. In the transmit direction, a single signal is dual-fed to 2 separate SONET processing blocks. In the receive direction, the S4804 provides automatic switching between 2 received signals, based on the status of the SONET path. Switching can be performed based on line or path status, or the user can simply control the switch via the management interface.

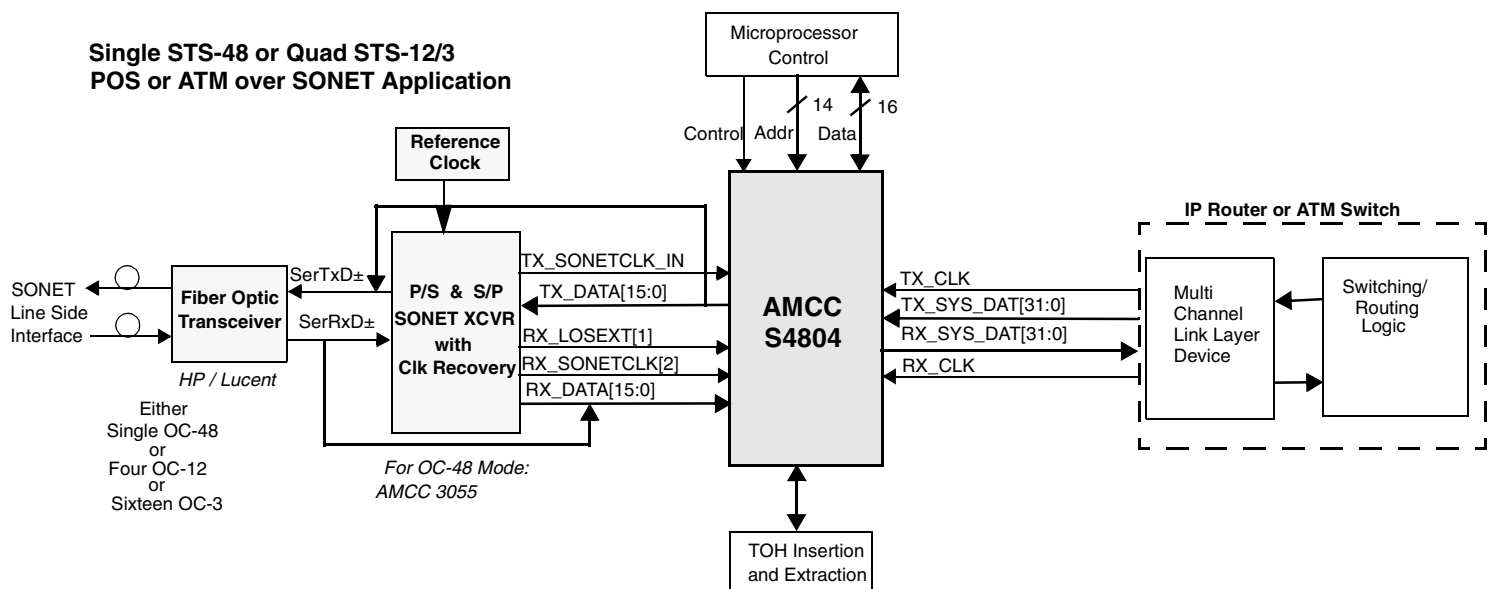
The S4804 also provides APS input and output interfaces to convey signals between 2 S4804 devices configured for APS operation. This configuration supports both 1+1 and 1:1 configurations.

Line-side Interface

On the line side, the S4804 supports a 16-bit parallel interface, operating at 155MHz for a single OC-48 optical interface. It provides serial interfaces at either 622 MHz or 155 MHz for OC-12 and/or OC-3 optical interfaces.

System Interface

The S4804 supports a 32-bit, 100-MHz system interface. For ATM cell transfers, the S4804 supports Utopia Level 3 interface. For packet transfers, the S4804 supports FlexBus™ interface. The S4804 also provides support for a quad, 8-bit extension of the Utopia 3.

TYPICAL APPLICATIONS: S4804 in 2.488 Mb/s ATM or POS System**AMCC**

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