

# S3090

## 10 Gbps Transimpedance Amplifier

### DEVICE SPECIFICATION DATA SHEET

#### FEATURES

- 10 GHz Bandwidth
- 1.4 k $\Omega$  Differential Transimpedance
- -5.2 V Power Supply
- 15 pA/rt Hz Typical Noise Current Density
- 2.2 mA p-p Max Input Current
- Low Pulse Width Distortion
- Source Terminated Differential Outputs
- Adjustable Output Offset
- Maximum Die Size: 1.946 mm by 1.946 mm

#### APPLICATIONS

- SONET OC-192
- Fiber Optic Data Links
- HDTV/CATV Fiber Links
- Fiber Optics Access Boxes
- 10 G Ethernet Fiber Links

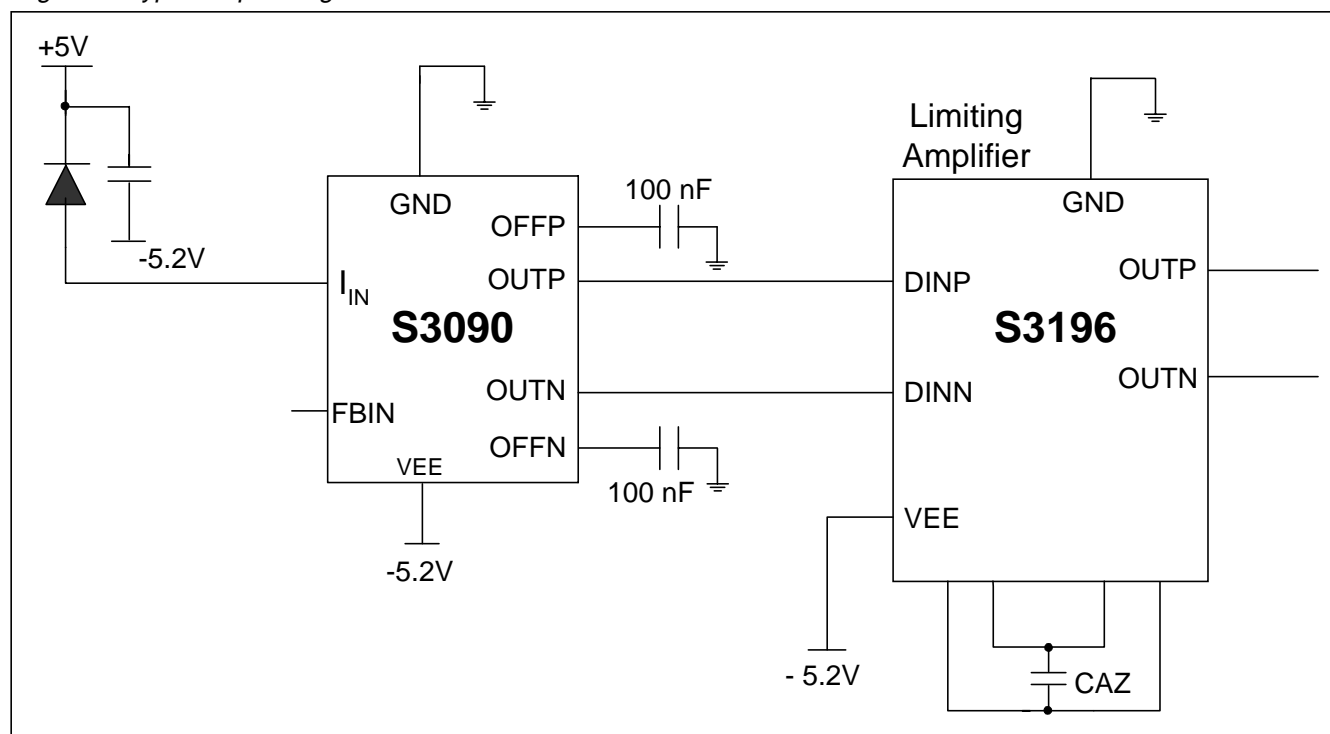
#### GENERAL DESCRIPTION

The S3090 is a high-speed transimpedance amplifier for 10 Gbps applications. Input currents as high 2.2 mA can be amplified with low duty cycle distortion. The low input noise allows signals down to 19  $\mu$ A (peak) to be detected with a signal to noise ratio of 21.5 dB (allows for BER < 1E-9).

The outputs are voltage limited to 1400 mV, differential, in order to allow a wide input dynamic range without exceeding the input voltage range of the limiting amplifier.

Also, the offset between the data outputs is adjustable, in order to provide adjustable decision threshold in the limiting amplifier. Figure 1 shows a typical application.

Figure 1. Typical Operating Circuit



## DETAILED DESCRIPTION

Figure 2 depicts the block diagram of the S3090 transimpedance amplifier. The amplifier circuitry consists of a transimpedance stage and an output stage with a gain of 7.3 dB. The output is linear for inputs of up to 1000  $\mu$ A (peak). For higher inputs the output will limit at a level of 1400 mV, differential.

The S3090 provides a feature which enables the adjustment of the decision threshold at the input of the limiting amplifier by allowing the adjustment of the DC

offset between the two complimentary data outputs, OUTP and OUTN. The OFFP and OFFN outputs provide the DC levels for the data outputs OUTP and OUTN. They can be used as inputs to a circuit that would control the DC offset,  $V_{\text{OFFSET}}$ , between OUTP and OUTN. This offset can be controlled by adjusting a DC voltage at the FBIN input. OFFP and OFFN should be connected to ground through capacitors. A plot of FBIN vs.  $V_{\text{OFFSET}}$  is provided in Figure 6.

Figure 2. S3090 Detailed Block Diagram

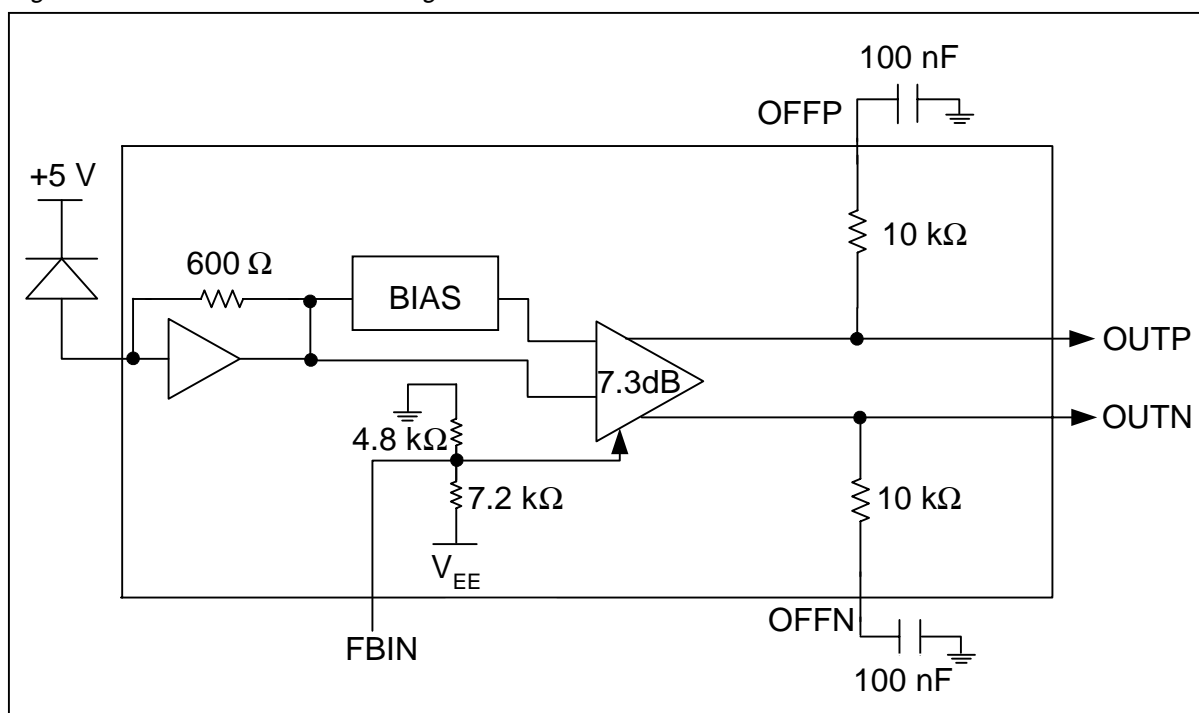


Table 1. Pad Assignment and Description

Pin Name	I/O	Pad #	Coordinate (X,Y) <sup>1</sup>	Description
GND	S	1 7 8 9 11 13 14 15 17 19 21 22 23 24 26 27 28	[292.175, 88.925] [1485.375, 88.925] [1689.075, 253.000] [1689.075, 519.125] [1689.075, 889.050] [1689.075, 1258.975] [1689.075, 1524.975] [1485.375, 1689.075] [1087.650, 1689.075] [689.925, 1689.075] [292.175, 1689.075] [99.075, 1524.975] [99.075, 1326.100] [99.075, 1127.225] [99.075, 650.725] [99.075, 451.850] [99.075, 252.975]	Ground
VEE	S	2 3 4 5 6	[491.050, 88.925] [689.925, 88.925] [888.800, 88.925] [1087.650, 88.925] [1286.500, 88.925]	Negative power supply
I <sub>IN</sub>	I	25	[99.075, 889.050]	PIN diode input
OUTP	O	12	[1689.075, 1087.925]	Positive output
OUTN	O	10	[1689.075, 690.175]	Negative output
OFFP	O	18	[888.800, 1689.075]	DC level of OUTP. This pad should be connected to ground through a 100 nF capacitor.
OFFN	O	16	[1286.500, 1689.075]	DC level of OUTN. This pad should be connected to ground through a 100 nF capacitor.
FBIN	I	20	[491.050, 1689.075]	A DC voltage at this pin controls the offset between OUTP and OUTN. -2V corresponds to no offset. (See Table 5).

1. The coordinates are in  $\mu\text{m}$  from the lower left corner of the circuit die to the center of the pad.

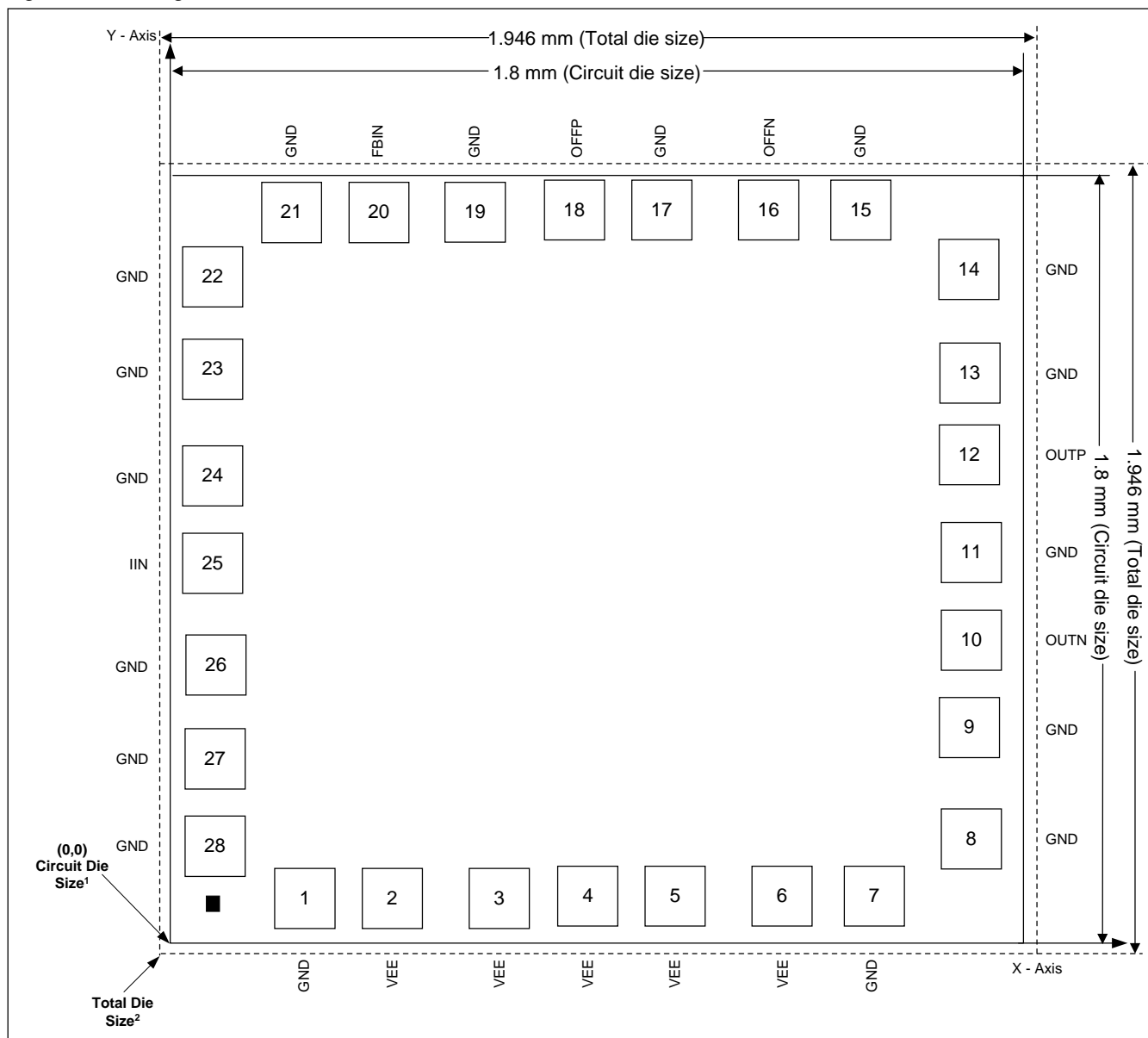
2. Total pad size is  $94\ \mu\text{m} \times 94\ \mu\text{m}$ . The size of the exposed area is  $80\ \mu\text{m} \times 80\ \mu\text{m}$ .

3. The back of the die is not metallized and should be connected to  $V_{EE}$  or left electrically unconnected.

### Die Issues

Die level test only. Test includes wafer probe, low frequency functional test, parametric test on I/O and power pins, and visual inspection.

Figure 3. Bonding Pad Location



Note: Die thickness is 0.254 mm (10 mils).

1. The circuit die size is the smallest possible size of the die. The lower left-hand corner of the circuit die is the origin of the xy-coordinate system. Pad coordinates indicated in Table 1 are measured from this origin to the pad's center.
2. The total die size is the largest possible size of the die. It includes a splicing area around the circuit die. The actual size of any given die may vary in size from the minimum (circuit die) size to the maximum (total die) size.

The following are the absolute maximum stress ratings for the S3090 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only and operation of the device at the maximums stated or any other

conditions beyond those indicated in the “Recommended Operating Conditions” of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Description
$T_j$	-20		100	°C	Junction temperature under bias
$T_A$	-40		85	°C	Ambient temperature under bias
VEE	-4.9	-5.2	-5.5	V	Voltage on VEE with respect to GND

Table 3. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature Range	-55		150	°C
Power Supply VEE	-6		0.5	V

**Electrostatic Discharge (ESD) Ratings**

The S3090 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 400 V, except the IIN pin. The IIN pin is rated at 100 V.

Table 4. AC Electrical Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
$Z_T$	AC Transimpedance	550	700	825	V/A	Single-ended, 50 $\Omega$ load
$Z_T$	AC Transimpedance	1100	1400	1650	V/A	Differential, 100 $\Omega$ load, line to line
BW <sub>-3dB</sub>	-3 dB Bandwidth	7.5	10	13	GHz	See Note 1.
BW <sub>LF</sub>	Low Frequency -3dB Cutoff		25	40	kHz	
$I_{PK}$	Peak Input Current			2.2	mA	
$I_{ND}$	Input Noise Current Density		15	18	pA/rt Hz	0 - 11 GHz
$I_{NOISE}$	Input Noise Current Power		2.5E - 12	3.5E - 12	A <sup>2</sup>	0 - 11 GHz
$V_{OD}$	Maximum Output Swing			1400	mV	Peak to peak differential. 100 $\Omega$ line-to-line termination.
$V_{OS}$	Maximum Output Swing			700	mV	Single-ended, 50 $\Omega$ line termination to GND.
$I_{IN, LIM}$	Input Current at which Output Limits		1000		$\mu$ A	
$R_{OUT}$	Output Impedance	42	50	58	$\Omega$	0 - 11 GHz, single ended

Table 4. AC Electrical Characteristics (Continued)

Parameter	Description	Min	Typ	Max	Units	Conditions
$S_{22}$	Output Reflection Coefficient			-10	dB	1 - 7 GHz, < 800 pH bond wire inductance
Ripple	Output Ripple	-0.5	0	0.5	dB	1 - 8 GHz. See Note 1.
Group Delay	Group Delay Deviation (100 MHz to 8 GHz)			20	ps	Input Current = 10 - 1000 $\mu$ A. See Note 1.
Group Delay	Group Delay Deviation (8 GHz to $F_{-3dB}$ )			40	ps	Input Current = 10 - 1000 $\mu$ A. See Note 1.
Peak	Peaking			1.2	dB	25 kHz to 11 GHz. See Note 1.
$J_T$	Total Jitter (Pk to Pk) (At 1E-12 BER)			0.12	UI	$I_{IN} = 2.2$ mA

Note 1. Assuming a total input bond wire inductance (between the photodiode and IIN pin) of 0.7 nH and photodiode capacitance of 0.2 pF.

Table 5. Output Offset Adjustment

Parameter	Description	Min	Typ	Max	Units	Conditions
$V_{OFFSET}$	$V_{DOUTP} - V_{DOUTN}$	200			mV	DC Voltage
$V_{OFFSET, NEG}$	$V_{DOUTN} - V_{DOUTP}$	200			mV	DC Voltage
$V_{FBIN, MIN}$	$V_{FBIN}$ corresponding to max positive $V_{OFFSET}$		-3		V	$V_{OFFSET} = +200$ mV
$V_{FBIN, NOM}$	$V_{FBIN}$ corresponding to zero $V_{OFFSET}$		-2.0		V	$V_{OFFSET} = 0$
$V_{FBIN, MAX}$	$V_{FBIN}$ corresponding to max negative $V_{OFFSET}$		-1		V	$V_{OFFSET} = -200$ mV
$R_{FBIN}$	FBIN Input Impedance		2.88		k $\Omega$	

Table 6. DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
$I_{EE}$	Supply Current		80	90	mA	
$V_{INBIAS}$	Input Bias Voltage		$V_{EE} + 1.7$		V	
$V_{OCM}$	Common Mode Output Voltage	Gnd - 0.7	GND - 0.45	Gnd - 0.2	V	50 $\Omega$ line termination to GND.
$V_{OCM}$	Common Mode Output Voltage	Gnd - 1.4	GND - 0.9	Gnd - 0.4	V	100 $\Omega$ line-to-line termination.

### Typical Operating Characteristics

Figure 4. Frequency Response (Gain vs. Frequency)

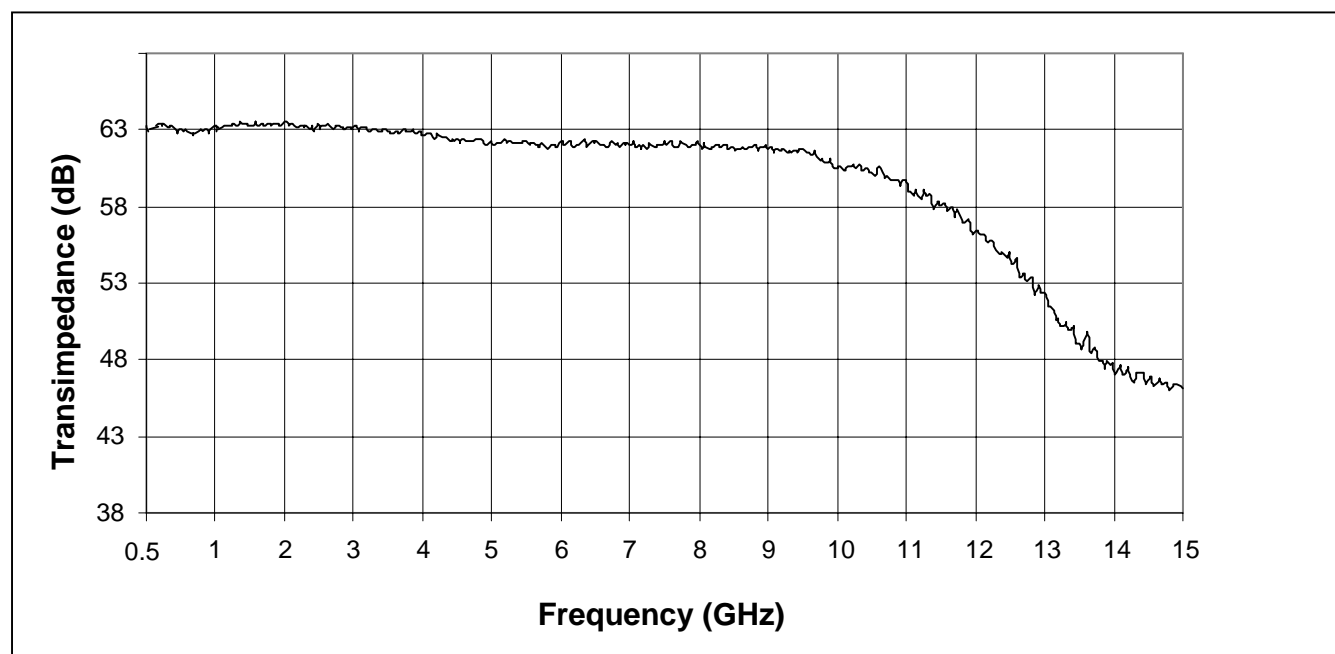


Figure 5. Eye Diagram (10 Gbps PRBS pattern,  $I_{IN} = 1\text{ mA}$ )

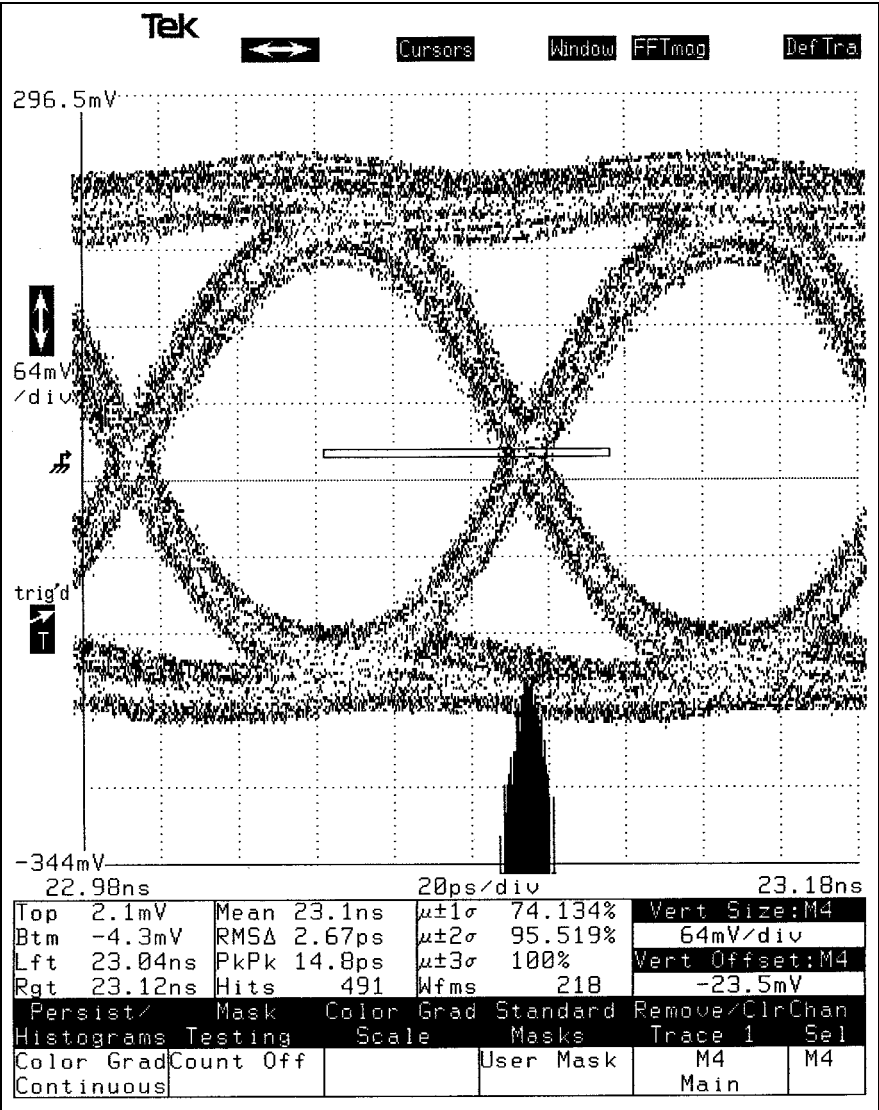




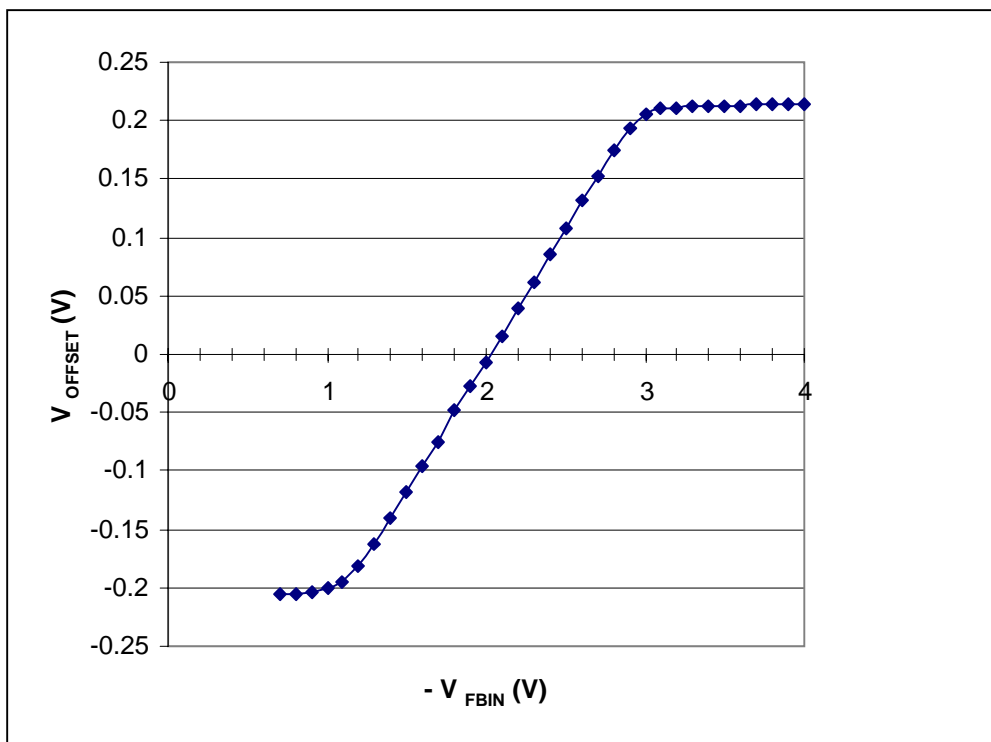
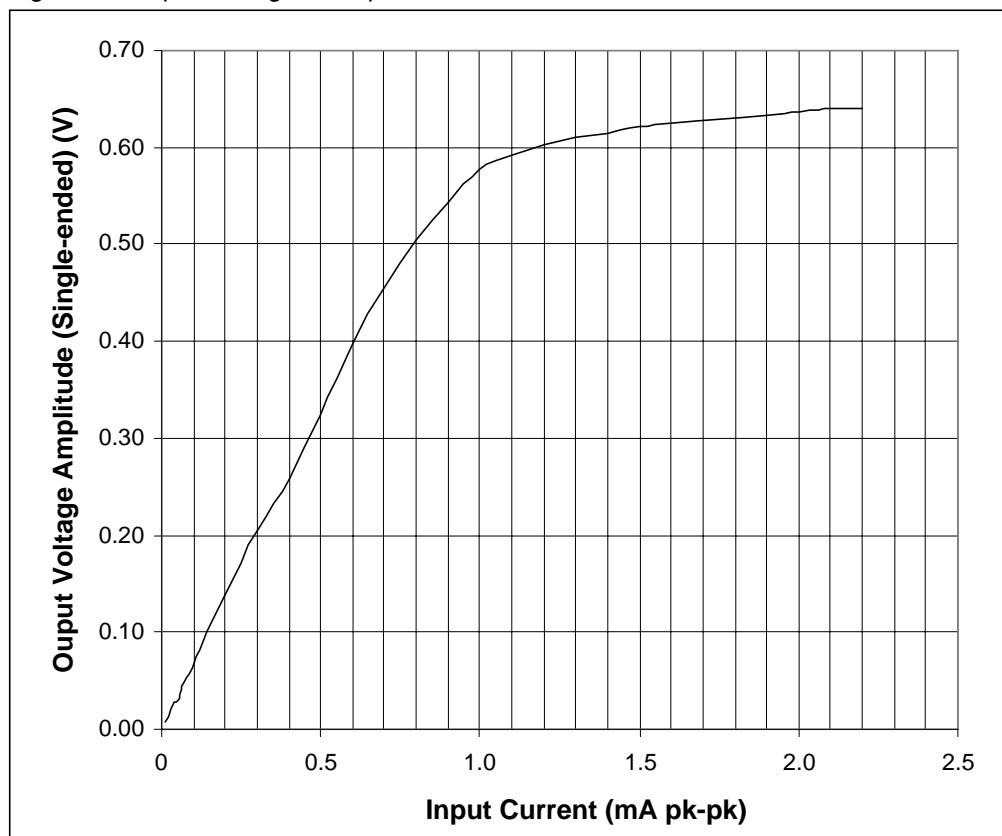
Figure 6.  $F_{\text{BIN}}$  vs.  $V_{\text{OFFSET}}$ 

Figure 7. Output Voltage vs. Input Current



## Ordering Information

Prefix	Device	Package
S – Integrated Circuit	3090	DI – Die

X

Prefix

XXXX

Device

XX

Package



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