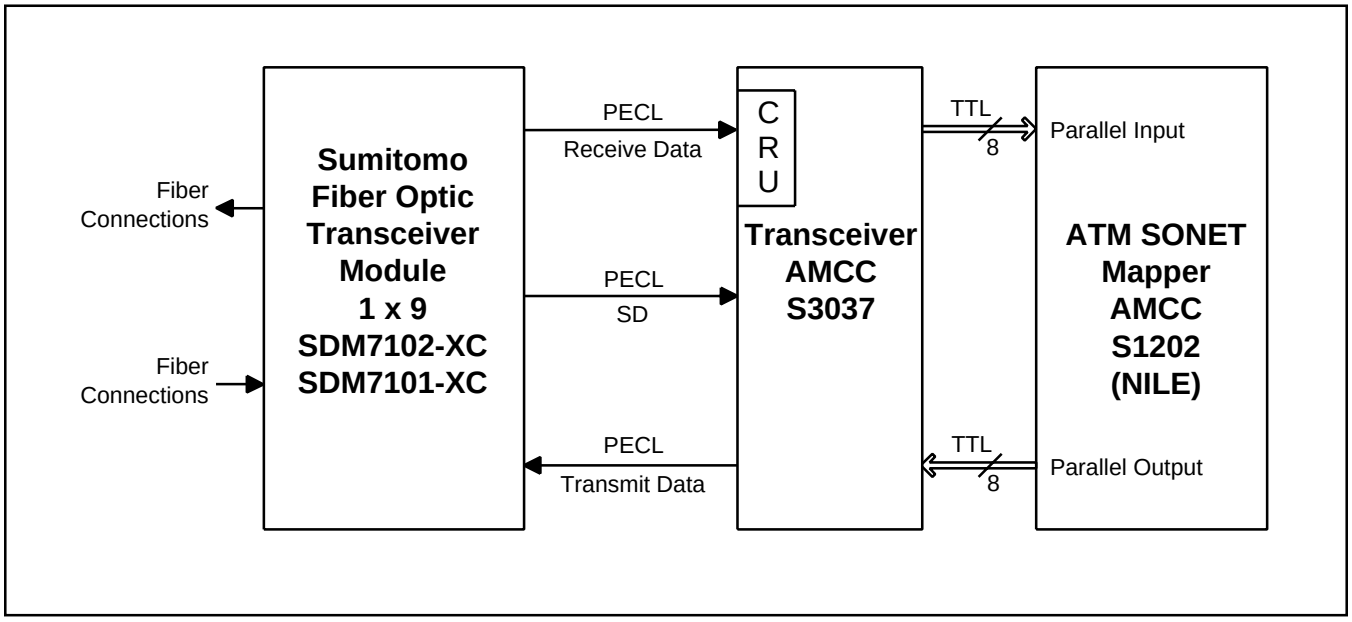
S3037, S1202 NILE, AND SUMITOMO 5 V FIBER OPTIC XCVR APPLICATION NOTE

INTRODUCTION

The AMCC S3037 SONET/SDH transceiver and clock recovery chip is a fully integrated serialization/ deserialization SONET STS-12/STM-4 (622.08 Mbps) and STS-3/STM-1 (155.52 Mbps) interface device. This device is suitable for SONET-based ATM applications. The AMCC S3037 transceiver chip provides the first stage of digital processing of a receive and a transmit SONET STS-3/STM-1 or STS-12/STS-4 bit serial stream.

In the receive path it converts a bit-serial data stream into a byte-serial data (parallel data) format, and in the transmit path it converts byte-serial data (parallel data) into bit-serial data. Figure 1 shows an application block diagram with an AMCC S3037 and a Sumitomo 1 x 9 fiber optic transceiver. Figure 2 shows specifically the design details of connecting the 5 V Sumitomo fiber optics to the 3.3 V AMCC S3037. Combining these devices provides a Physical Media Dependent (PMD) layer for SONET/SDH data transfer.

Figure 1. Typical Network Application Block Diagram with a 1 x 9 Fiber Optic Transceiver with CRU



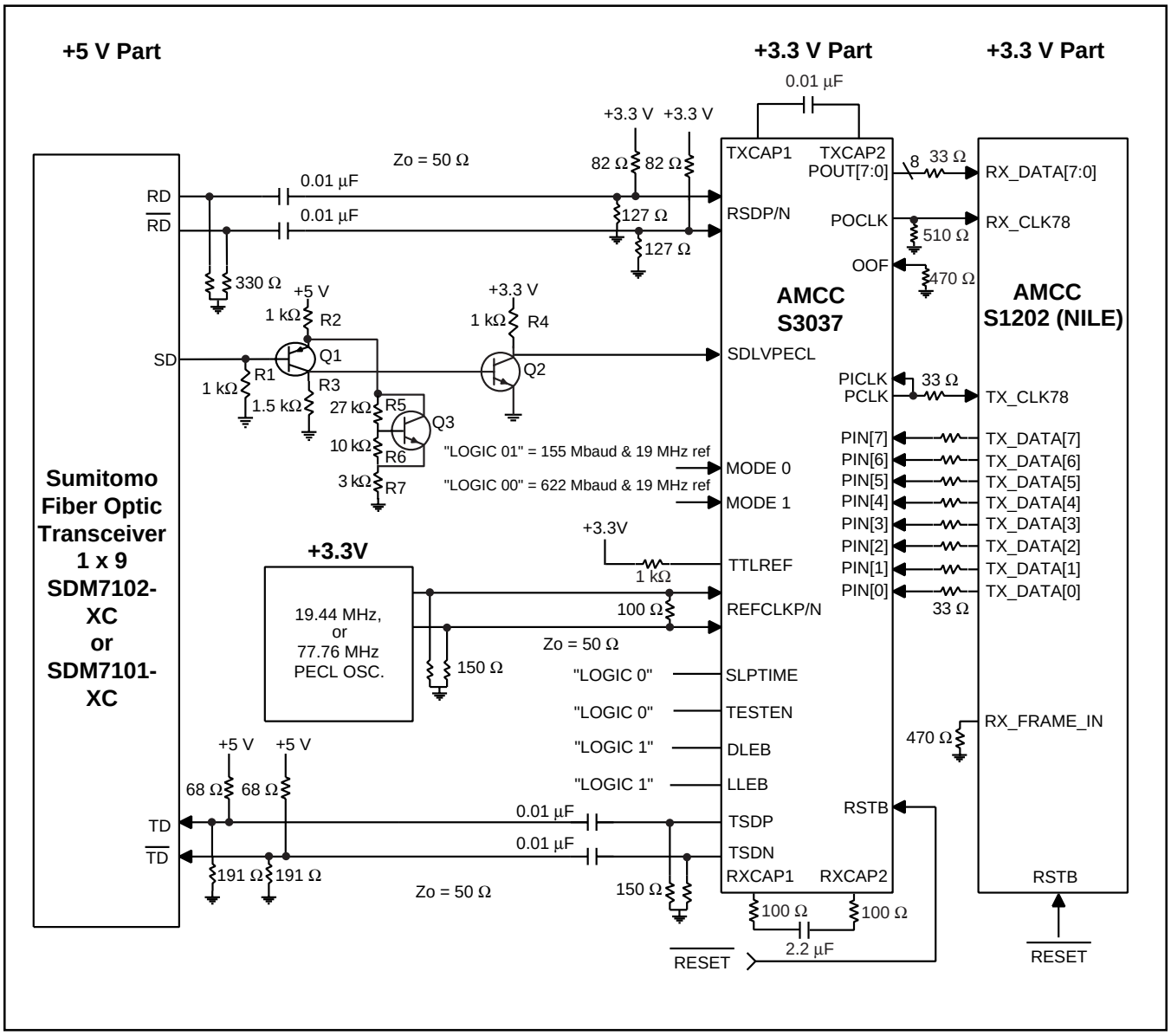
Note: CRU = Clock Recovery Unit

Signal Connect Description

Figure 1 shows the block diagram of this solution.

1. The Sumitomo SDM7102-XC (for OC-12 intermediate reach applications) or SDM7101-XC (for OC-3 intermediate reach applications) fiber optic transceivers interface to the AMCC S3037 with bit-serial data stream. The clock is recovered within the S3037.
2. The AMCC S3037 converts the bit-serial data to 8-bit parallel data, and outputs the data to the S1202 (NILE) via an 8-bit parallel TTL interface.
3. The S1202 (NILE) transmits 8-bit parallel data to the AMCC S3037 via a TTL interface.
4. The AMCC S3037 transmits the bit-serial data to the fiber optic transceiver via a PECL interface.

Figure 2. AMCC S3037, Sumitomo SDM7102-XC or SDM7101-XC 1 x 9 Fiber Optic Transceiver and AMCC S1202 (NILE) Block Diagram



Notes:
1. The SDM7101-XC is for OC-3 intermediate reach applications.
2. The SDM7102-XC is for OC-12 intermediate reach applications.
3. The minimum TTL Output High Voltage (V_{OH}) for the S3037 is +2.1 V. Therefore, any +5 V TTL input that must be driven by the S3037 should be capable of detecting a minimum Input High Voltage (V_{IH}) of less than 2.1 V.

Parts List

The following is a parts list that is a recommendation for the designer to implement the circuit in Figure 2.

QTY	Part # or equivalent	Description
4		Resistor, 1 kΩ, 10% 1/8W, 805 or 603 package size
4		Resistor, 150 Ω, 10%, 1/8W, 805 or 603 package size
1		Resistor, 1.5 kΩ, 10%, 1/8W, 805 or 603 package size
3		Resistor, 100 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 191 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 68 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 127 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 82 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 330 Ω, 10%, 1/8W, 805 or 603 package size
17		Resistor, 33 Ω, 10%, 1/8W, 805 or 603 package size
2		Resistor, 470 Ω, 10%, 1/8W, 805 or 603 package size
1		Resistor, 510 Ω, 10%, 1/8W, 805 or 603 package size
1		Resistor, 3 kΩ, 10%, 1/8W, 805 or 603 package size
1		Resistor, 10 kΩ, 10%, 1/8W, 805 or 603 package size
1		Resistor, 27 kΩ, 10%, 1/8W, 805 or 603 package size
5		Capacitor, 0.01 µF, 10%, X7R, 16 V, Surface Mount package
1		Capacitor, 2.2 µF, PCC 1923 CT-ND, 6.3 V ± 10%, 805 package
1	S3037	SONET/SDH/ATM OC-3/OC-12 Transceiver
1	S1202 (NILE)	AMCC S1202 (NILE)
1	SDM 7101-XC or	Sumitomo 5 V Fiber Optic 1 x 9 Transceiver for OC-3 intermediate reach applications
1	SDM 7102-XC	Sumitomo 5 V Fiber Optic 1 x 9 Transceiver for OC-12 intermediate reach applications
1		LVPECL Oscillator, 19.44 MHz or 77.76 MHz
2	MMBT3904LT1	NPN Transistor, 2N3904
1	MMBT3906LT1	PNP Transistor, 2N3906

Theory of Operation

1. The 1 x 9 transceiver converts the optical signals to electrical signals from the fiber optic input when the Signal Detect (SD output of the transceiver) is active. When the signal detect output of the transceiver is inactive, the data on the RSDP/N inputs of the S3037 transceiver will be internally forced to a constant zero.
2. The S3037 receives the STS-12/STM-4 (622.08 Mbps) or STS-3/STM-1 (155.52 Mbps) scrambled NRZ data signals on the serial data stream (RSDP/N) PECL inputs. These inputs are received into the S3037, and the S3037 recovers the clock and re-times the input data. This clock is used by the receive section as the master clock to perform framing and deserialization functions.
3. When the NILE device is in default mode (RX_FRMR_INH = 0), Out Of Frame (OOF) should be connected through a 470 Ω resistor to ground and the Frame Pulse (FP) will be inactive. The parallel data is not assumed to be byte aligned. The NILE device will align to the incoming data.
4. The bit-serial data stream is then converted into an 8-bit parallel data format for output onto the TTL Parallel Output data bus (POUT[7:0]). The 8-bit parallel data is clocked out of the S3037 and into the S1202 (NILE) with the TTL Parallel Output Clock (POCLK).
5. The 8-bit parallel data is output from the S1202 (NILE) into the S3037 TTL Parallel Data Input bus (PIN[7:0]) and is sampled by the TTL Parallel Input Clock (PICLK) of the S3037. This clock is generated by the S3037 TTL Parallel Clock (PCLK) which is fed back into the PICLK input.
6. The 8-bit parallel data is then converted to bit-serial data and output through the PECL Transmit Serial Data (TSDP/N) connections to the fiber optic transceiver inputs (TD and $\overline{TD}$).

Terminations

The following is a list of terminations that need to be added for this particular design.

1. The 100 Ω line-to-line termination resistors should be as close to the termination points as possible.
2. The 330 Ω pull down resistors should be as close to the sources as possible.
3. The high frequency traces should be designed as 50 Ω transmission lines with the termination as depicted in Figure 2.
4. All of the termination resistors should be placed at the end of the transmission line, and the power supply decoupling should be placed as close as possible to the devices. Refer to the S3037 layout applications note and Sumitomo data sheet for specific power and ground decoupling and isolation rules.
5. The PECL and LVPECL (differential pairs) traces should have equal length (allows both lines to arrive at the destination at the same time) and be run in parallel and in close proximity of one another. This allows the same noise to couple onto both of the lines and become common mode noise which is ignored by the differential inputs.
6. The 150 Ω pull down resistors set the output current of the LVPECL gate to approximately 13 mA.
7. The Single-Ended (S.E.) 5 V PECL to 3.3 V Single-Ended PECL converter was designed to meet the level shifting, reliability, and temperature requirements, and to implement the conversion with the minimum number of components. The design task is to convert 5 V PECL S.E. voltage to the proper 3.3 V PECL S.E. level. Shown on Figure 2, this conversion process is a three transistor solution.
8. AC coupling is needed between the fiber optic modules (5 V) and the rest of the system (3.3 V). The AC coupling capacitor acts as a block to DC current and allows the DC level of each side of the capacitor to be at different levels. This AC coupling capacitor has negligible impedance above 1 MHz which allows SONET/SDH signals (frequencies much higher than 1 MHz) to pass through the capacitor. On the destination side of the capacitor, the voltage dividers are designed so that the voltage swings traveling through the capacitor will be centered at the appropriate levels, one for 5 V (3.7 V) and the other for 3.3 V (2.0 V) on each side of the capacitor. The voltage swing's magnitude will be equal on both sides of the capacitor. The AC coupling capacitor should be placed as close to the source as possible, allowing the termination of the circuit to be at the destination.
9. The 33 Ω series resistors between the PIN[7:0] Parallel Input data of the AMCC S3037 and the TX_DATA[7:0] of the S1202 (NILE) should be as close to the source (S1202 outputs) as possible.
10. Separate resets should be used for the S3037 and S1202 NILE. During Reset, the PCLK of the S3037 is disabled. The NILE requires the TX_SONETCLK from the PCLK to run the microprocessor device.
11. The 510 Ω pull-down resistor should be used to improve the duty cycle on POCLK.

The S1202 (NILE) uses low impedance CMOS totempole outputs on the TX_DATA[7:0] data bus. When this output drives small capacitance loads, it is capable of very high edge rates approaching 4 V/nsec. Therefore, it has been determined for short trace lengths that 33 Ω will reduce these edge rates and minimize noise (ringing and overshoot) to sufficient levels.

In general, reducing switching edge rates to the minimum necessary to accomplish the job at hand is good design practice. It minimizes on-chip and on-board noise, reflections for non-ideal stubs and terminations, and radiated EMI. The small size and low cost of surface mount resistors make them an extremely cost effective investment in the system design.

Power Sequencing

Please note that 33 Ω is recommended on dynamically switching input signals such as PIN[7:0], PICLK, and RX_DATA[7:0] to limit overshoot and ringing. Static control lines such as LLEB, DLEB, SLPTIME, MODE[1:0], TESTEN, and RSTB should also be provided with series resistors of at least 33 Ω (100 Ω recommended).

Conclusion

The AMCC S3037, Sumitomo SDM7102-XC (for OC-12 intermediate reach applications) or SDM7101-XC (for OC-3 intermediate reach applications), and the AMCC S1202 (NILE) solution combine to make a complete STS-12/STM-4, or an STS-3/STM-1 Physical Media Dependent (PMD) layer for SONET/SDH data transfer at a rate of 622.08 Mbps or 155.52 Mbps.

Disclaimer:

The circuit presented in this application note is based on data sheet information as well as standard implementation of termination schemes. It has not been built and tested in the lab environment.

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