

# S3033

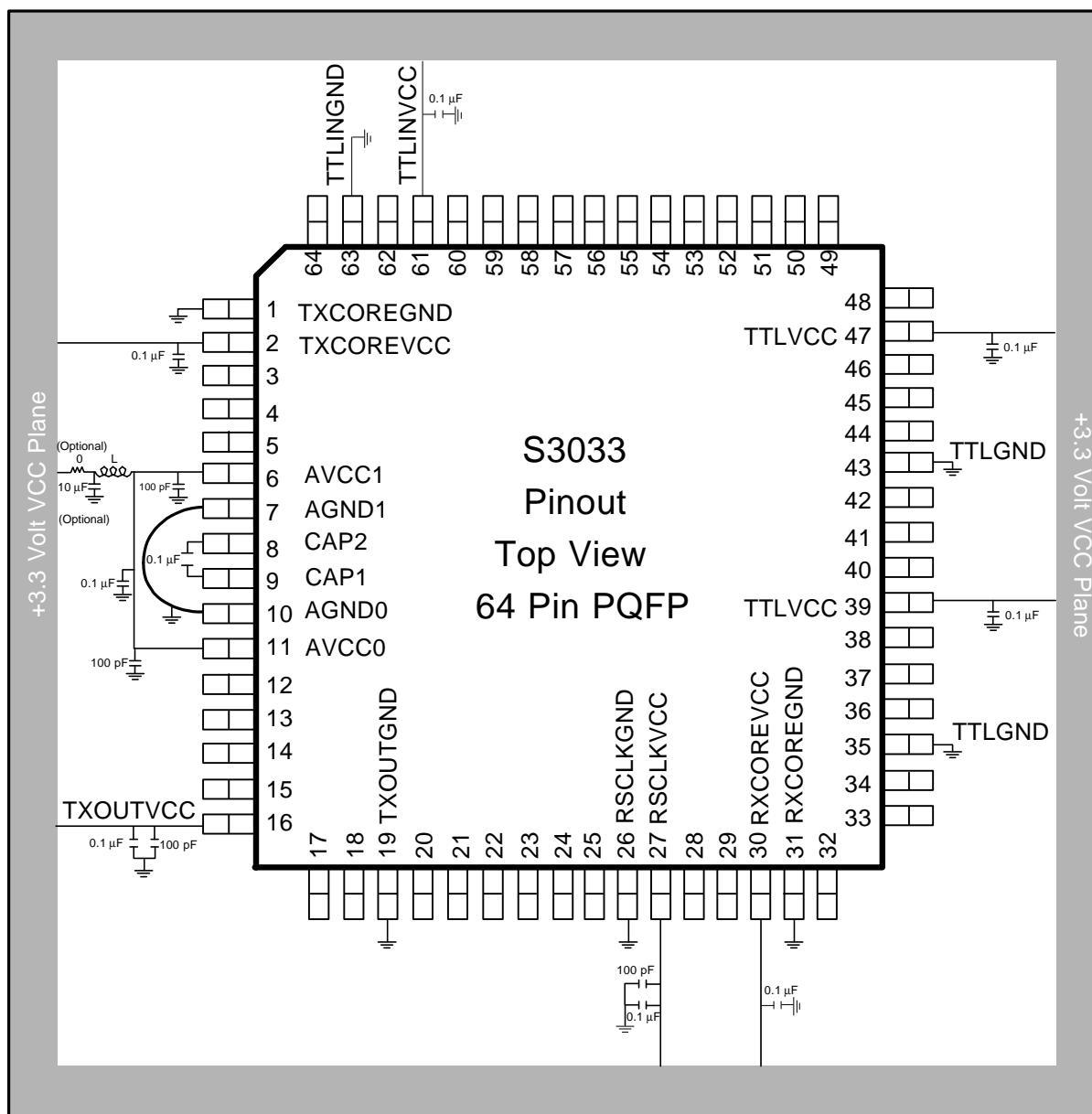
## APPLICATION NOTE

### Board Decoupling Guidelines

#### SONET/SDH/ATM OC-3/12 Transceiver S3033 Example

The S3033 transceiver chip is a fully integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) and OC-3 (155.52 Mbit/s) interface device. Figure 1 illustrates the connections for the S3033 device. External capacitors are required for power supply decoupling only. The inductor is a Murata BLM31B601SPB or BLM11B601SPB surface mount ferrite. The double capacitors shown are parallel 0.1  $\mu$ F X7R and 100 pF are COG or NPO ceramic chip. The CAP1/CAP2 capacitor should be 0.01  $\mu$ F X7R. Note that the 0.1  $\mu$ F should be placed on the bottom side of the board for better capacitor efficiency. The Low ESR 10  $\mu$ F capacitor and 0  $\Omega$  resistor are optional for AVCC, for higher noise environments.

Figure 1. S3033 Connections





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