S2074

DECOUPLING APPLICATION NOTE

SIX PORT BYPASS AND REPEATER FOR FC-AL

S2074 Decoupling Layout

The S2074 Six Port Bypass and Repeater contains a Clock and Data Recovery (CDR) PLL. The LPF1/LPF2 pins should be connected to a 2.2 µF (X7R Type) capacitor in series with 24 Ω resistors. Figure 1 illustrates the connections for the S2074. The ground ring is shown around the loop filter capacitor. The ring should be attached to pin 30 (GND) and brought to minimum metal spacing distance to pins 33 and 34. Please note that the ring should be directly connected to the ground plane as close as possible to pin 30 to avoid current through the ground ring. The values of the decoupling components are listed in Table 1.

Figure 1. Power and Ground Connections

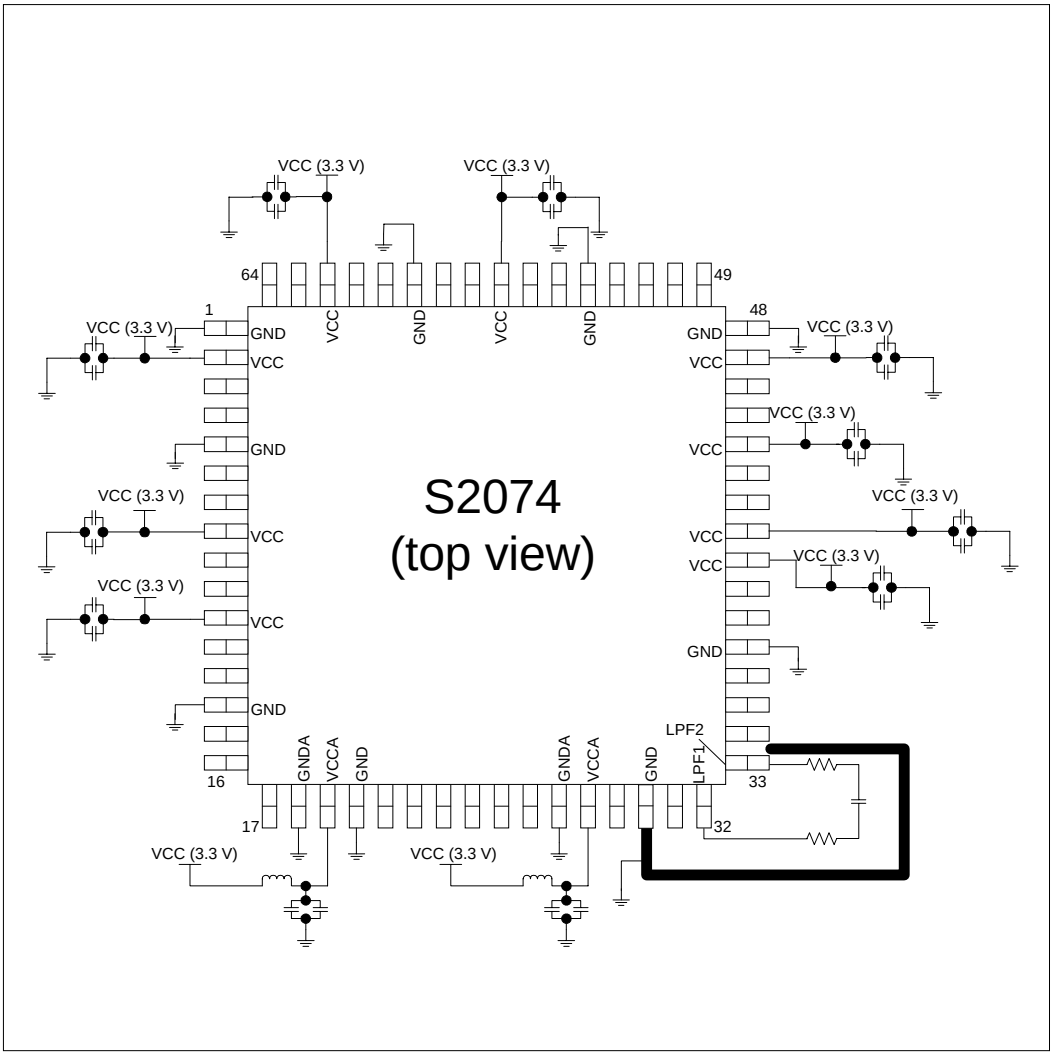

Table 1. Power and Ground Application Information

Function	Pinout Name	Instructions
ANALOG	VCCA	Connect to low noise or filtered 3.3 V supply through a ferrite bead (600 W at 100 MHz: Murrata BLM31B601S or equivalent). Provide dual local HF bypassing to AVEE (0.1 µF, 100 pF) for low inductance and resistance. A single low inductance 0.1 µF capacitor can be substituted for the pair (Vishay VJ0612 or equivalent, < 0.5 nH max inductance).
	GNDA	Connect to ground plane.
DIGITAL	VCC	Provide low impedance connection to 3.3 V. Provide dual local bypassing to GND plane (0.1 µF and 100 pF in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µF cap).
	GND	Connect to ground plane

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