S2067

APPLICATION NOTE

BYPASSING 8B/10B ENCODING and DECODING

PURPOSE

The purpose of this application note is to explain how to configure the S2067 to bypass the 8B/10B encoding/decoding blocks. Details on how the signals are renamed and the functional changes will also be explained.

Transmitter Description

The S2067 provides an option to bypass the 8B/10B encoding/decoding blocks by setting the LC_BYP pin. The LC_BYP signal is located at pin B1. The S2067 datasheet states that pin B1 is 'GND'. The bypass mode will be referred to as 10 bit mode. The 10 bit mode does not provide line coding/decoding; data passed into the device should be 8B/10B encoded by the upstream device. The transmitter block diagram is shown in Figure 1.

The input, LC_BYP, provides the option of either using the 8B/10B encoding/decoding scheme or bypassing it. This signal controls the line coding for both the transmit and receive paths on both channels. When LC_BYP is not asserted, the input consists of 8 bits of user data (DINx[0:7]) and two signalling bits (KGENx and SOFx). When LC_BYP is asserted, the input consists of 10 bits: DINx[0:7], and where KGENx and SOFx are redefined as DINx8 and DINx9. See Tables 1 and 2. A parallel input and a clock input (TCLKx) are provided for each channel of the S2067. The two 10 bit data channels are clocked into the S2067 FIFOs by the TCLKx signal provided with each parallel bus.

The data must be 8B/10B encoded prior to transmission to the S2067 to ensure that adequate transition density and DC balance are maintained. Data is transmitted DINx[0] first across the serial interface.

Table 1. Control Signal for 8B/10B Encoding/Decoding

LC_BYP (PIN B1)	Operation
0	8 bit mode. 8B/10B encoding/decoding is enabled.
1	10 bit mode. 8B/10B encoding/decoding is disabled. KGENx and SOFx are redefined as DINx8 and DINx9 on the transmitter side. On the receiver side, KFLAGx and ERRx are redefined as DOUTx8 and DOUTx9.

Table 2. Pin Naming Convention when 8B/10B is Enabled or Bypassed

Pin Number	Pin Name with B1 Deasserted (Low)	Pin Name with B1 Asserted (High)
G2	KFLAGA	DOUTA8
J2	ERRA	DOUTA9
R13	KGENA	DINA8
T15	SOFA	DINA9
R1	KFLAGB	DOUTB8
P4	ERRB	DOUTB9
L14	KGENB	DINB8
L15	SOFB	DINB9

Receiver Description

Each receiver channel is designed to implement a serial backplane receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 2.

When LC_BYP is asserted, the 8B/10B decoding block is disabled and the KFLAGx and ERRx outputs are redefined to be DOUTx8 and DOUTx9, respectively. See Tables 1 and 2. The EOFx output reports occurrences of the K28.5 character.

Figure 1. Transmitter Block Diagram

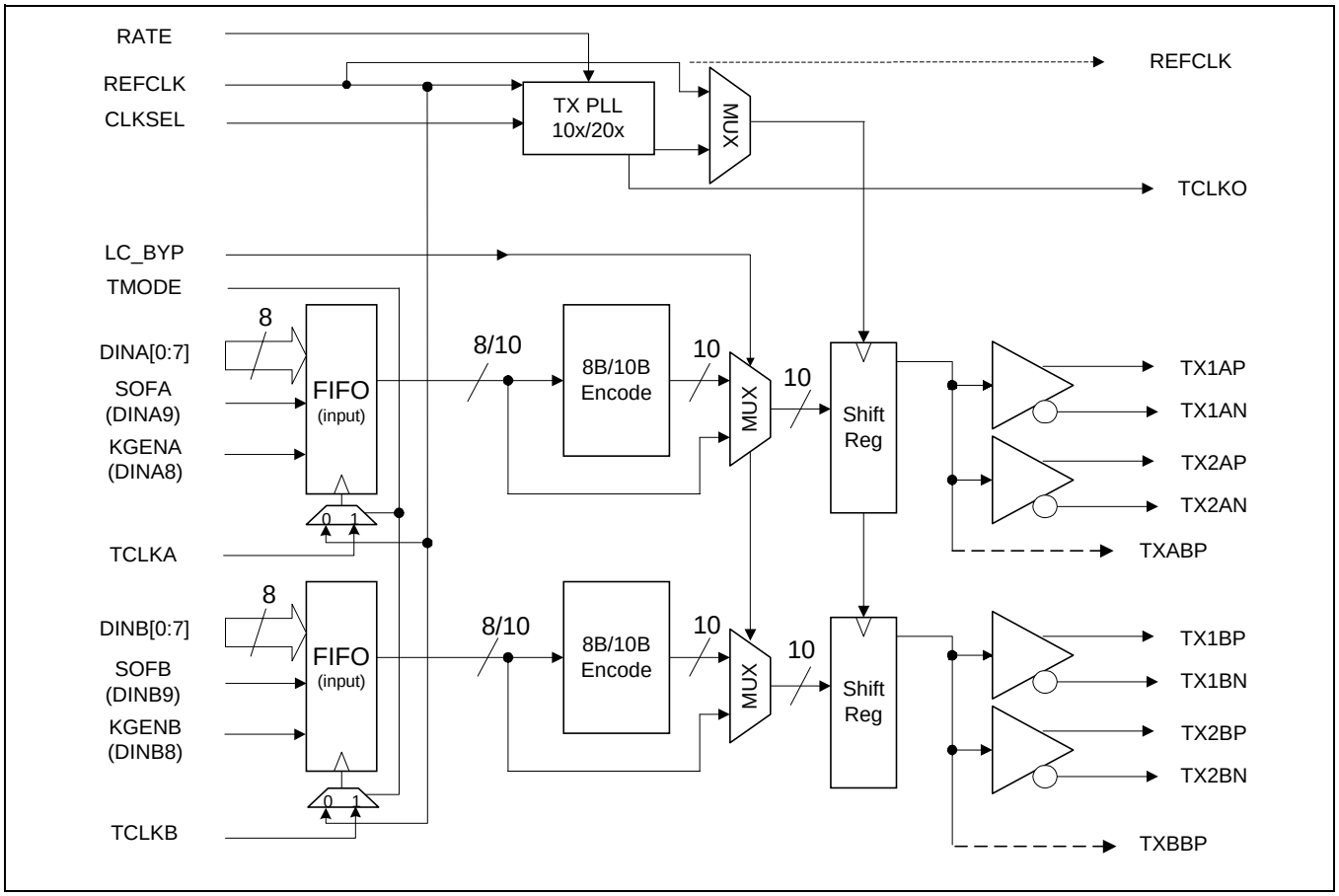

Figure 2. Receiver Block Diagram

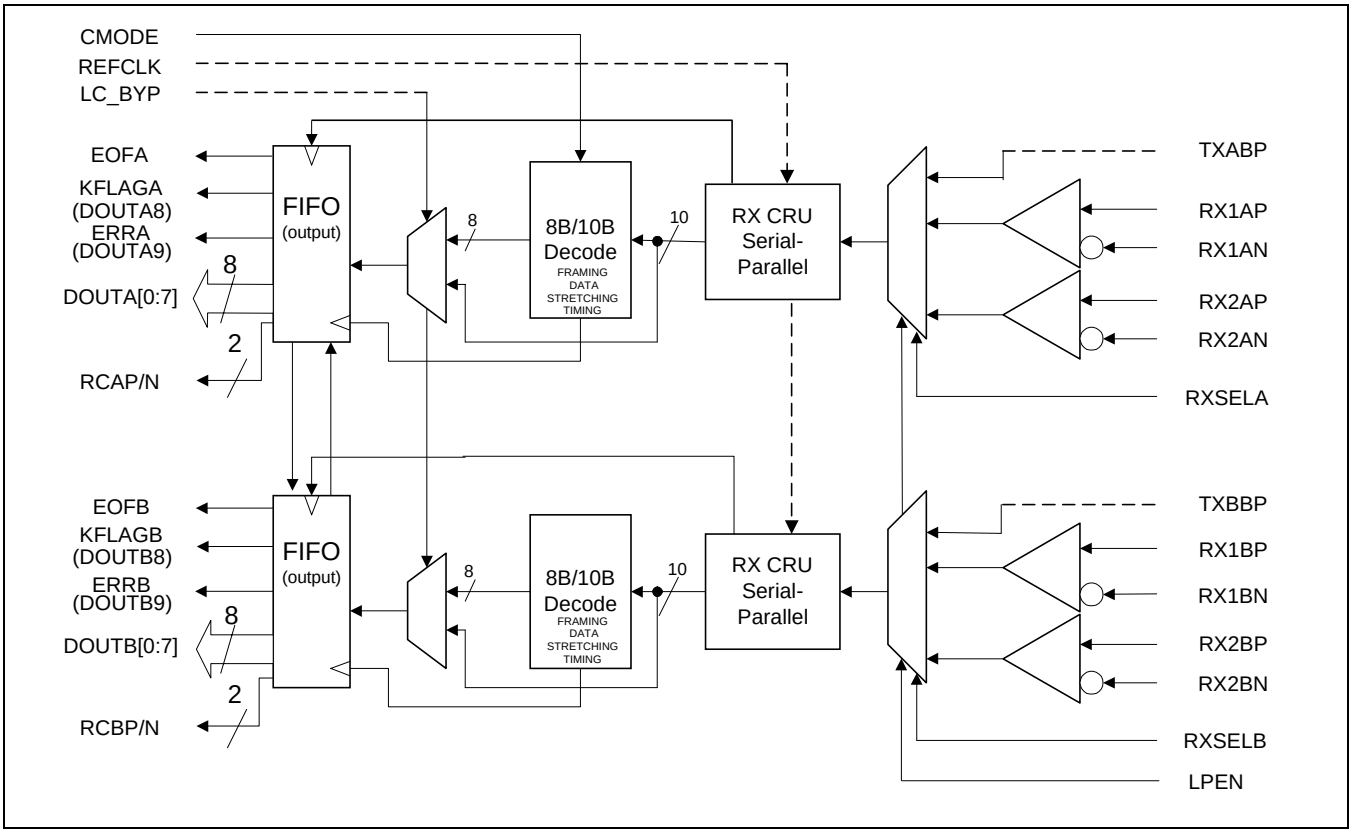

Figure 3. S2067 Pinout (Bottom View, only showing signal changes when 8B/10B is disabled)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
1		LC_BYP													KFLAGB (DOUTB8)	
2							KFLAGA (DOUTA8)		ERRA (DOUTA9)							
3																
4														ERRB (DOUTB9)		
5																
6																
7																
8																
9																
10																
11																
12																
13															KGENA (DINA8)	
14											KGENB (DINB8)					
15											SOFB (DINB9)					SOFA (DINA9)
16																

Figure 4. S2067 Pinout (Top View, only showing signal changes when 8B/10B is disabled)

	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1		KFLAGB (DOUTB8)													LC_BYP	
2								ERRA (DOUTA9)		KFLAGA (DOUTA8)						
3																
4			ERRB (DOUTB9)													
5																
6																
7																
8																
9																
10																
11																
12																
13		KGENA (DINA8)														
14						KGENB (DINB8)										
15	SOFA (DINA9)					SOFB (DINB9)										
16																

S2067 Device Specification Modifications

The timing and voltage levels specified from Figures 12 through 23 and Tables 16 through 26 in the S2067 device specification are correct regardless of the state of LC_BYP (Pin B1). In Figures 12 and 13, KGENx and SOFx are renamed DINx8 and DINx9 respectively when bypassing the 8B/10B blocks. In Figures 14 and 15, KFLAGx and ERRx are renamed DOUTx8 and DOUTx9 respectively. The loop filter resistor and capacitor values are not affected by the state of pin B1.

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