S2065

APPLICATION NOTE

Application Note and Reference Diagrams

Introduction

This document is intended to assist customers in using AMCC's S2065 quad channel physical layer device. Details concerning application information, circuit design, layout, and component selection are provided to help insure first-pass success in implementing a functional design with optimal signal quality. This document should be used in conjunction with the S2065 product device specification. An elementary knowledge of high-speed printed circuit layout techniques is assumed. Contact your local AMCC Field Applications Engineer or Regional Sales Manager to discuss any questions or concerns you may have.

Serial Input / Output Connections

Figure 1 shows the basic coupling termination scheme for the S2065 high-speed serial inputs. The serial inputs are internally DC biased at VCC - 1.3 V. Recommended external connections include 0.01 μF AC coupling capacitors and a line-to-line termination resistor. The termination resistor is required for line lengths greater than 1 cm, which exhibit transmission line effects at gigabit speeds. The termination must match the characteristic impedance of the differential lines to minimize signal reflections. The 100 Ω value shown assumes characteristic line impedance of 50 Ω (if the lines are 75 Ω, the line-to-line termination resistor should be 150 Ω). The AC coupling capacitors allow the DC bias point to be set internally by the input stage. The DC bias can be set externally by implementing a resistor divider network on each line, but this is not recommended since it increases the part count and does not provide performance improvement.

Figure 2 shows the connection diagram for high-speed serial outputs. The outputs of the S2065 have internal pull-down resistors integrated into the output macro and do not require external pull-down resistors

Figure 3 shows an input offset voltage biasing configuration, which should be implemented in the event that the input is unused and may be subjected to noise. The 220 kΩ pull-down resistor offsets the input by approximately 60 mV, insuring that noise signals with amplitude less than 60 mV will not cause the input to chatter.

At a signal rate of 1.25 Gbps the output stage can drive more than 25 m of Twinax cable directly.

Figure 1. High Speed Differential

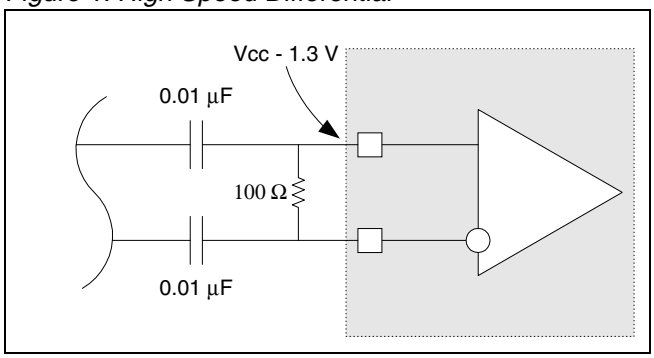


Figure 2. Serial Output Load

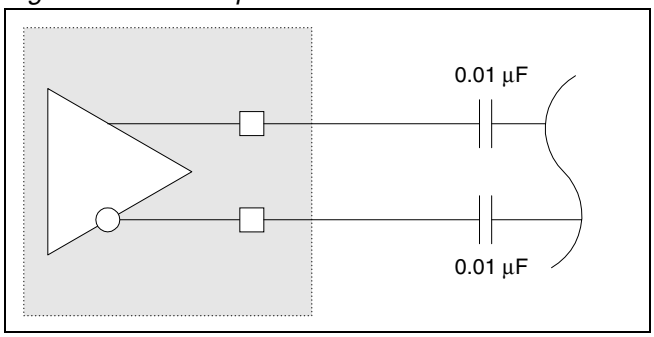
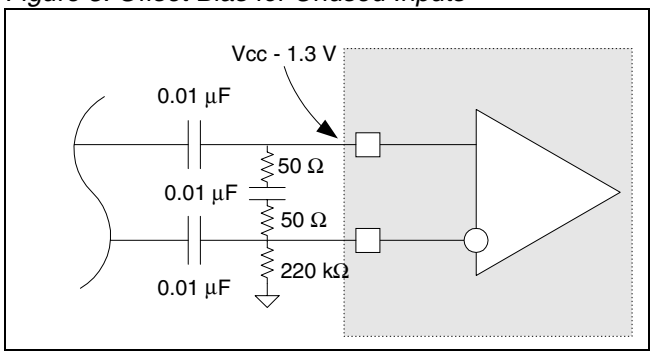


Figure 3. Offset Bias for Unused Inputs



Power and Ground Connections

Recommended connection diagram is shown below in Figure 4 and 5. Figure 4 shows the bottom view. Figure 5 shows the inner signal layer looking in from the bottom view. Table 1 provides power and ground connection recommendations.

Figure 4. Recommended Connection Diagram

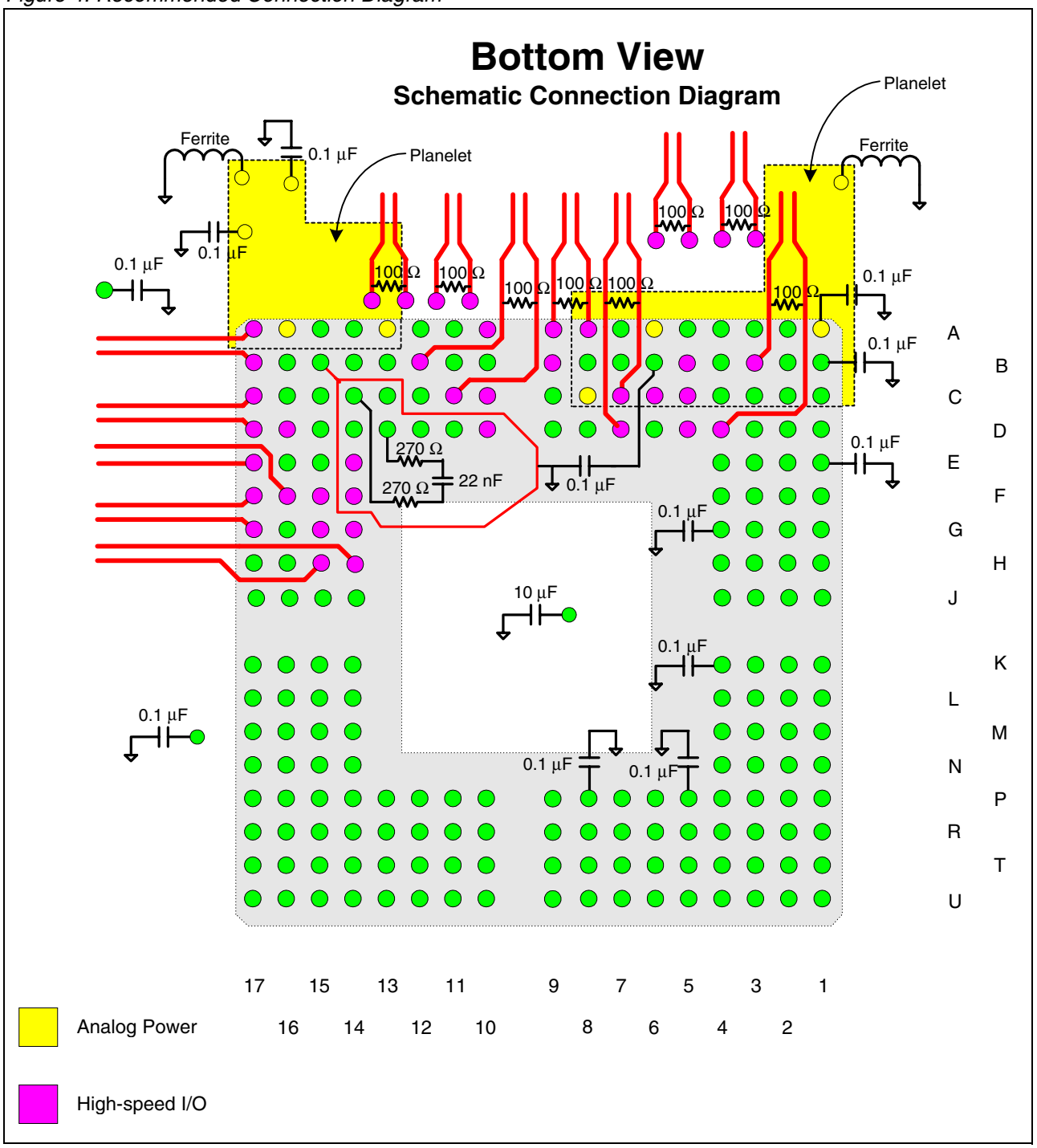


Figure 5. Recommended Connection Diagram

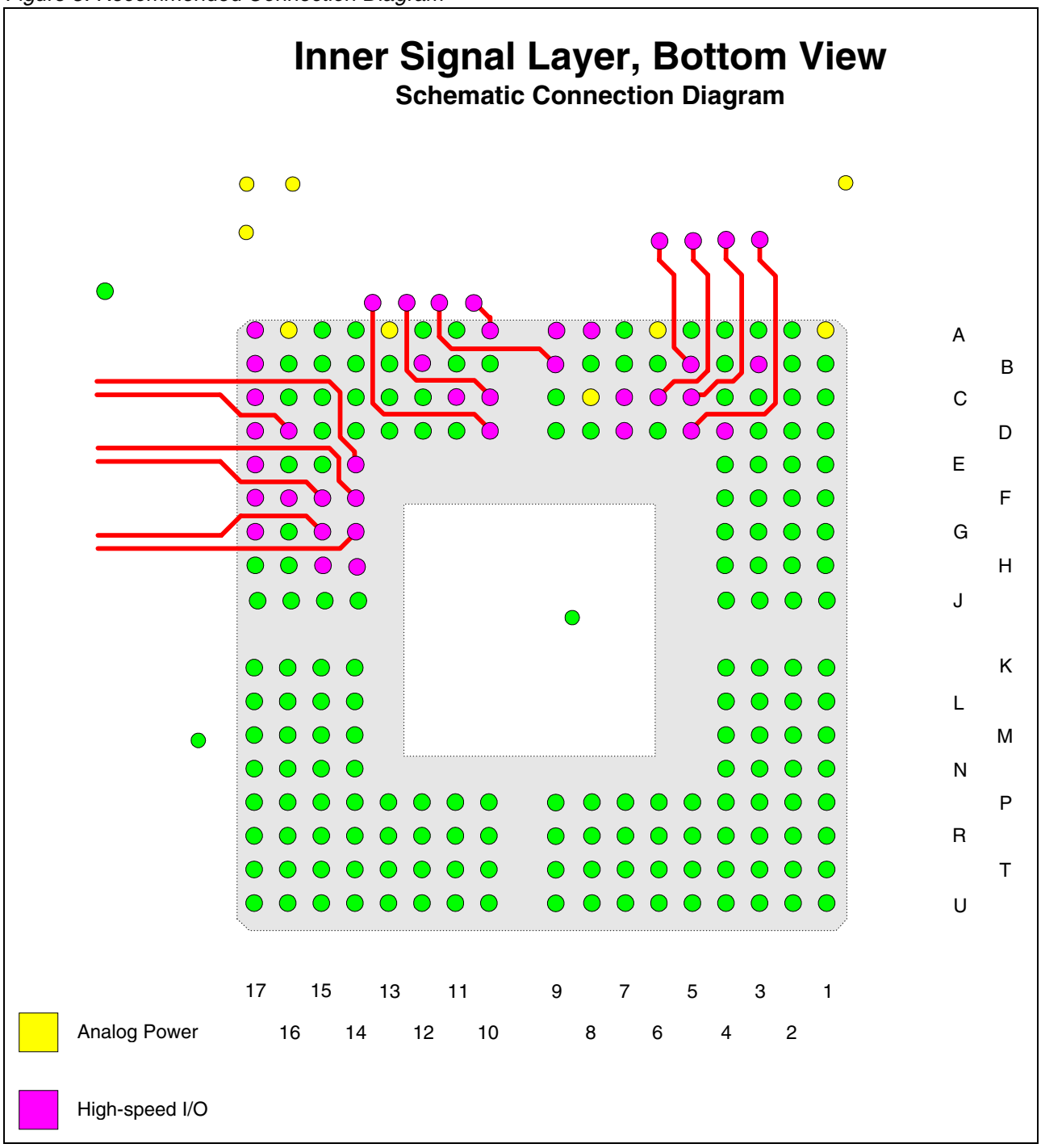


Table 1. Power and Ground Application Information

Function	Pinout Names	Instructions
ANALOG	AVCC	Connect to low noise or filtered 3.3 V supply through a ferrite bead (600 Ω at 100 MHz: Murrata BLM31B601S or equivalent). Provide dual local HF bypassing to AVEE (0.1 μF, 100 pF) for low inductance and resistance. A single low inductance 0.1 μF capacitor can be substituted for the pair (Vishay VJ0612 or equivalent, less than 0.5 nH max inductance).
	AVEE	Connect to ground plane.
LVPECL I/O	ECLIOVCC	Provide low impedance connection (via) to 3.3 V. Provide dual local bypassing to GND plane (0.1 μF and 100 pF in parallel) or a single low inductance Vishay VJ0612 or equivalent 0.1 μF cap.
	ECLIOVEE	Connect to ground plane.
CORE	ECLVCC	Provide low impedance connection (via) to 3.3 V. Provide dual local bypassing to GND plane (0.1 μF and 100 pF in parallel) or a single low inductance Vishay VJ0612 or equivalent 0.1 μF cap.
	ECLVEE	Connect to ground plane.
TTL I/O	TTLVCC	Provide low impedance connection (via) to 3.3 V. Provide dual local bypassing to GND plane (0.1 μF and 100 pF in parallel) or a single low inductance Vishay VJ0612 or equivalent 0.1 μF cap.
	TTLVEE	Connect to ground plane.

Layout Recommendations

Figures 6, 7 and 8 show a sample layout from top and bottom view.

Figure 6 is a top view, showing each ball landing pad with an associated via. The vias are offset from the balls and exploded outward with respect to the center of the part. Offsetting the vias from the ball pad insures that solder from the ball is not wicked down into the via during the soldering process. The vias are exploded outward in order to maximize the current paths through the via field into the area under the center of the chip.

Figure 7 shows the view from the bottom of the board with the chip outline superimposed. This provides an illustration of the wide corridors through the vias that allow current to flow into the area under the center of the chip (one corridor on the center of each side). This sample layout shows all decoupling, loop filter, and high-speed I/O components on the back side of the board. Figure 8 shows an inner layer from the bottom view of the chip.

Figure 6. S2065 Sample Layout, top view

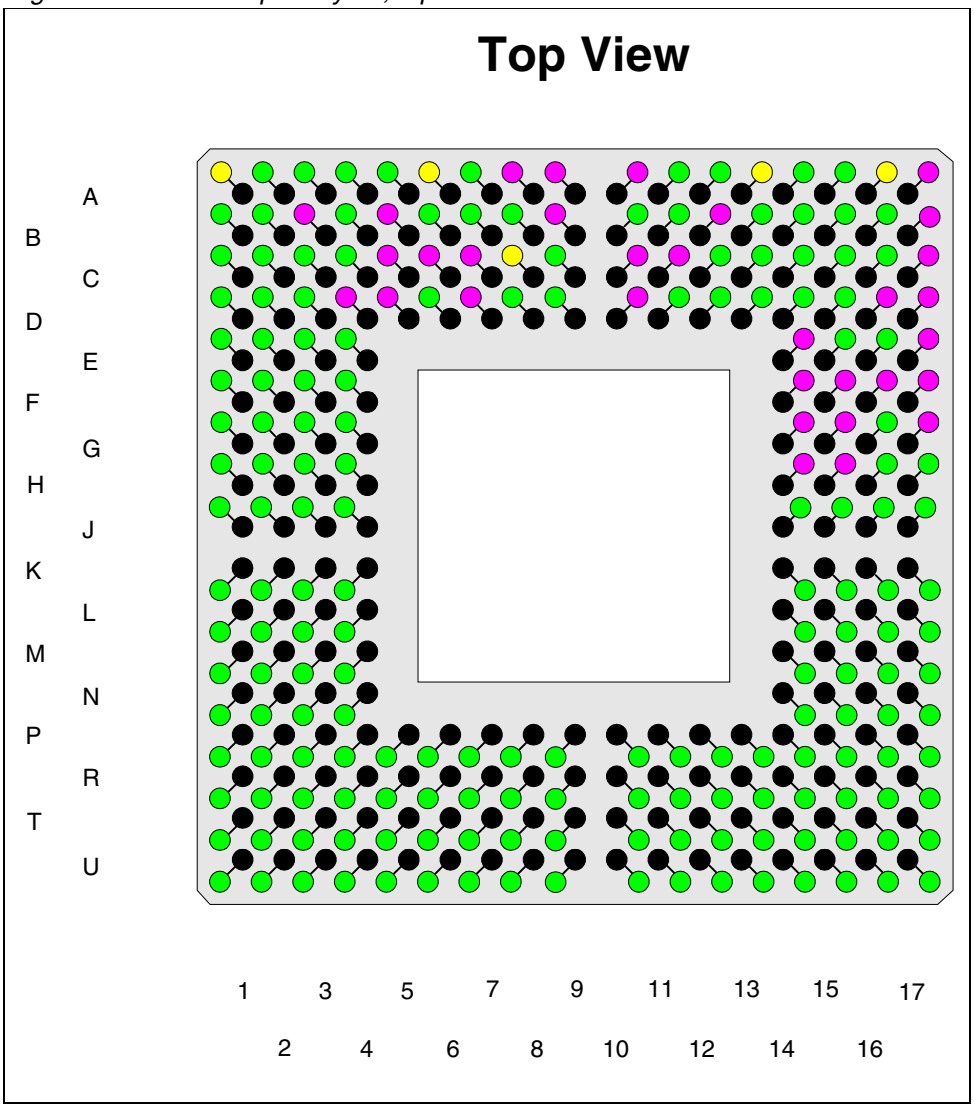


Figure 7. S2065 Sample Layout, bottom view

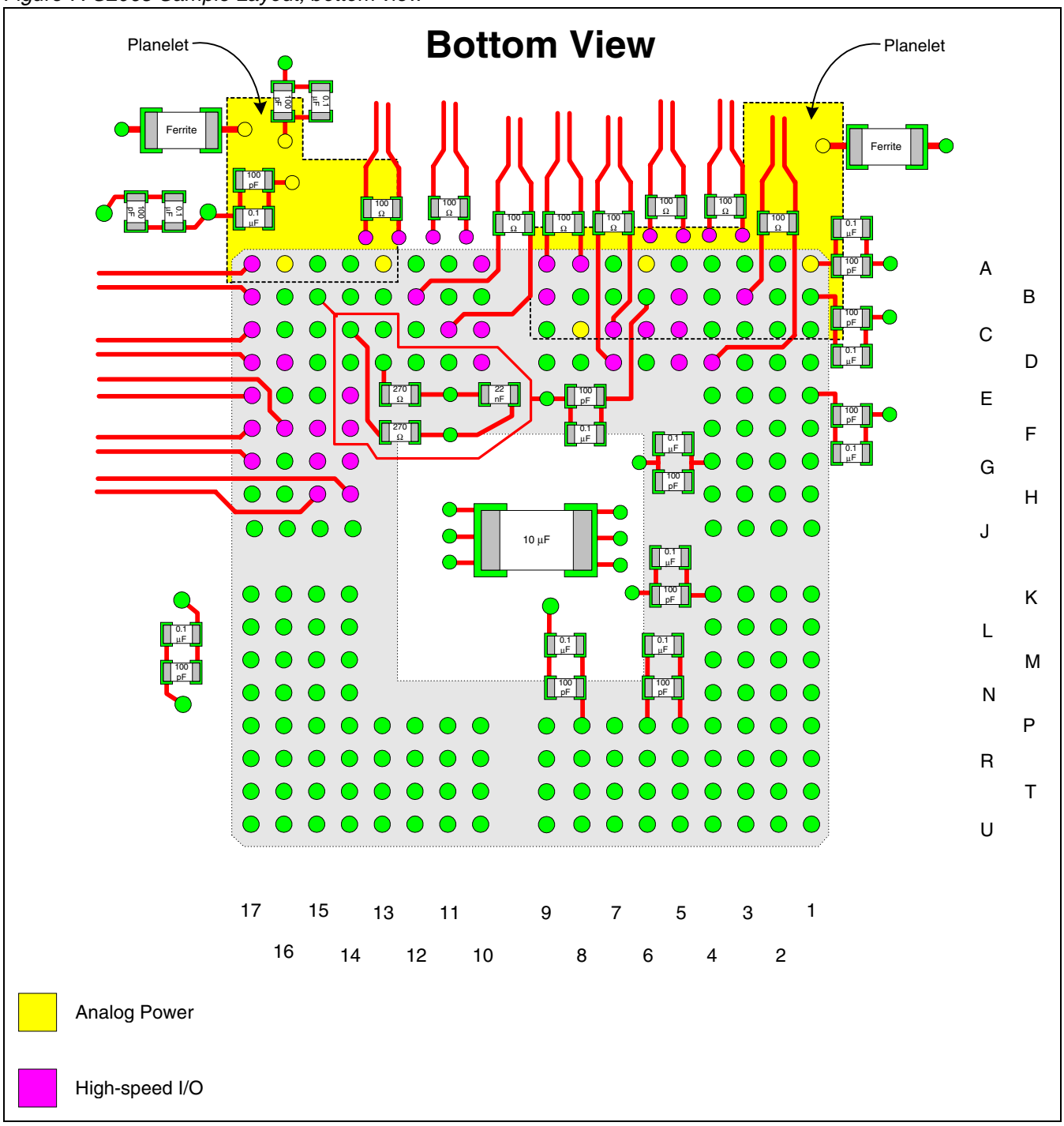
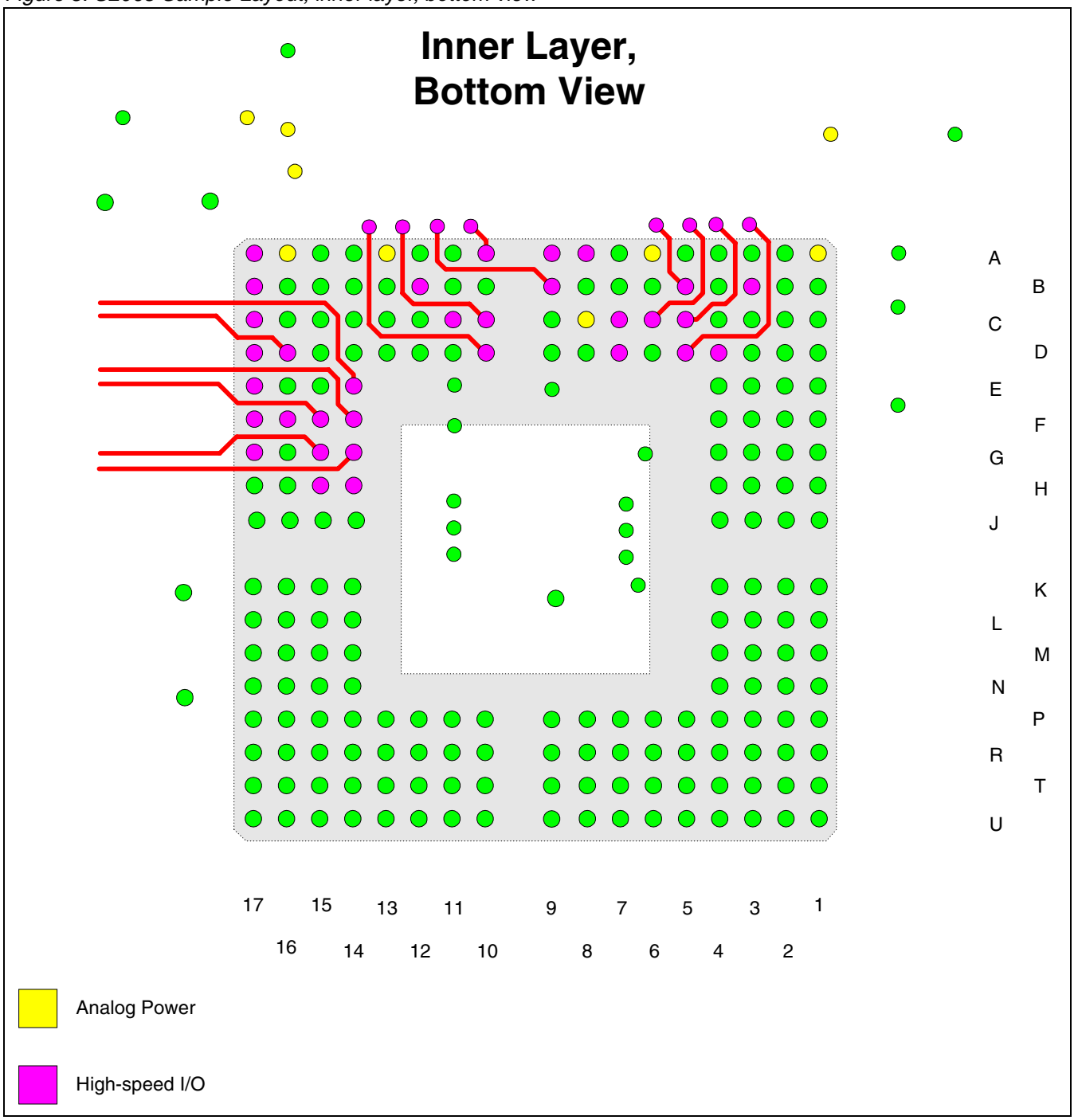


Figure 8. S2065 Sample Layout, inner layer, bottom view



When laying out a high-speed part, high-speed I/O should be considered first. The differential receive pairs are shown with 100 Ω line-to-line termination resistors. The resistors should be placed as close to the receive inputs as possible while adhering to layout rules. If pull-down resistors are included on the differential transmit pairs, they should be placed as close as possible to the transmit outputs while adhering to layout rules. AC coupling capacitors are not shown in this layout. They are typically included in the high-speed signal path in order to insure that the DC bias of the high-speed outputs does not affect the inputs. There is no requirement to place the coupling capacitors close to either the transmitting or receiving part. If a signal is routed through a connector, the AC coupling capacitors are often laid out close to the connector. If AC coupling capacitors are employed, they may be included with the outputs, the inputs, or both places[1]. When two parts from the AMCC SiliconHiway™ family are connected, coupling capacitors are not required to reconcile DC levels. However, there are several design considerations that may make it desirable to include them. In applications where a board may be hot swapped, it is likely that the high speed I/O will be excited before the chip has been powered up. Adding coupling capacitors insures that the signal on any input (or output) will not be more than approximately one volt.

At gigabit rates, the high-speed traces exhibit transmission line effects. It is important to keep the trace lengths of differential pairs the same length in order to minimize skew, and to use either chamfered or rounded corners in order to reduce ElectroMagnetic Interference (EMI) and impedance mismatches. In Figure 7, the high-speed lines are microstrip traces (placed on the surface of the board above a power or ground plane). The traces in Figure 8 are stripline traces (sandwiched between power/ground planes on an internal signal plane). Stripline traces have the advantage of better EMI shielding, but the vias cause small impedance mismatches that will result in small reflections in the signal lines.

After considering the high-speed I/O traces, the reference clock input, loop filter, and analog power decoupling are the next most important layout features. Each of these is critical because they could potentially offer a path for noise into the analog portion of the chip, which translates into jitter. The clock line should be kept as short as possible, and care should be taken to minimize the potential for crosstalk or noise coupling onto the clock line. The loop filter is shown in Figure 7; two 270 Ω resistors are connected to the external loop filter pins, with an AC coupling capacitor (22 nF) between them. The entire loop filter is surrounded by a ground ring to increase noise immunity. The analog power pins are connected to power planelets, which can be created on one of the signal planes. If power planelets are employed, insure that the planes above and below are solid power/ground planes in order to avoid ground loops and antenna effects in return current paths. The planelet is isolated from the power plane by inductors and capacitors. Ferrites may be employed (see Table 1). In addition, decoupling capacitors are added close to each analog power pin.

Finally, decoupling capacitors are added around the chip as space allows. Due to the ball density of BGA packages, it is not reasonable to attempt to decouple every power pin. Where space permits, power pins are directly decoupled. In addition, capacitors are sprinkled around the chip, the most notable of which is the 10 μF capacitor in the center of the chip. We use multiple vias to both the power and ground planes to reduce the impedance between the capacitor pads and the respective planes.

1. Applications where hot swapping of boards is required often employ AC coupling capacitors at both the input and the output to insure that DC levels do not harm the chip prior to power on.

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