17 X 17 CROSSPOINT SWITCH APPLICATION NOTE S2018

APPLICATIONS

- Internet switches
- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

PURPOSE

The purpose of this application note is to describe the basic operation of the S2018, a 17 x 17 3.2 Gbps Differential Crosspoint Switch. All information needed to successfully operate the S2018 are in this application note. Included in this note is the configuration procedure that explains how to program the S2018 for new configurations. It also includes a description of how to correctly set the programmable output swing. Furthermore, information on connectivity and thermal management are included to ensure proper use of the device.

In addition to the operation of the S2018, this application note also explains how the S2018 and the S2092 can be used together as illustrated in Figure 1. A basic description of the S2092 is given along with information pertaining to the S2092 pinout, thermal management and connectivity. More importantly, this note shows how the S2018 and the S2092 are connected together when combined.

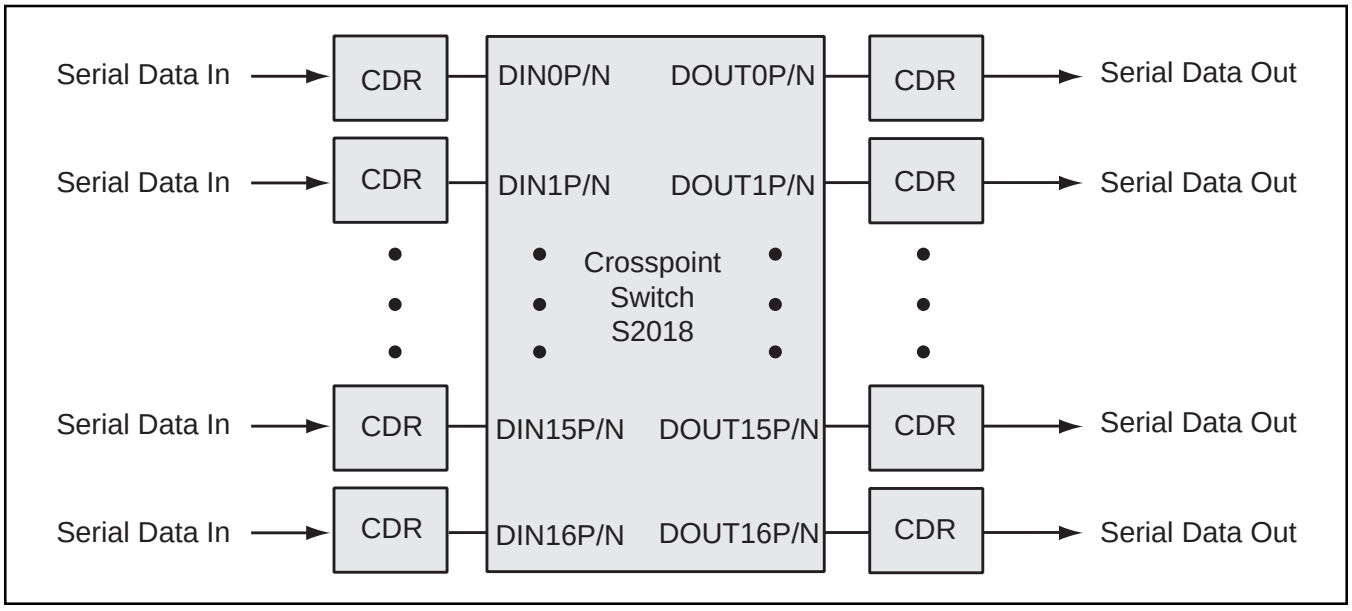
S2018 GENERAL DESCRIPTION

The S2018 is a very high-speed 17 x 17 differential crosspoint switch with full broadcast capability. Any of its 17 differential LVPECL input signal pairs can be connected to any or all of its 17 differential CML output signal pairs.

The differential 10K LVPECL logic data path makes the part ideal for high-speed applications. The differential nature of the data path is retained throughout the crosspoint structure, to minimize data distortion and to handle NRZ data rates up to 3.2 gigabits per second. The high speed serial inputs to the S2018 are internally biased to Vcc -0.84V and have internal 100 Ω line-to-line termination.

LVTTL configuration controls simplify interfacing to slower speed circuitry. Once a new configuration has been entered into the configuration register file, the S2018 can be completely reconfigured by pulsing the CONFIGN input.

Figure 1. System Block Diagram



S2018 Crosspoint Operation

The following describes the basic configuration operation of the S2018.

1. CSN is set active by setting it Low.
2. OADDR[4:0] (output address) is configured. (See Table 1.)
3. IADDR[4:0] (input address) is configured. (See Table 1.)
4. LOADN is strobed. This loads IADDR[4:0] into the Configuration Register File (CRF) location selected by OADDR[4:0]. (See Figure 8.)
5. The above steps are repeated until configuration loading is complete.
6. Finally CONFIGN is strobed and the incoming differential data (DIN) is routed according to the control data (IADDR and OADDR).

Output Swing Adjust

The S2018 output swing can be adjusted by connecting one or more of the VADJUST_X pins to the VCSHIGH pin according to Table 2. Note that as the output swing is increased, the power dissipated by the part is proportionally increased. The output swing range is from 240 mVpp differential up to 1300 mVpp differential per Table 2.

S2018 Crosspoint Configuration Time

Configuration time is the time interval from when the first address to be configured is input, to the time where the reconfiguration is complete (i.e. after the CONFIGN strobe occurs and the switch is newly configured). The configuration timing diagram is shown in Figure 2. Table 3 shows the respective timing values.

Table 1. Input/Output Addresses of S2018

DIFF INPUT	IADDR4	IADDR3	IADDR2	IADDR1	IADDR0	**DIFF OUTPUT**	OADDR4	OADDR3	OADDR2	OADDR1	OADDR0
DIN0	0	0	0	0	0	**DOUT0**	0	0	0	0	0
DIN1	0	0	0	0	1	**DOUT1**	0	0	0	0	1
DIN2	0	0	0	1	0	**DOUT2**	0	0	0	1	0
DIN3	0	0	0	1	1	**DOUT3**	0	0	0	1	1
DIN4	0	0	1	0	0	**DOUT4**	0	0	1	0	0
DIN5	0	0	1	0	1	**DOUT5**	0	0	1	0	1
DIN6	0	0	1	1	0	**DOUT6**	0	0	1	1	0
DIN7	0	0	1	1	1	**DOUT7**	0	0	1	1	1
DIN8	0	1	0	0	0	**DOUT8**	0	1	0	0	0
DIN9	0	1	0	0	1	**DOUT9**	0	1	0	0	1
DIN10	0	1	0	1	0	**DOUT10**	0	1	0	1	0
DIN11	0	1	0	1	1	**DOUT11**	0	1	0	1	1
DIN12	0	1	1	0	0	**DOUT12**	0	1	1	0	0
DIN13	0	1	1	0	1	**DOUT13**	0	1	1	0	1
DIN14	0	1	1	1	0	**DOUT14**	0	1	1	1	0
DIN15	0	1	1	1	1	**DOUT15**	0	1	1	1	1
DIN16	1	X	X	X	X	**DOUT16**	1	X	X	X	X

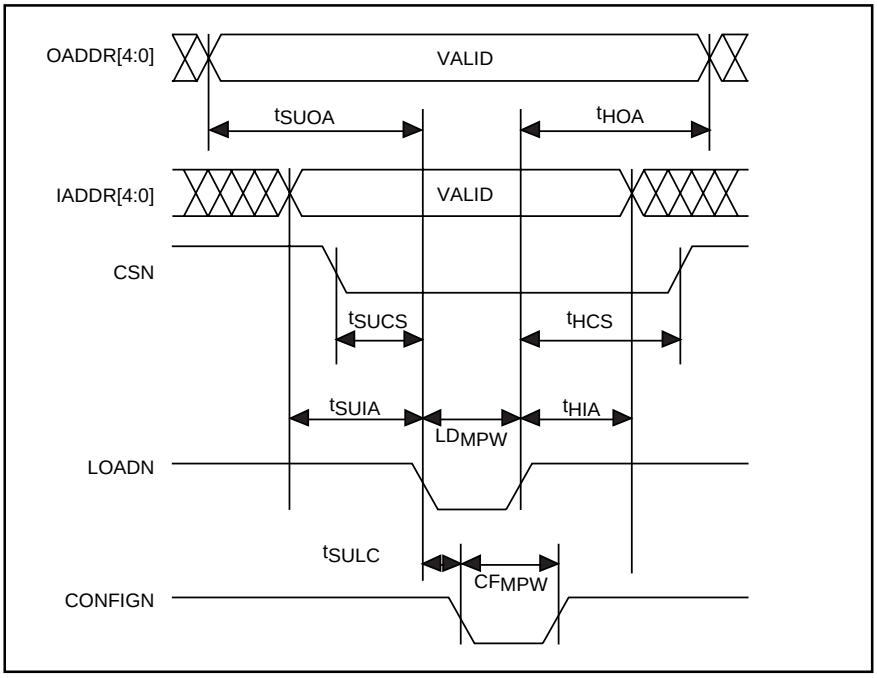
Note: X denotes don't care.

Table 2. Output Swing Adjust Pin Settings

Vadjust_1	**Vadjust_2**	**Vadjust_3**	**DOUTxx (mVpp Diff.)**
T	O	O	240
O	T	O	440
T	T	O	600
O	O	T	780
T	O	T	940
O	T	T	1100
T	T	T	1260

Note: T = Tie pin(s) VADJUST_X to pin VCSHIGH
O = Open

Figure 2. Reconfiguration Waveforms



Note: CONFIGN is strobed after the last corresponding input/output address pair to be configured or reconfigured has been loaded.

Figure 3. Data Transfer Waveforms

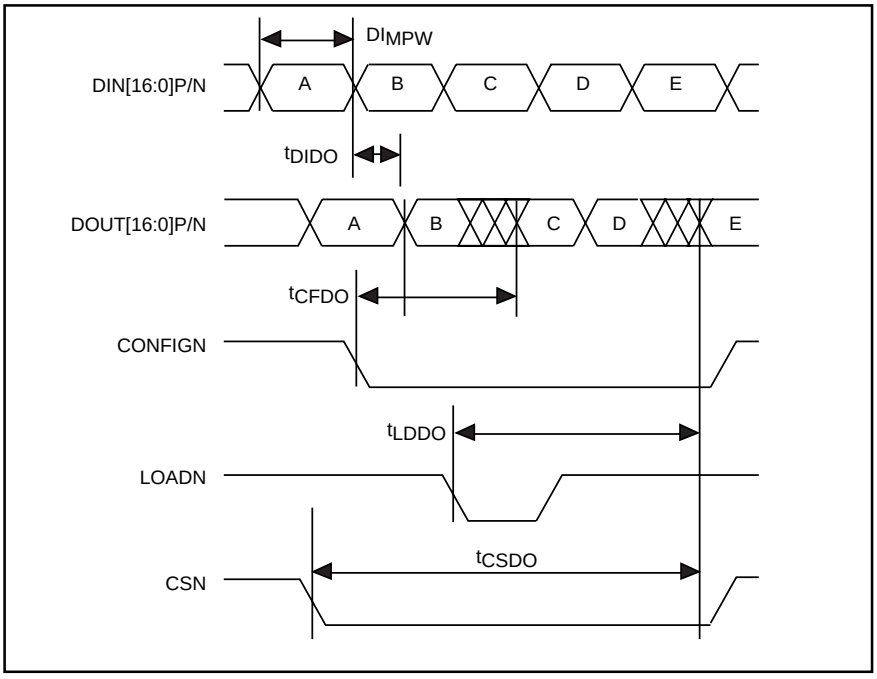


Table 3. Reconfiguration Timing Values for the S2018

Symbol	Description	Min	Max	Units
t_{CFDO}	Propagation Delay from falling edge of CONFIGN to DOUT[15:0]P/N valid.		3	ns
t_{SUOA}	Setup time of OADDR[4:0] before falling edge of LOADN.	0		ns
t_{HIA}	Hold time of IADDR[4:0] after rising edge of LOADN.	2		ns
LD_{MPW}	Pulse width low of LOADN.	2		ns
CF_{MPW}	Pulse width low of CONFIGN.	2		ns
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration.	2		ns

Equation 1. The Configuration Time for the S2018.

Configuration Time Equation =

$$(n-1)\ (t_{SUOA} + LD_{MPW} + t_{HIA}) + (t_{SUOA} + t_{SULC} + t_{CFDO})$$

The variable "n" is the number of outputs to be reconfigured. The first term in the equation is the time required to load (n-1) addresses. The second term in the equation is the time required for the last address to be loaded and CONFIGN strobed.

Substituting the timing values from Table 3, into Equation 1, the configuration time is then calculated, as shown in Equation 2.

Equation 2. Minimum Configuration Time

Minimum Configuration Time = n(4ns) + 1ns

Where "n" is the number of outputs being reconfigured.

In the following example, the S2018 crosspoint switch will be configured as shown in Figure 4.

Figure 4. Crosspoint Sample Configuration

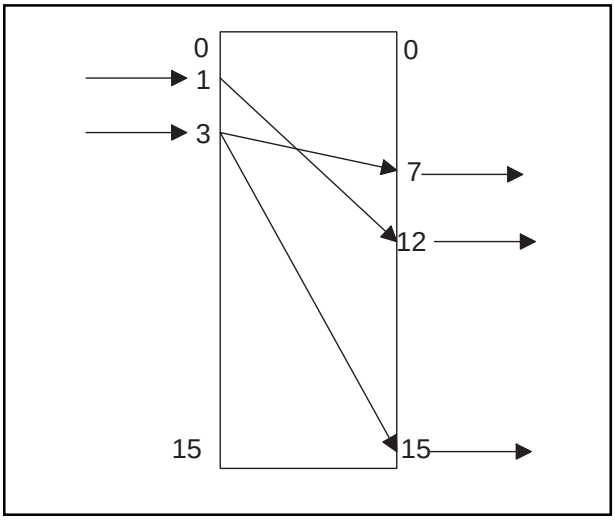


Table 4 shows the signals and a corresponding description of what will be used in this example.

Table 4. S2018 Configuration Signals

Signal	Description
OADDR	Serial data input to the Output Shift Register; defines output address.
IADDR	Serial data input to the Input Shift Register; defines input address.
LOADN	Load strobe is active low. On the falling edge of LOADN, the 5 bit output address (OADDR[4:0]) gets transferred in parallel to be decoded and the associated 5 bit input address (IADDR[4:0]) gets loaded into the configuration register file (CRF) location determined by OADDR[4:0].
CONFIGN	Configuration strobe is active low. When strobed low, loads the contents of the configuration register file to reconfigure the crosspoint.

The following procedure is a step-by-step description of the events that occur when setting up the S2018 to the configuration shown in Figure 4.

1. To connect an output pair to a given input pair, an output is selected using bits OADDR [4:0]. The 5 bits are transferred (on falling edge of LOADN) in parallel to Decode. At Decode, the 5 bits are interpreted as one of 17 output addresses. The corresponding Configuration Register File (CRF) is then opened to accommodate the input address. If for example, the 5 bits that are passed in are 01100, the 12^{th} output address will select the 12^{th} (out of 17) register file in the CRF as shown in Figure 6.
2. The IADDR[4:0] (input address) is loaded in parallel into the CRF on the falling edge of LOADN. The IADDR[4:0] address is placed into the CRF location that is specified by OADDR[4:0] as shown in Figure 8.
3. Steps 1-2 are repeated until 1 or all outputs are specified. The CRF end result for our example is shown in Figure 9.
4. Once all addresses have been loaded in the Configuration Register File, CONFIGN is strobed (active low), and the data in the 17 registers, (each 5 bits long, 85 bits) are sent in parallel to the Active Configuration Latch.
5. The Active Configuration Latch takes the 85 data bits and sends them to the crosspoint. The crosspoint is then set up accordingly (see step 3). The final result is that as shown in Figure 4.

The configuration time for the 3 address configuration shown in Figure 4 is 3(4ns) + 1ns = 13ns.

Figure 5. Output Address

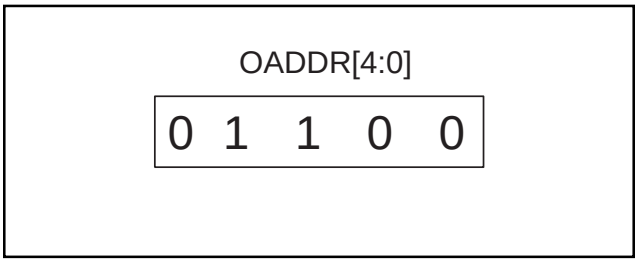


Figure 6. CRF Register Select

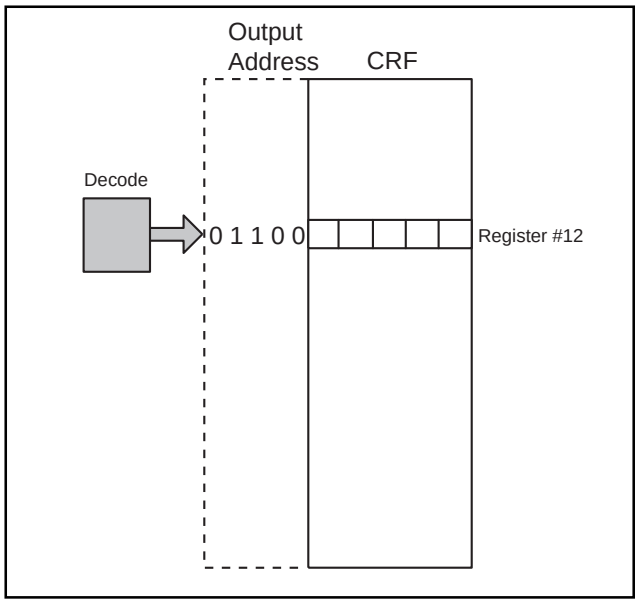


Figure 7. 5 Bit Input Address

Input and Output Address Codes

The 5-bit input address (IADDR[4:0]) and 5-bit output address (OADDR[4:0]) each allow 32 possible address codes. Only the first 17 input address codes and first 17 output address codes are used to reference 17 input ports and 17 output ports, respectively. Both input and output address normally use codes 0 to 16 (see Table 1). However, the S2018 was designed such that any input address codes greater than 16 will select input port 16. Similarly, any output address codes greater than 16 will select output port 16.

Figure 8. Loading CRF

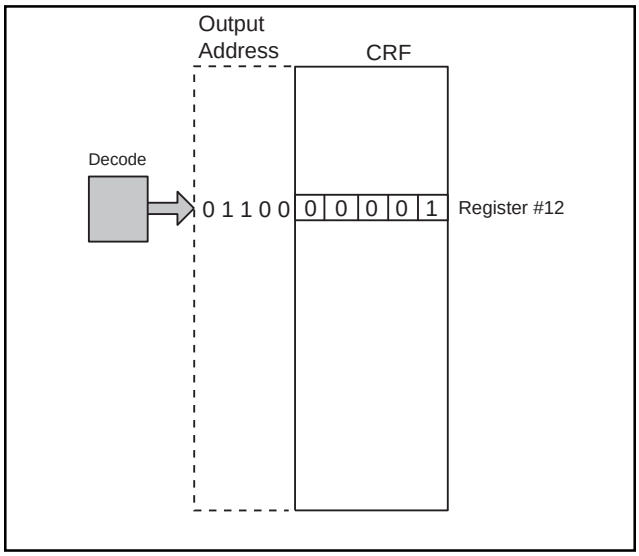
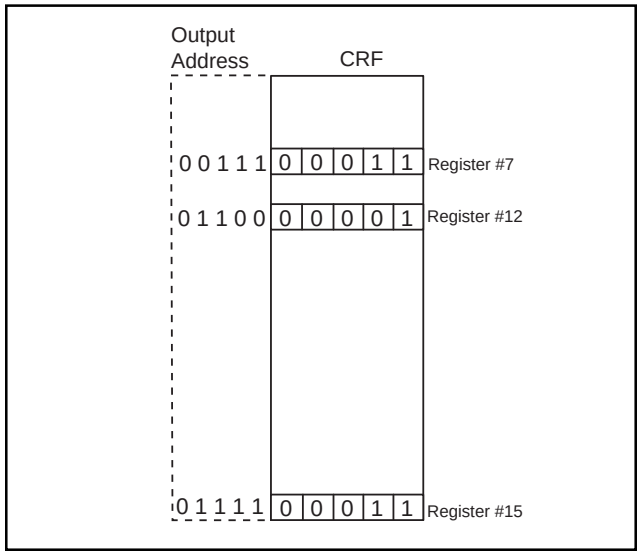


Figure 9. Complete CRF



Serial Input/Output Connections

Figure 10 shows the recommended coupling termination scheme for the S2018 high speed serial inputs. The S2018 serial inputs are internally DC biased to Vcc -0.84 V. External connections include 0.01 µF AC coupling capacitors on each line. The AC coupling capacitors allow the DC bias point to be set internally by the input stage. An external line-to-line resistor termination is not required as each S2018 serial input has an internal line-to-line termination resistor.

A termination resistor is required for lines longer than ~1 cm, which exhibit transmission line effects at these high speeds. This resistor matches the characteristic impedance of the differential lines and minimizes signal reflections. The resistor values shown in Figures 10 and 11 assumes characteristic line impedance of 50 Ω. If the line impedance is 75 Ω, the line-to-line termination resistor should be 150 Ω. However, there can only be 50 Ω. line impedance at the inputs as the internal line-to-line termination resistors are fixed at 100 Ω.

Figure 11 shows the connection diagram for high-speed serial outputs. External connections include 0.01 µF AC coupling capacitors on each line and a line-to-line terminating resistor. The drive current of the output stage is set internally eliminating the need for external pulldown resistors. Note that at the output the terminating resistor can be 100 Ω or 150 Ω depending on characteristic impedance of the differential lines, 50 Ω or 75 Ω, respectively.

Figure 10. High Speed Differential Inputs (S2018)

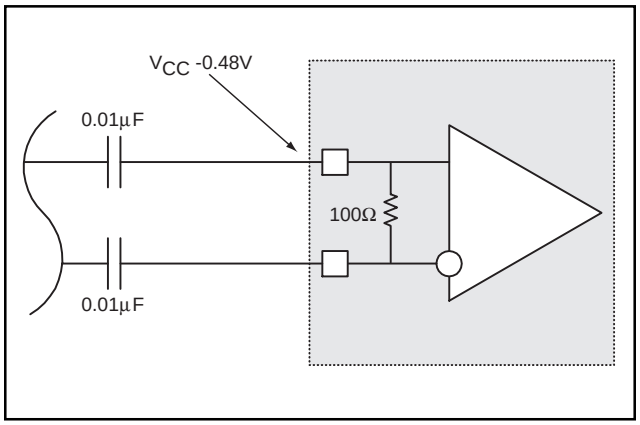


Figure 11. Serial Output Load (S2018)

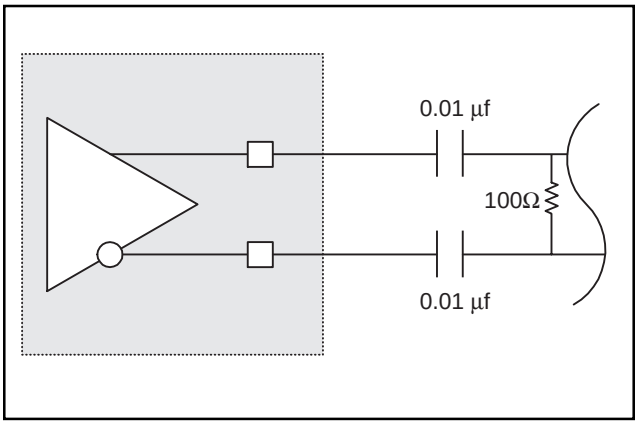
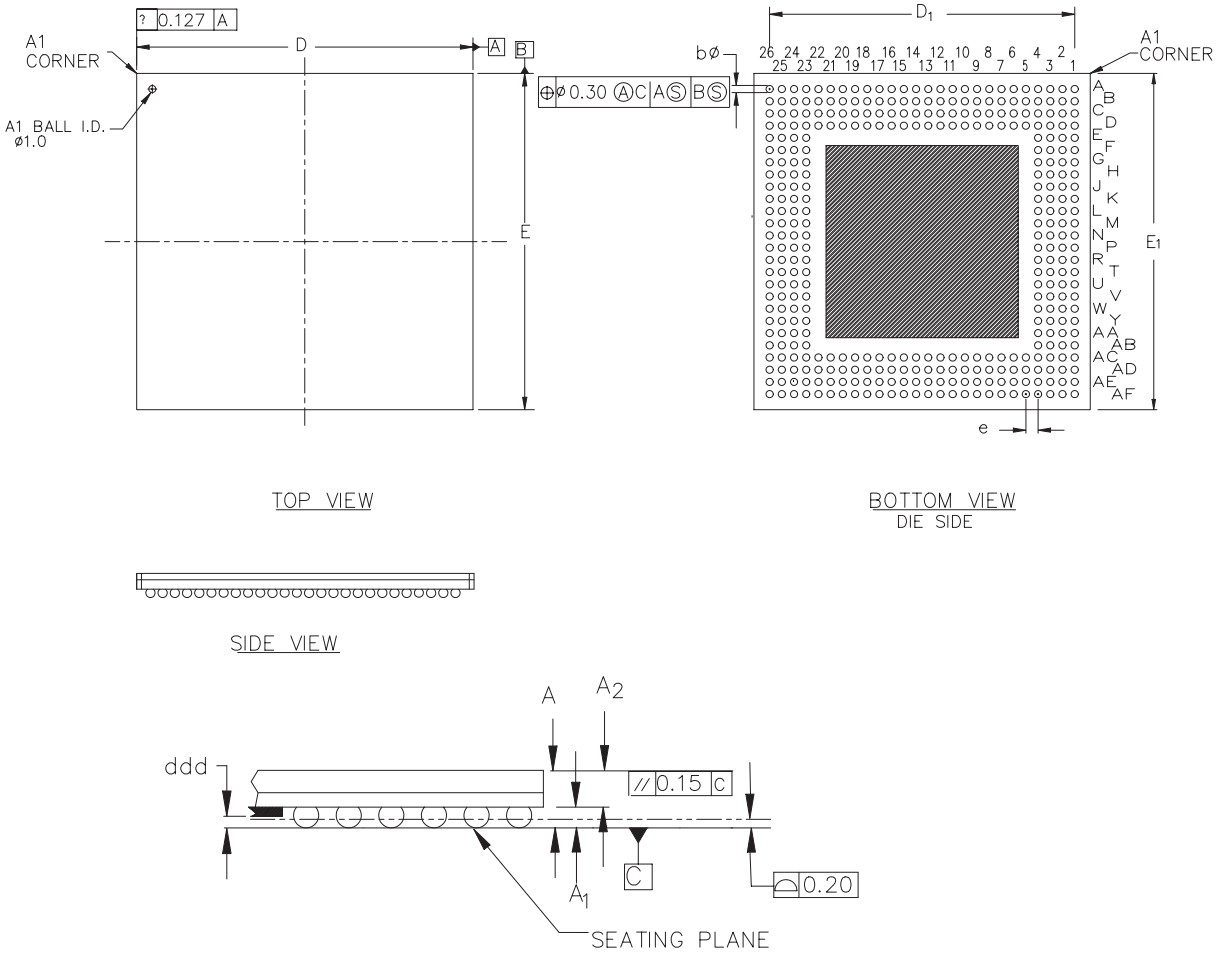


Figure 12. 352 SBGA Package



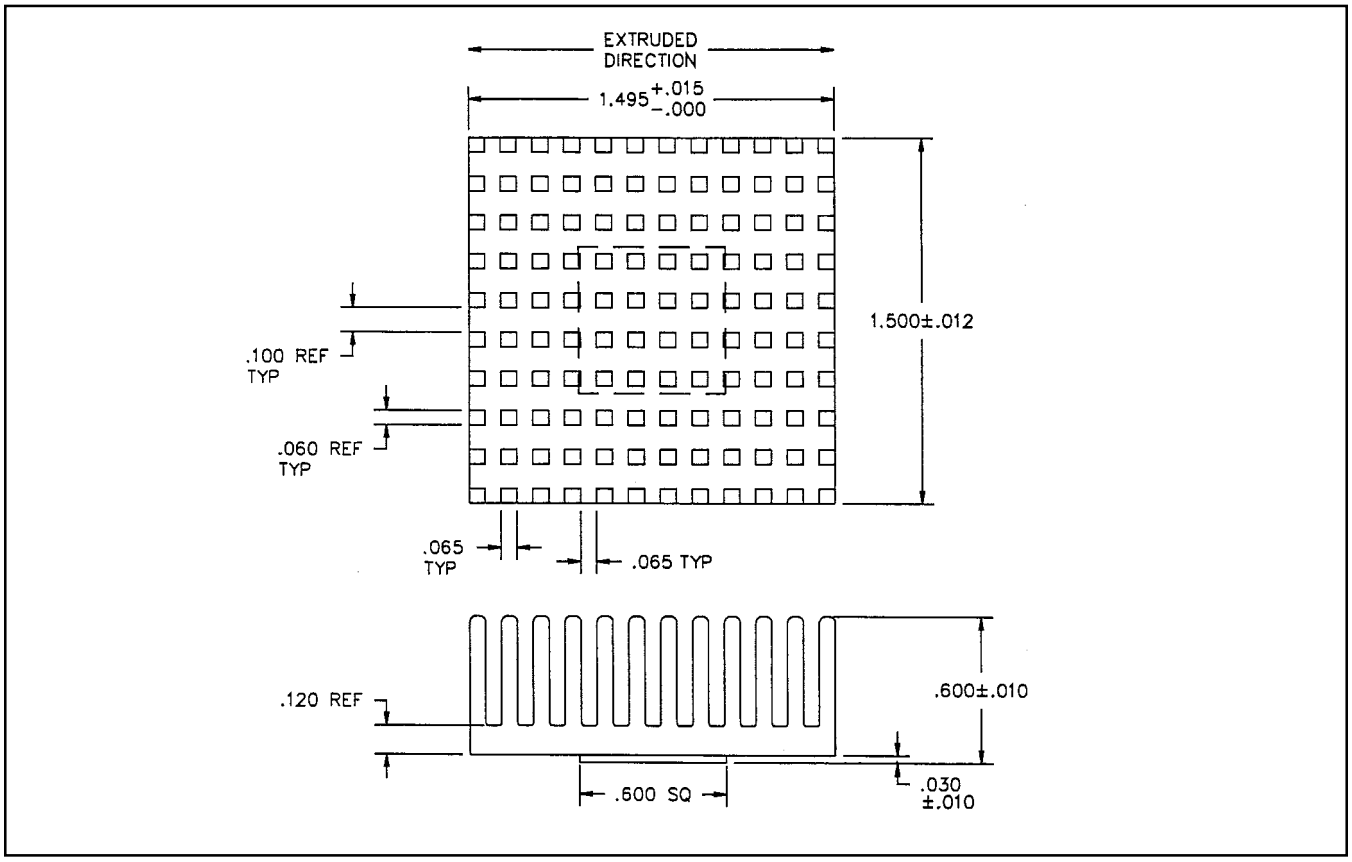
DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	ddd	b	e
MIN	1.41	0.56	0.85	34.90	31.65	34.90	31.65	0.20	0.60	1.27 BSC
NOM	1.54	0.63	0.91	35.00	31.75	35.00	31.75	0.30	0.75	
MAX	1.67	0.70	0.97	35.10	31.85	35.10	31.85	0.35	0.90	

Thermal Data

Device	Θja (Still Air)	Θjc
S2018	16˚ C/W	0.72˚ C/W

Figure 13. AMCC Heat Sink 45-18



Thermal Management

The S2018 device requires sufficient thermal management for proper functionality and reliability. It is recommended that the user investigate, define, and implement correct techniques in thermal management of this product. Techniques to consider include: heatspreading through metal layers within your PCB in addition to heatsinking with mounted heatsink and moving fluid controlled thermal management.

The best heatsink currently available at AMCC is the 45-18 (see Figure 13). This heatsink is capable of handling the thermal management required for the different power dissipation associated with the different programmable output swings. Refer to Table 5 for more information.

Table 5. S2018 Thermal Management

Output Swing (mVpp)	Typical Power (W)	Airflow (LFPM)	Θja (˚ C/W)
240	2.95	100	12.5
440	3.29	100	12.5
600	3.61	200	10.5
780	3.92	200	10.5
940	4.22	200	10.5
1100	4.51	200	10.5
1260	4.8	300	9.75

Table 6. S2018 Data Inputs

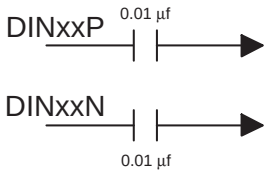
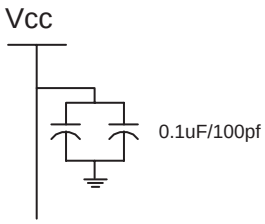
Pin Name	Pin #	Termination Circuit
DIN16P DIN16N DIN15P DIN15N DIN14P DIN14N DIN13P DIN13N DIN12P DIN12N DIN11P DIN11N DIN10P DIN10N DIN9P DIN9N DIN8P DIN8N DIN7P DIN7N DIN6P DIN6N DIN5P DIN5N DIN4P DIN4N DIN3P DIN3N DIN2P DIN2N DIN1P DIN1N DIN0P DIN0N	J2 J2 G2 G1 E2 E1 A4 B4 A6 B6 A8 B8 A10 B10 A12 B12 A14 B14 AE13 AF13 AE11 AF11 AE9 AF9 AE7 AF7 AE5 AF5 AB2 AB1 Y2 Y1 V2 V1	
VCCINPUT	A1, A2, A11, B1, B2, B11, C3, C11, C15, D4, D11, D15, F1, F2, V3, V4, AC1, AC2, AC4, AC9, AC13, AD3, AD9, AE1, AE2, AF1, AF2	

Table 6. S2018 Data Inputs (Continued)

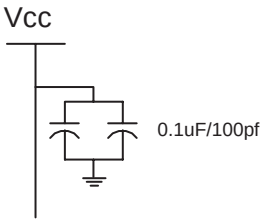
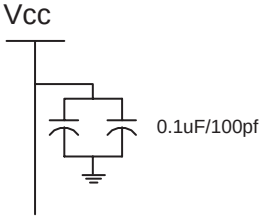
Pin Name	Pin #	Termination Circuit
GNDINPUT	A3, A15, B3, B15, C1, C2, C4, C12, D3, D12, F3, F4, W1, W2, W3, W4, AC3, AC10, AD1, AD2, AD4, AD10, AD13, AE3, AE10, AF3, AF10, AF25, AC24, N4, AE4, AF4, K3, K4, AE24, AE26, AF24, AD23, AD25, AD26, R3, R4, T3, T4, U1, U2, U3, U4, M3, M4, L3, L4, A24, B24, C23, C25, C26, D24, D25, D26	
TTLVCC	C16, D16, J24, K1, K2, P3, AC7, AD7, AE14, AE17, AF14, AF17, AC23, AD24, AE25, AF26	
TTLGND	A16, B16, J3, J4, J23, P4, AC8, AC14, AC17, AD8, AD14, AD17, AE18, AF8	
VCCCORE	A5, A7, A9, A13, B5, B7, B9, B13, C5, C7, C9, C13, C17, D1, D2, D5, D7, D9, D13, G3, G4, R24, Y3, Y4, AB3, AC5, AC11, AD5, AD11, AE15, AF15	

Table 6. S2018 Data Outputs (Continued)

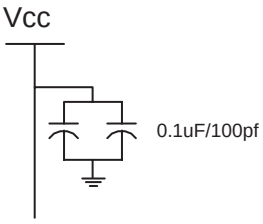
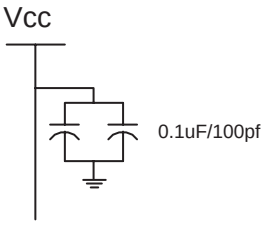
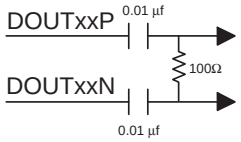
Pin Name	Pin #	Termination Circuit
GNDCORE	C6, C8, C10, C14, D6, D8, D10, D14, D17, E3, E4, H1, H2, H3, H4, R23, AA1, AA2, AA3, AA4, AB4, AC6, AC12, AC15, AD6, AD12, AD15, AE6, AE12, AF6, AF12	
VCC	A18, A20, A22, A25, A26, B18, B20, B22, B25, B26, C18, C20, C24, D18, D20, D23, F23, F24, F25, F26, H23, H24, K23, K24, K25, K26, M23, M24, M25, M26, P23, P24, T23, T24, T25, T26, V23, V24, V25, V26, Y25, Y26, AA23, AA24, AC16, AC18, AC20, AD18, AD20, AD22	
GND	C19, C21, C22, D19, D21, D22, E23, E24, G23, G24, H25, H26, L23, L24, N23, N24, P25, P26, U23, U24, W23, W24, Y23, Y24, AB25, AB26, AC19, AC21, AC22, AD16, AD19, AD21, AE19, AE21, AF19, AF21	

Table 6. S2018 Data Outputs (Continued)

Pin Name	Pin #	Termination Circuit
VCCADJUST	AB24	
GNDADJUST	AB23	
DOUT16P DOUT16N DOUT15P DOUT15N DOUT14P DOUT14N DOUT13P DOUT13N DOUT12P DOUT12N DOUT11P DOUT11N DOUT10P DOUT10N DOUT9P DOUT9N DOUT8P DOUT8N DOUT7P DOUT7N DOUT6P DOUT6N DOUT5P DOUT5N DOUT4P DOUT4N DOUT3P DOUT3N DOUT2P DOUT2N DOUT1P DOUT1N DOUT0P DOUT0N	N26 N25 L26 L25 J26 J25 G26 G25 E26 E25 B23 A23 B21 A21 B19 A19 B17 A17 AF16 AE16 AF18 AE18 AF20 AE20 AF22 AE22 AA26 AA25 W26 W25 U26 U25 R26 R25	

Cascading S2018

For applications where the S2018 is cascaded or connected together, AC coupling capacitors and line-to-line terminating resistors are not required at the interface. DC coupling of the differential output to the differential input is allowed at all output swing settings. The internal terminating resistor at the inputs make external resistors unnecessary. More importantly, the S2018 was designed such that the voltage levels of the outputs and the inputs are compatible eliminating the need for AC coupling capacitors.

Table 7. Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
DIN16P DIN16N DIN15P DIN15N DIN14P DIN14N DIN13P DIN13N DIN12P DIN12N DIN11P DIN11N DIN10P DIN10N DIN9P DIN9N DIN8P DIN8N DIN7P DIN7N DIN6P DIN6N DIN5P DIN5N DIN4P DIN4N DIN3P DIN3N DIN2P DIN2N DIN1P DIN1N DIN0P DIN0N	Diff. LVPECL	I	J2 J1 G2 G1 E2 E1 A4 B4 A6 B6 A8 B8 A10 B10 A12 B12 A14 B14 AE13 AF13 AE11 AF11 AE9 AF9 AE7 AF7 AE5 AF5 AB2 AB1 Y2 Y1 V2 V1	Input data. Differential.
OADDR4 OADDR3 OADDR2 OADDR1 OADDR0	LVTTL	I	P1 R2 R1 T2 T1	Output address. Active High. Used to select an output configuration register in the configuration register file.
IADDR4 IADDR3 IADDR2 IADDR1 IADDR0	LVTTL	I	N2 M2 M1 L2 L1	Input address. Active High. IADDR[4-0] selects the input pair to connect to the output pair selected by OADDR[4-0].
LOADN	LVTTL	I	P2	Load strobe. Active Low. When active, stores the configuration data on IADDR[4-0] into the configuration register file.
CONFIGN	LVTTL	I	N3	Configuration strobe. Active Low. When active, parallel loads the contents of the configuration register file into the active configuration latch.
VCSHIGH		O	AF23	Output Swing Adjust. Used to tie to VADJUST_X pin(s) for adjustable output swing. See Table 1 for details.

Table 7. Pin Assignment and Description (Continued)

Pin Name	Level	I/O	Pin #	Description
VADJUST1 VADJUST2 VADJUST3		I	AE23 AC25 AC26	Used to tie to VCSHIGH pin, per Table 1 for adjustable output swing.
CSN	LVTTL	I	N1	Chip Select. Active Low. When inactive, the LOADN signal will be ignored. New addresses will not be allowed. When active, S2018 will operate as specified.
DOUT16P DOUT16N DOUT15P DOUT15N DOUT14P DOUT14N DOUT13P DOUT13N DOUT12P DOUT12N DOUT11P DOUT11N DOUT10P DOUT10N DOUT9P DOUT9N DOUT8P DOUT8N DOUT7P DOUT7N DOUT6P DOUT6N DOUT5P DOUT5N DOUT4P DOUT4N DOUT3P DOUT3N DOUT2P DOUT2N DOUT1P DOUT1N DOUT0P DOUT0N	Diff. CML	O	N26 N25 L26 L25 J26 J25 G26 G25 E26 E25 B23 A23 B21 A21 B19 A19 B17 A17 AF16 AE16 AF18 AE18 AF20 AE20 AF22 AE22 AA26 AA25 W26 W25 U26 U25 R26 R25	Output data. Differential.

Table 8. Power and Ground Signals

Pin Name	Quantity	I/O	Pin #	Description
VCCINPUT	27		A1, A2, A11, B1, B2, B11, C3, C11, C15, D4, D11, D15, F1, F2, V3, V4, AC1, AC2, AC4, AC9, AC13, AD3, AD9, AE1, AE2, AF1, AF2	Power for high speed circuitry.
GNDINPUT	60		A3, A15, B3, B15, C1, C2, C4, C12, D3, D12, F3, F4, W1, W2, W3, W4, AC3, AC10, AD1, AD2, AD4, AD10, AD13, AE3, AE10, AF3, AF10, AF25, AC24, N4, AE4, AF4, K3, K4, AE24, AE26, AF24, AD23, AD25, AD26, R3, R4, T3, T4, U1, U2, U3, U4, M3, M4, L3, L4, A24, B24, C23, C25, C26, D24, D25, D26	Ground for high speed circuitry.
TTLVCC	16		C16, D16, J24, K1, K2, P3, AC7, AD7, AE14, AE17, AF14, AF17, AC23, AD24, AE25, AF26	Power for TTL inputs.
TTLGND	14		A16, B16, J3, J4, J23, P4, AC8, AC14, AC17, AD8, AD14, AD17, AE8, AF8	Ground for TTL inputs.
VCCCORE	31		A5, A7, A9, A13, B5, B7, B9, B13, C5, C7, C9, C13, C17, D1, D2, D5, D7, D9, D13, G3, G4, R24, Y3, Y4, AB3, AC5, AC11, AD5, AD11, AE15, AF15	Core circuitry power.
GNDCORE	31		C6, C8, C10, C14, D6, D8, D10, D14, D17, E3, E4, H1, H2, H3, H4, R23, AA1, AA2, AA3, AA4, AB4, AC6, AC12, AC15, AD6, AD12, AD15, AE6, AE12, AF6, AF12	Core circuitry ground.

Table 8. Power and Ground Signals (Continued)

Pin Name	Quantity	I/O	Pin #	Description
VCCADJUST	1		AB24	Power for VADJUST input.
GNDADJUST	1		AB23	Ground for VADJUST input.
VCC	50		A18, A20, A22, A25, A26, B18, B20, B22, B25, B26, C18, C20, C24, D18, D20, D23, F23, F24, F25, F26, H23, H24, K23, K24, K25, K26, M23, M24, M25, M26, P23, P24, T23, T24, T25, T26, V23, V24, V25, V26, Y25, Y26, AA23, AA24, AC16, AC18, AC20, AD18, AD20, AD22	3.3V power supply.
GND	36		C19, C21, C22, D19, D21, D22, E23, E24, G23, G24, H25, H26, L23, L24, N23, N24, P25, P26, U23, U24, W23, W24, Y23, Y24, AB25, AB26, AC19, AC21, AC22, AD16, AD19, AD21, AE19, AE21, AF19, AF21	Ground.

S2018 With S2092

In applications where serial data retiming and buffering is required, the S2092 serial backplane retimer will be needed. The S2092 receives differential serial data as input and recovers the clock from the incoming data stream. Next the recovered clock is used to retime the serial data. Then the S2092 buffers out the serial data as output. This document should be used in conjunction with the S2018 datasheet and the S2092 datasheet. A specific application note is available that shows the electrical connection between the two devices.

S2092 General Description

The S2092 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 15.

The S2092 retimer device performs clock recovery on serial data links from 2.488 Gbps to 2.67 Gbps. The chip extracts the clock from the serial data inputs and provides retimed data outputs. A 155.52 to 166.63 or 19.44 to 20.83 MHz (REFCLK frequency is dependent on which FEC capability is required. See Table 10.) reference clock is required for phase locked loop start up and proper operation under loss of signal conditions. See Table 9. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

Figure 14. S2018 With S2092 System Block Diagram

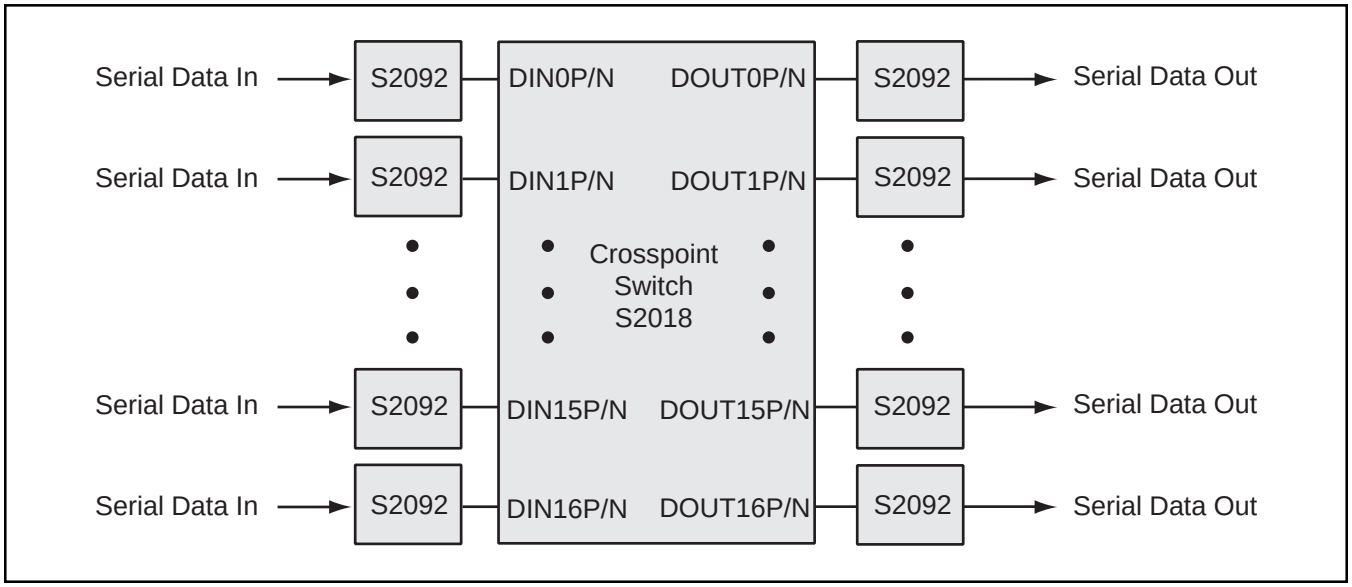


Figure 15. S2092 Functional Block Diagram

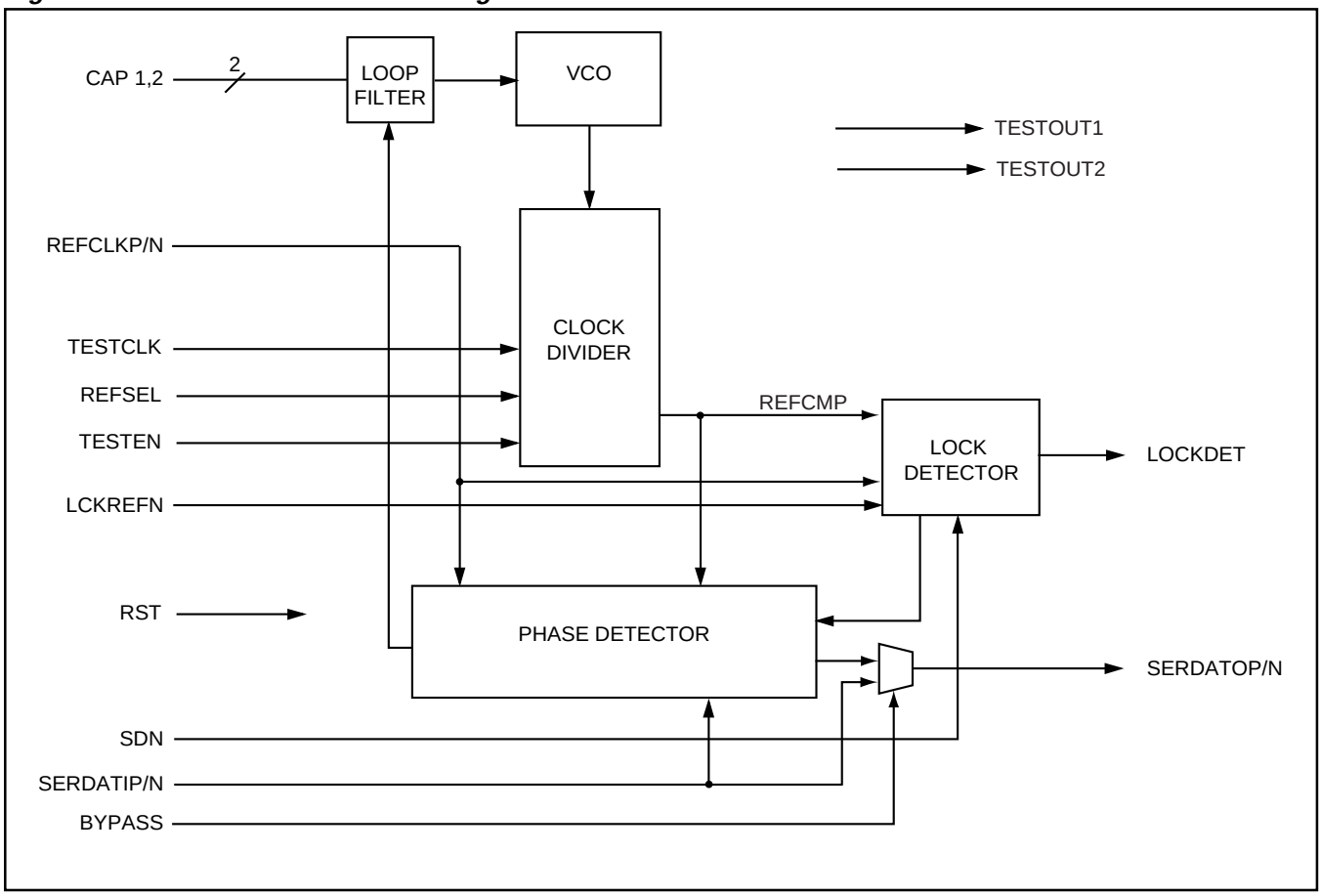


Table 9. S2092 Reference Frequency Select

REFSEL	Reference Frequency
0	19.44 to 20.83 MHz
1	155.52 to 166.63 MHz

Table 10. FEC Modes

REFSEL	Reference Frequency for Data Rates with FEC Capability of X bytes per 255–Byte Block						
	X = 0	X = 3	X = 4	X = 5	X = 6	X = 7	X = 8
0	19.44 MHz	19.99 MHz	20.15 MHz	20.31 MHz	20.48 MHz	20.65 MHz	20.83 MHz
1	155.52 MHz	159.91 MHz	161.21 MHz	162.53 MHz	163.87 MHz	165.26 MHz	166.63 MHz

REFERENCE DESIGN

Figure 16. Typical Router Operation Setup

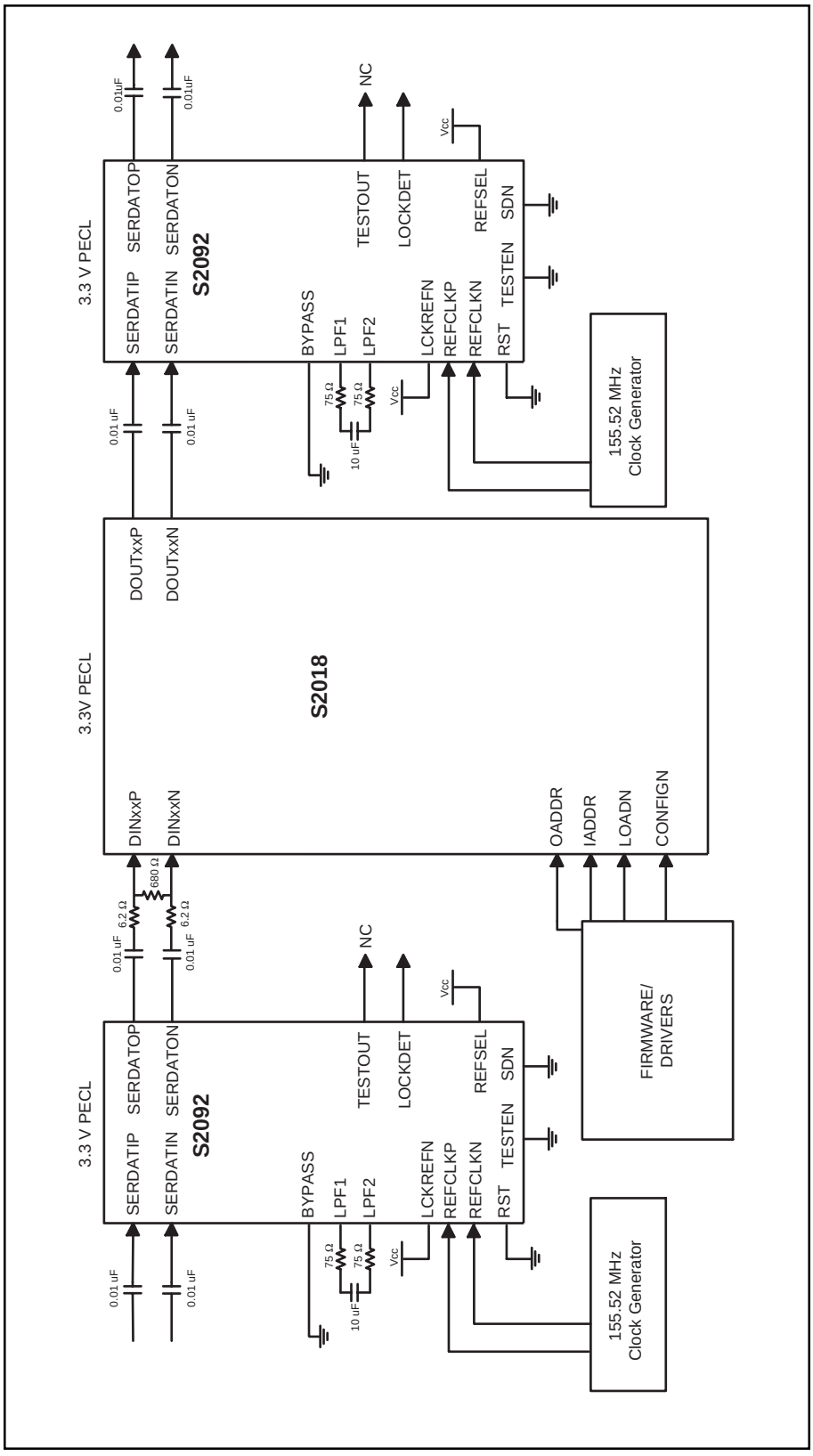


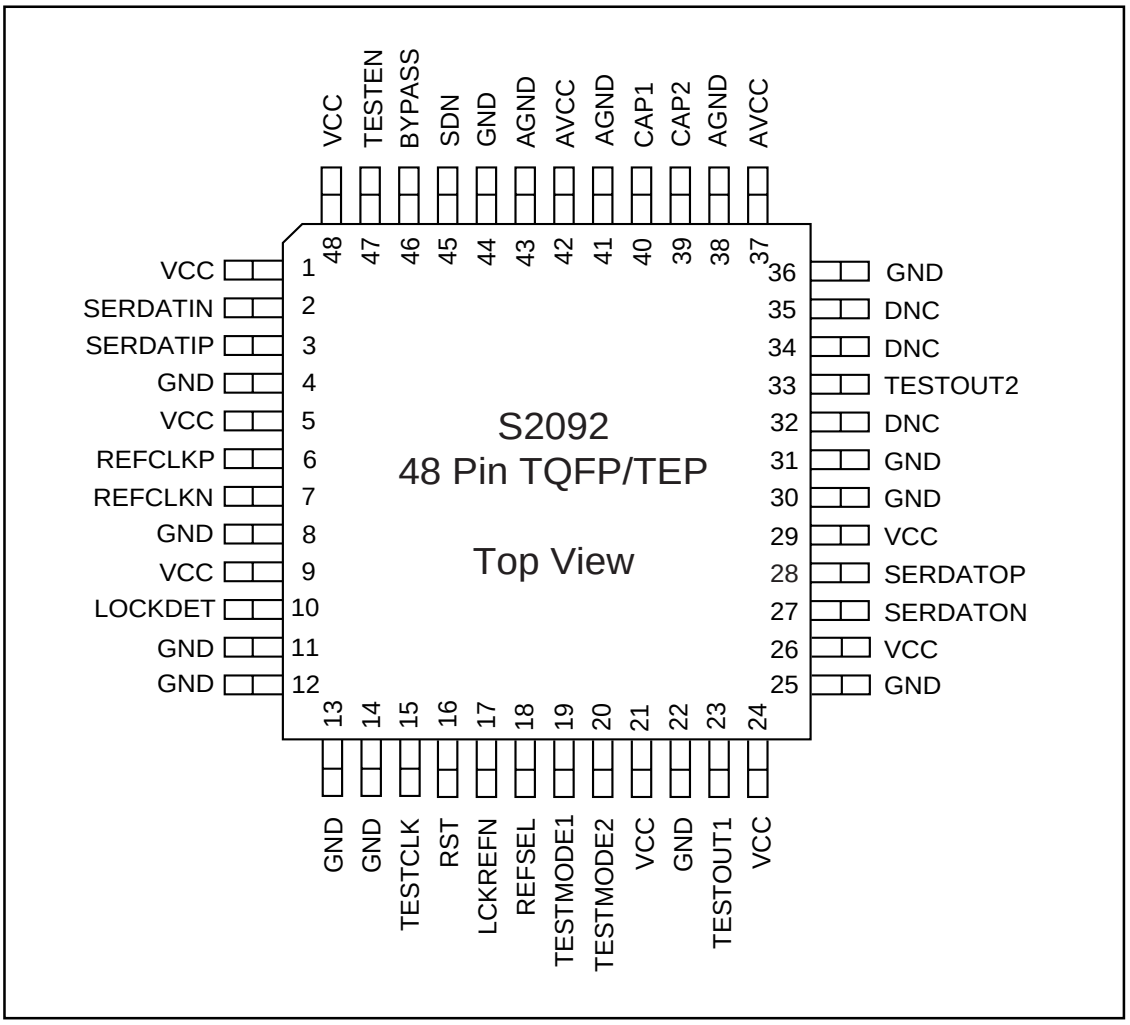
Table 11. S2092 Pin Assignment and Description

Pin Name	Level	I/O	Pin#	Description
SERDATIP SERDATIN	Diff. CML	I	3 2	Serial Data In. Clock is recovered from the transitions on these inputs. Internally biased and terminated. (See Figure 19.)
BYPASS	LVTTL	I	46	Active High. Used to bypass the PLL. It allows transmission of data input without clock recovery.
SDN	LVPECL	I	45	Signal Detect. Active Low. A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDN is inactive, the data on the Serial Data In (SERDATIP/N) pins will be internally forced to a constant zero, and the PLL will be forced to lock to the REFCLK inputs. When SDN is active, data on the SERDATIP/N pins will be processed normally.
REFCLKP REFCLKN	Diff. LVPECL	I	6 7	Reference Clock. 155.52 to 166.63 or 19.44 to 20.83 MHz (see Table 10 for additional reference clock frequencies) input used to establish the initial operating frequency of the clock recovery PLL and also used as a standby clock in the absence of data, during reset, or when SDN is inactive. Internally biased.
CAP1 CAP2		I	40 39	Loop Filter Capacitor. The loop filter capacitor and resistors are connected to these pins. (See Figure 22.)
LCKREFN	LVTTL	I	17	Lock to Reference. Active Low. When active, the serial output will be invalid.
TESTCLK	LVTTL	I	15	Test input signal used for production test. Leave open (no DC connection) for normal operation.
REFSEL	LVTTL	I	18	Selects the reference frequency (See Table 9.)
RST	LVTTL	I	16	Active High. Resets lock detect circuit and VCO divide-by-N circuit for production test.
TESTEN	LVTTL	I	47	Test Enable. Active High. Bypasses the VCO for production test. Tie Low for normal operation.
SERDATOP SERDATON	Diff. CML	O	28 27	Serial Data Out. This signal is the delayed version of the incoming data stream (SERDATI).
LOCKDET	LVTTL	O	10	Lock Detect. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming data stream. LOCKDET is an asynchronous output.
TESTOUT1		O	23	Test Output. Leave open (no DC connection) for normal operation.
TESTOUT2		O	33	Test Output. Leave open (no DC connection) for normal operation.
TESTMODE1	LVTTL	I	19	Test Mode Control. Keep High for normal operation.
TESTMODE2	LVTTL	I	20	Test Mode Control. Keep High for normal operation.

Table 11. S2092 Pin Assignment and Description (Continued)

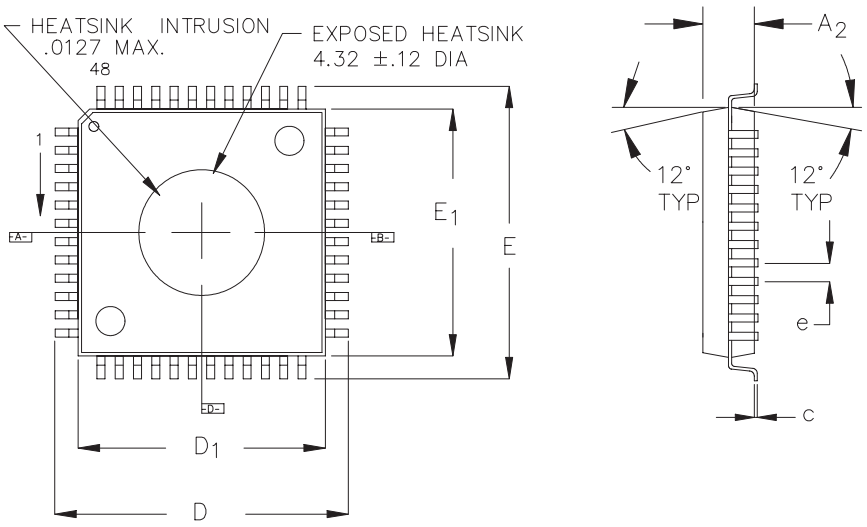
Pin Name	Qty.	Pin#	Description
AVCC	2	37, 42	+3.3 V Analog power supply.
AGND	3	38, 41, 43	Analog GND connection.
VCC	8	1, 5, 9, 21, 24, 26, 29, 48	+3.3 V Power Supply.
GND	12	4, 8, 11, 12, 13, 14, 22, 25, 30, 31, 36, 44	Ground connection.
DNC	3	32, 34, 35	Do Not Connect. Used as test pins.

Figure 17. S2092 Pinout

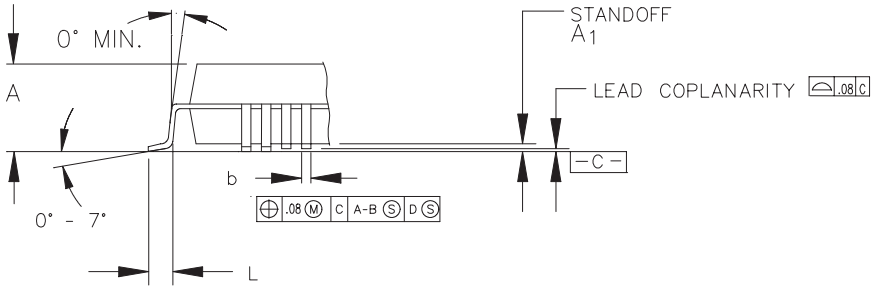


Note: DNC used as test pins. Do not connect.

Figure 18. S2092 Compact 7 mm x 7 mm 48 Pin TQFP/TEP Package



TOP VIEW



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	8.80	6.90	8.80	6.90	0.75	0.50 BSC.	0.17	
NOM			1.40	9.00	7.00	9.00	7.00	0.60		0.22	1.27
MAX	1.60	0.15	1.45	9.20	7.10	9.20	7.10	0.50		0.27	

Thermal Management

Device	Package Max Power	Θja
S2092	650 mW	50° C/W

Table 12. S2092 Power and Ground

Function	Pinout Name	Instructions
ANALOG	AVCC	Connect to low noise or filtered 3.3V supply through a ferrite bead (600 Ω at 100 MHz: Murrata BLM31B601S or equivalent). Provide dual local HF bypassing to AVEE (0.1 µf, 100 pf) for low inductance and resistance. A single low inductance 0.1 µf capacitor can be substituted for the pair (Vishay VJ0612 or equivalent, < 0.5 nH max inductance).
	AGND	Connect to ground plane.
CORE	VCC	Provide low impedance connection to 3.3V. Provide dual local bypassing to GND plane (0.1 µf and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µf capacitor).
	VEE	Connect to ground plane.

Figure 19. +5 V Differential PECL Driver to S2092 Input AC Coupled Termination

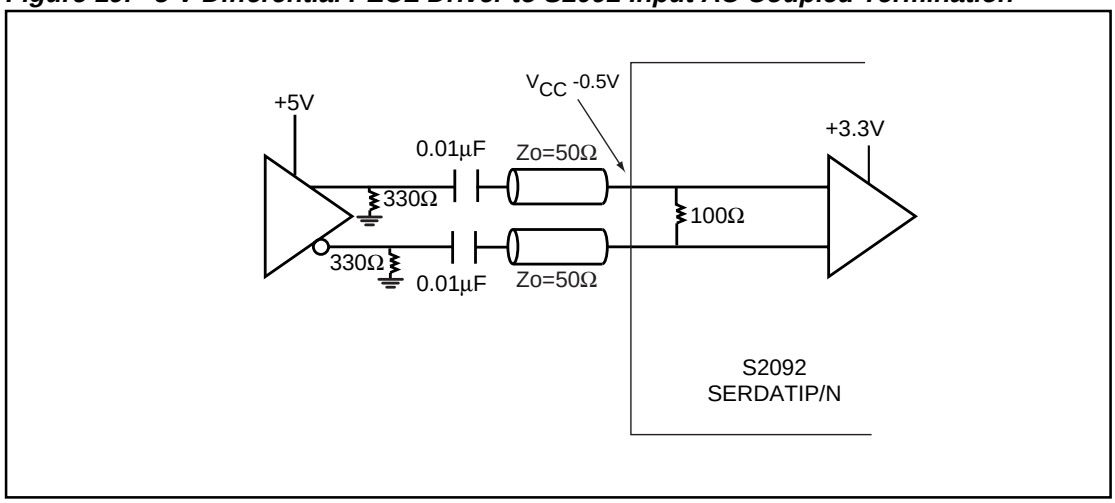


Figure 20. +5 V Differential PECL Driver to S2092 Reference Clock Input AC Coupled Termination

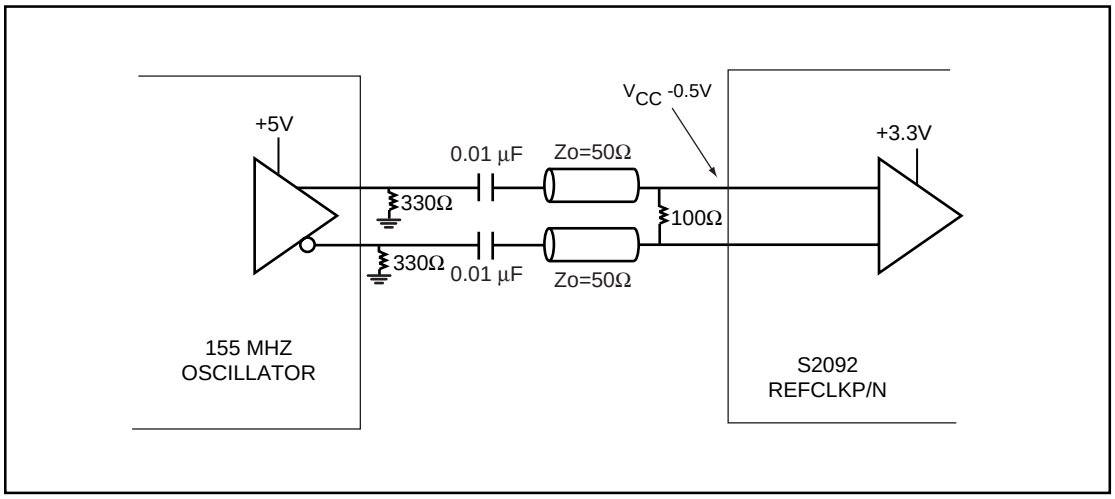


Figure 21. +3.3 V Differential LVPECL Driver to S2092 Reference Clock Input DC Coupled Termination

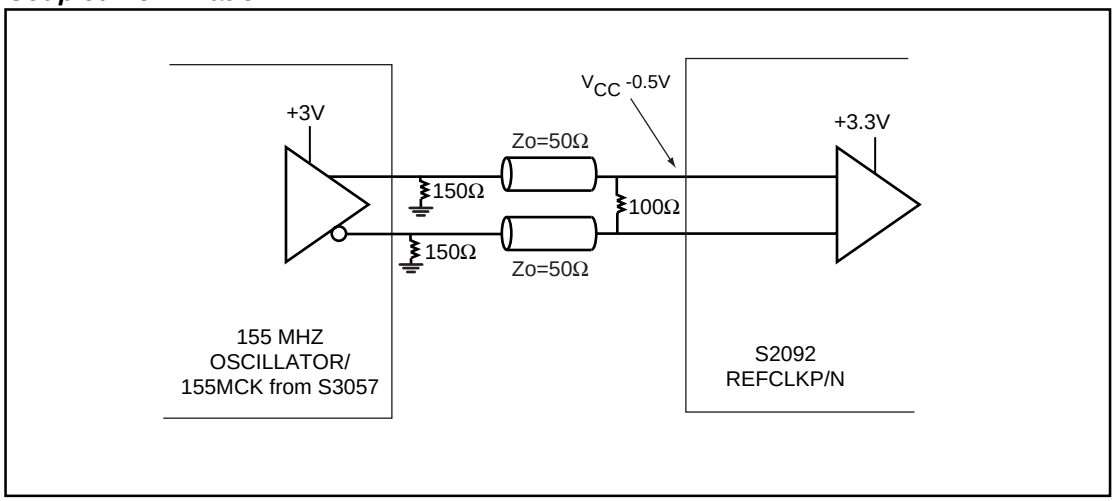
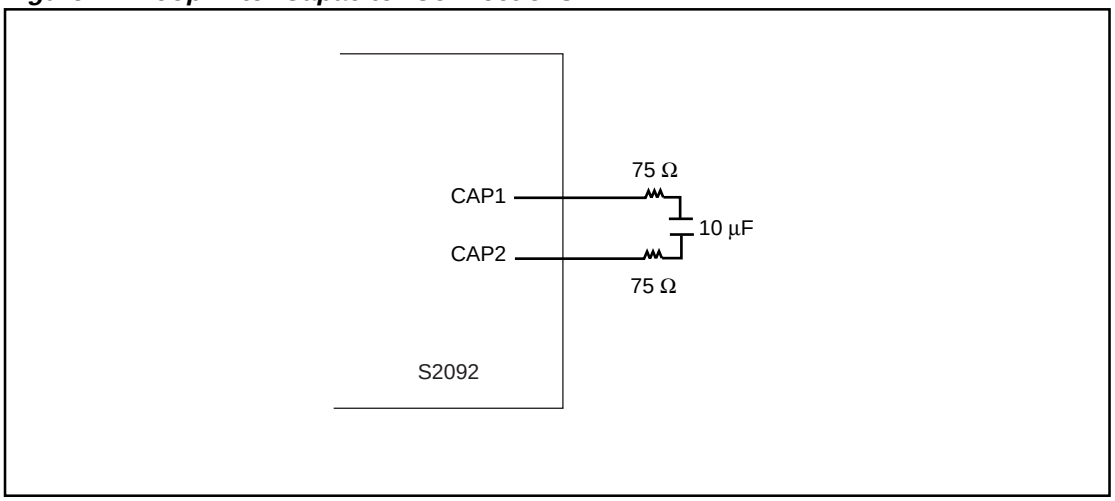


Figure 22. Loop Filter Capacitor Connections



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