ADVANCED SUMMARY DATASHEET

GANGES

STS-192 POS/ATM SONET/SDH MAPPER

Features

- Supports full duplex mapping of ATM cells or packets for a single STS-192c/AU-4-64c, four STS-48c/AU-4-16c or sixteen STS-12c/AU-4-4c SONET/SDH payloads.
- Supports quad STS-48/STM-16 line interfaces. Each STS-48/STM-16 can support a concatenated payload, or can be channelized down to STS-12c/AU-4-4c.
- Terminates and generates SONET/SDH section, line, & path layers, with transport/section E1, E2, F1 and DCC overhead interfaces in both transmit and receive directions.
- Provides a 622.08 MHz 16-bit bus interface on the line side in both the TX and RX directions.
- Provides a 64-bit, 200 MHz system interface that supports the transfer of either packets or ATM cells.
- Selectable scrambling/descrambling ($1+X^6+X^7$) of SONET/SDH frame.
- 16-bit synchronous microprocessor interface for configuration, control, and status monitoring.
- Supports independent loop timing when in quad STS-48/STM-16 mode.
- Supports Automatic Protection Switching (APS)
- Packaged in a 624-pin CBGA.
- Implemented in .18 micron, 1.8V and 2.5V technology.

General Description

The GANGES IC is a highly-integrated VLSI device that provides full-duplex mapping of packets or ATM cells into SONET/SDH payloads.

GANGES provides full section and line overhead processing for either a single STS-192/STM-64, or four STS-48/STM-16s. It supports framing, scrambling and descrambling, alarm signal insertion and detection, and bit interleaved parity (B1/B2) processing. It also provides path overhead processing for STS-192c/AU-4-64c, STS-48c/AU-4-16c or STS-12c/AU-4-4c SONET/SDH payloads and includes bit interleaved parity (B3) processing.

The GANGES IC includes an automatic protection switching (APS) port, that permits protection switching between two GANGES devices.

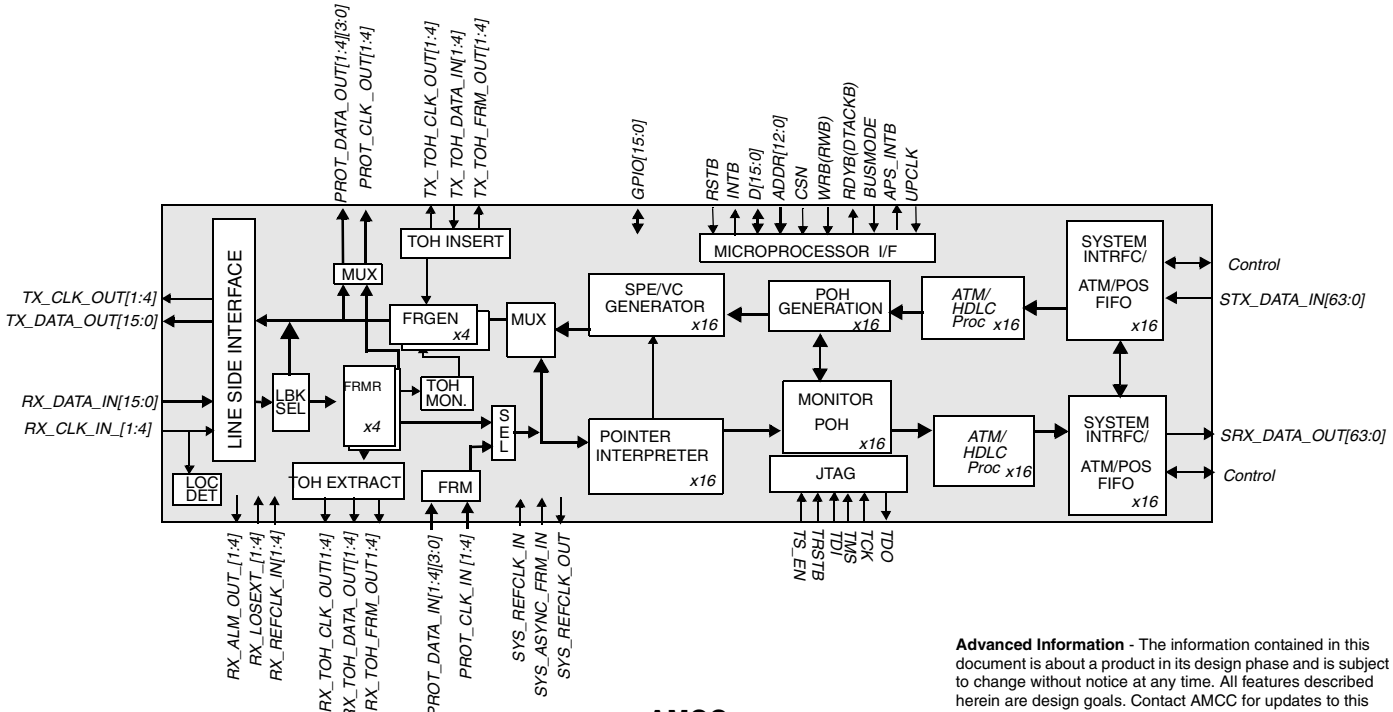
The S19202 is SONET/SDH standards compliant with Bellcore GR-253, ITU G.707, and ANSI T1.105 -1995.

A general purpose 16-bit microprocessor interface is provided for control, and monitoring.

Applications

- ATM switches and Packet over SONET Routers
- SONET/SDH Add Drop Multiplexers, Terminal Multiplexers and Digital Cross Connects
- WDM and DWDM

S19202 Block Diagram



Overview and Applications

SONET Processing

The S19202 supports either a single STS-192/STM-64, or four STS-48/STM-16 SONET/SDH Line interfaces. It provides full duplex mapping of ATM cells or packets for STS-192c/AU-4-64c, STS-48c/AU-4-16c, and/or STS-12c/AU-4-4c SONET/SDH payloads.

A TOH/SOH interface provides direct add/drop capability for E1, E2, F1, and both Section and Line DCC channels. The S19202 also includes a clear channel mode that enables the direct transmission of system payload from the system interface to the line-side interface.

Side door APS interfaces are supported in both the TX and RX directions.

On the transmit side the S19202 generates section, line, and path overhead. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and generates section, line and path Bit Interleaved Parity (B1/B2/B3) for far-end performance monitoring.

On the receive side the S19202 processes section, line, and path overhead. It performs framing (A1, A2), descrambling, alarm detection, pointer interpretation, bit interleaved parity monitoring (B1/B2/B3), and error count accumulation for performance monitoring.

ATM Processing

When configured for ATM cell processing, the S19202's ATM processor(s) will perform all necessary cell processing as defined by ATM UNI3.1 and ITU-T I.432.1 and I.432.2.

HDLC Processing

When configured for POS mode, the S19202's HDLC processor(s) provide the insertion of HDLC framed packets into the STS SPE(s)/STM VC(s). The S19202 performs HDLC processing as defined by IETF RFCs 1661, 1662 and 2615.

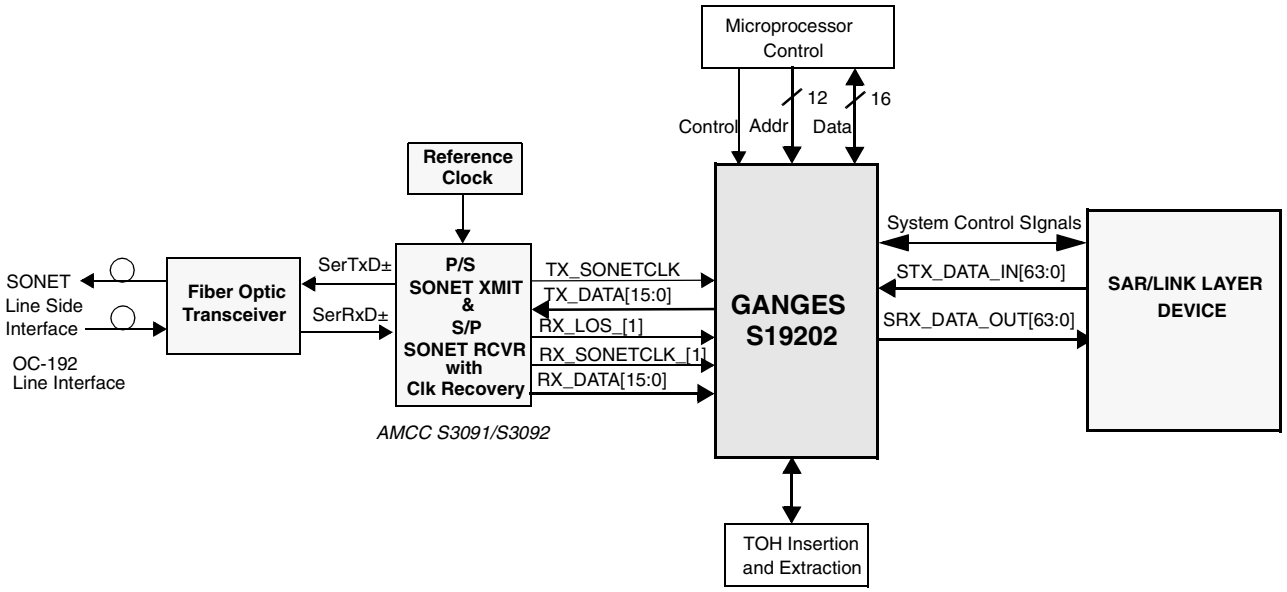
Line-side Interface

On the line-side, the S19202 supports a 16-bit parallel interface, operating at 622MHz, for a single OC-192 optical interface. For quad STS-48/STM-16 operation, the S19202 supports four 4-bit, 622 MHz, line interfaces. (See figure below.)

System Interface

The GANGES IC provides a 64-bit, 200 MHz, system interface for the transport of either packets or ATM cells.

TYPICAL APPLICATIONS: GANGES in a STS-192/AU-4-64 channelized System



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