S2020 HIPPI SOURCE CONNECT CONTROL

The S2020 Source Device meets the signalling protocol for the Hippi-Source as determined by ANSI X3.183-1991 HiPPI-PH Mechanical Electrical and Signalling Protocol Specification. As the Source, the S2020 functions as the initiator and controller of all data transfers on the Hippi channel.

The RESET Command (Mode 0) initializes all internal state machines in the S2020 and clears all data and parity bit registers to zero. The only function that is not cleared or held at an initialized state is the clock control which generates the internal 25 MHz and the external RDCLK signal. The RESET Command provides phase control of the internal and external clocks.

If the RESET Command is placed on the MODE(2:0) inputs while the RDCLK output is in the logic high state, there will be no change in the continuous 25 MHz signal observed at the RDCLK output. If, however, the RESET Command is placed on the MODE(2:0) inputs while the RDCLK output is in the logic low state, the RDCLK output will go high after the next rising edge of the 50 MHz input, remain high for two cycles of the 50 MHz input and then produce a rising edge on the third 50 MHz falling edge applied to the S2020. From that point until the next application of the RESET Command the RDCLK (and the internal clocks) will be a continuous 25 MHz signal synchronized to the 50MHZ input rising edge.

This “phase slip on low” function can be used to unambiguously set the phase relation between the 50 MHz input and the RDCLK output. Since most of the Host interface control inputs are required to be synchronous with the 25 Mhz RDCLK output, this phase slip control gives the user the capability of aligning the S2020’s timing to the 50 MHz and 25 MHz used in the external Host circuitry.

It should be noted that while the RESET Command clears the Parity Error bit (INPRR output), the internal data and parity registers have also been cleared. This “zero data/zero parity” condition is a Parity Error with respect to the HIPPI odd byte parity convention. If a parity correct word is present at the inputs of the S2020 at the time the RESET state is exited, there will be a two clock period parity error bit on the INPRR output. If the attached FIFO has also been cleared during the RESET Command, the INPRR bit will remain high until three clocks after the first read cycle of the FIFO.

While there are some differences in FIFO or “FIFO equivalent” memory structures that have been successfully used with the S2020, the available or announced synchronous clocked FIFOs from IDT, Cypress and Sharp all share this feature. Even if the external data source memory had “correct” parity available at the inputs of the S2020, the two clock period parity error would be observed.

The first function that must be performed after the power-up initialization of the S2020 (RESET Mode 0) is to determine the status of the Destination to Source Interconnect [DSIC] signal. That signal, generated by the remote HIPPI Destination, is an input signal from the HIPPI Channel to the S2020 and must be in the logic low (active) state for any control or data transfer functions to be valid on the HIPPI Channel.

The filtered and inverted state of the DSIC input is available at the Destination Available [DSTAV] output. Since the S2020 has the capability of switching its own Source to Destination output signal to the inactive state during Reset and Board Test modes, the Device must be placed in the Wait for Destination mode (Mode 2) immediately after RESET to allow the filter to recognize either the static low (active) DSIC input or the high to low transition of the DSIC input.

If the S2020 is placed directly from the RESET Mode into the Operational Mode (Mode 3), the DSTAV output will not correctly respond to the DSIC input state, even if the DSIC input is already in the active low condition when the RESET to Operational mode change is made. The Wait for Destination mode avoids possible control ambiguities in systems where both Source and Destination have active control of their respective Interconnect signals.

With the S2020 in the Wait for Destination mode (Mode 2), the observation of an active high state on the DSTAV output indicates that the internal reset and initialization cycle of the entire HIPPI Channel (both Source and Destination) is complete. The S2020 may now be legally placed in the Operational mode, and the internal Connect State Machine of the S2020 will be placed in the {IDLE} state.

If there is any interruption of the DSIC input greater than the filter integration time (four clock cycles), the Connect State Machine will be forced to the {LOSTDEST} state. This will immediately stop any current data transfer, and cause the REQUEST, PACKET and BURST signals on the HIPPI Channel to go to the inactive state. The DSTAV signal will go low to indicate this condition to the Source Host System. The only recovery from this condition is the RESET and WAIT sequence described above. It is the responsibility of the Source Host System to exercise a reasonable “time-out” if the remote Destination does not generate a stable active low state on the DSIC signal.

Once the DSTAV signal is observed at an active high state and the Operational Mode (Mode 3) is commanded, the S2020 is ready to initiate a Connection Request sequence. The design of the S2020 is optimized to use the external synchronous FIFO as the source of the I-Field Word as well as the PKTAV and SHBST signals used to flag the I-Field Word. If the I-Field and/or the two control signals are not placed in the FIFO, care must be taken that their timing is controlled to meet the specification of the Data Sheet. Failure to honor that timing will cause erroneous and unpredictable operation of the FIFO with resultant data loss.

The S2020 acts as a continuously running, two register deep pipeline. In the HIPPI application, the only point at which a data word is held static for multiple clock cycles is the output register of the FIFO. The NREN output of the S2020 is applied to the Not Read Enable input of the FIFO to control this register.

It should be also noted that for the recommended FIFO and most equivalents, the operation of writing into the FIFO from the Host System does not directly write any data into the FIFO's output register. The data in the output register is indeterminate (it may be zero if the entire system including the FIFO was initialized, otherwise it is usually the last transmitted data word.)

Placing the I-Field and the two signals defining the I-Field in the FIFO eliminates any ambiguity as to the previous contents or state of the FIFO. If the FIFO has been filled with data, and the Not Empty output of the FIFO is connected to the DATAV input of the S2020, then a high signal on the CNREQ input and the high signal already at the DATAV input will cause an active low on the NREN output. The NREN signal will remain low for at least one cycle of the 25 MHz RDCLK until the 01 condition is observed on the PKTAV and SHBST inputs respectively.

The detection of the 01 condition will asynchronously raise the NREN signal to the inactive state, locking the current data word (assumed by its PKTAV/SHBST label to be the I-Field) in the output register of the FIFO. Two clock cycles later, this data is available at the HIPPI Channel outputs and the REQUEST signal is asserted on the HIPPI Channel.

The REQUEST signal will remain active on the HIPPI Channel until the CNREQ input is returned to the logic low state. The S2020 will make no more read requests of the FIFO until the Destination has responded with a Connect Accept or a Connect Reject. This status is indicated by the CNOUT and ACREJ signals. If both of these outputs are at logic high, the Connection has been accepted and recognized at both Source and Destination.

The S2020 distinguishes between Connect Accept and Connect Reject conditions in accordance with the HIPPI Specification. If the CONNECT signal from the HIPPI Channel is detected for less than four clock cycles (160 nsec) it is ignored and the S2020 remains in the {REQ} state.

If the CONNECT signal is detected for more than three and less than twenty clock cycles with no activity detected on the READY signal, The Destination is judged to have issued an active Connect Rejection. In that case the S2020 will place a logic high on the CNOUT output and a logic low on the ACREJ output. This condition will persist until the Host returns the CNREQ signal to the low state or the Host executes the Mode 0 Reset sequence.

The READY signal is also monitored to determine the Connect Accept or Connect Reject status. If the READY signal is detected two or more clock cycles after the detection of CONNECT signal, the Connection is considered as accepted and the 11 pattern is posted to the CNOUT and ACREJ outputs. If the Destination drops the CONNECT signal at this point while the CONREQ input remains high, the {DESTERR} state is entered.

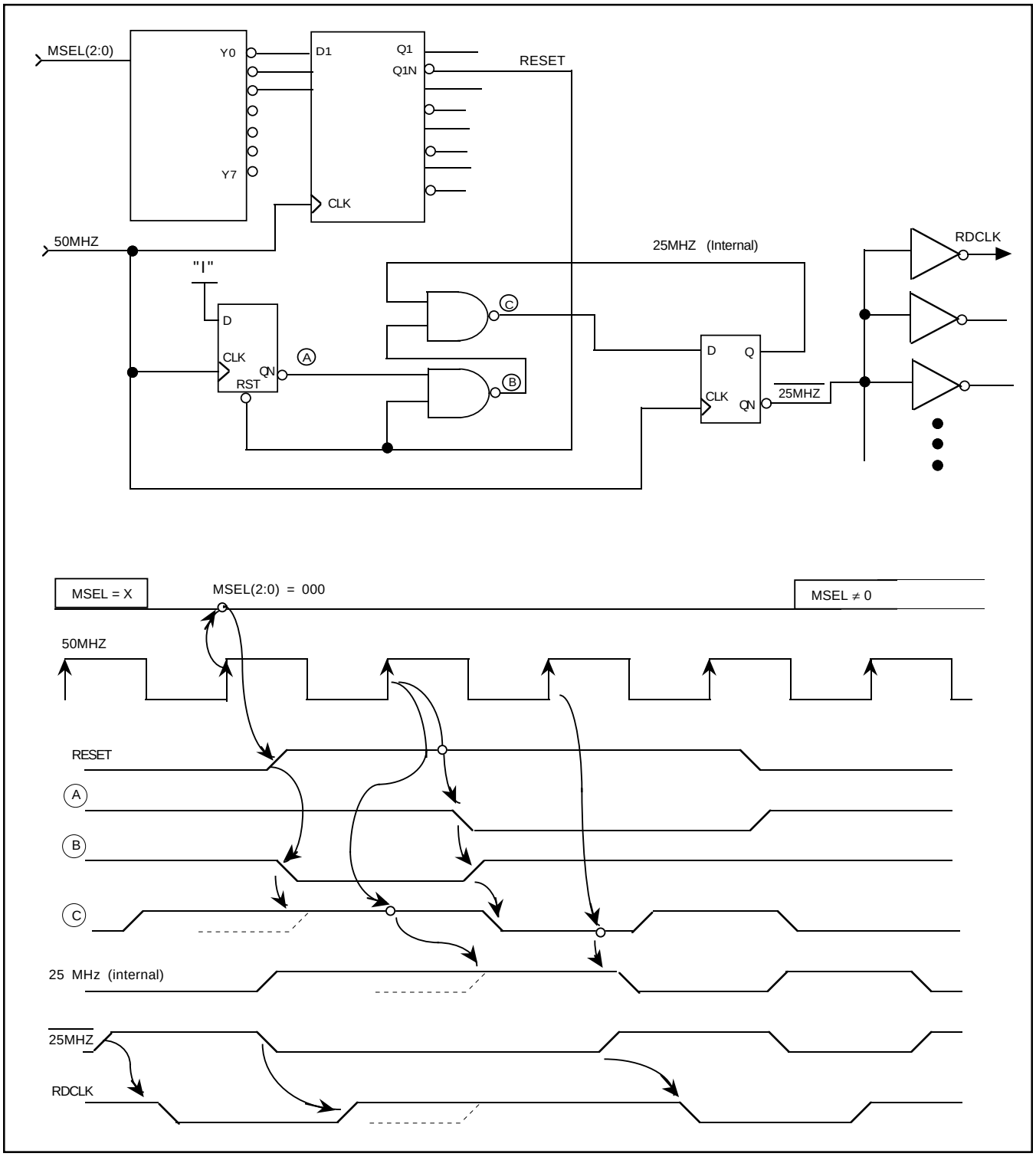
If a READY signal is detected during the Connect Request cycle or later at any time while in the {CONNECTED} state, the Ready counter in the S2020 will be incremented by one. This counter and a similar Burst counter (incremented at the last word of every Burst) are compared to generate, when not equal, the external DTREQ signal. This inequality is also used internally by the S2020 to automatically control the flow of Bursts in response to received READYs. Both counters are cleared to zero at Reset Mode or at the termination of the current {CONNECTED} state.

If the I-Field is to be sourced from a register separate from the FIFO, the NREN signal must be blocked to avoid erroneously advancing the FIFO.

Care must also be taken to control the FIFO in order to recognize the beginning of the Burst data if the PKTAV and SHBST are not used to delimit the data.

Once the Connection is established, the S2020 waits in the {IDLE} state until both BSTAV and DATAV input signals are asserted before starting any further data transfers. The BSTAV is used to initiate the search of the FIFO for the first word of the Burst and Packet. It should be noted that the BSTAV signal must be set high before the S2020 can attempt to read in the PKTAV signal.

Figure 0. S2020 50 MHz / RDCLK RESYNCH at MODE = 0 RESET (Corrected Version)



The S2020 sets the PACKET signal on the HIPPI Channel prior to setting the BURST signal as required by the HIPPI Standard. If the external DTREQ signal is low (Burst and Ready counters are equal), there are no "unanswered" READYs. In this case the S2020 will pause in the {PENDBST} state until a READY signal is detected and the Ready counter is incremented.

This function allows the Destination to "meter" the transmission of HIPPI Bursts on a one-by-one basis. A logic high on the DTREQ signal indicates that the S2020 is allowed to proceed, setting the BURST signal active and reading the next word of the Burst from the FIFO.

While this process when started proceeds automatically, the Host system can observe its progress via the DTREQ output.

The BSTAV should not be placed in the FIFO as a data bit, since it is used along with the DATAV signal to start and stop transmission gracefully at even Burst boundaries.

In all cases the BSTAV must be synchronized with the 25 MHz RDCLK for reliable operation of the S2020. The rising edge of BSTAV asynchronously controls the leading edge of the low active NREN signal.

Once the Connection is established and the first Packet and Burst are started, the S2020 Source Device will generate properly formatted Bursts with the appropriate LLRC word and inter-burst idle cycles as long as the FIFO has data and the PKTAV and BSTAV signals remain high. The BSTAV signal is used to pause at the even 256 word Burst boundaries while the Host System "refills" the FIFO.

The BSTAV signal must be set for at least the first word of the Burst. Once started the Burst will continue until 256 words are transmitted unless the SHBST signal is set active, the PKTAV signal is set inactive, or the DATAV signal is set low inactive. The word being read from the FIFO at the time that any one of these three events occurs becomes the last word of the Burst. The last word is transmitted, followed immediately by the LLRC for that Burst, and the S2020 pauses and waits for both the DATAV and BSTAV to be true (active high).

If the Burst was terminated due to an inactive PKTAV, the S2020 will wait for DATAV and BSTAV in the internal inter-packet {IDLE} state. Inter Burst pauses within a Packet cause the S2020 to wait in the {LLRC} state.

Each time a Burst reaches the last word condition, the Burst Counter is incremented and the previous value of the Burst Counter is saved in an internal Last Burst Register. In addition to the comparison between the Ready Counter and the Burst Counter used to control the FLOWON and DTREQ signals, a second comparison between the Ready Counter and the Last Burst Register is used to prevent the Ready Counter from being incremented to a value greater than the old Burst Count. Thus the Ready Counter is prevented from "wrapping around" after receiving more than 65,535 unanswered READY signals from the Destination.

The 65,536th and subsequent READY signals will be disregarded until at least one more Burst is completed, the Burst Counter incremented, the Last Burst Register updated, and the comparator conditions re-enable the incrementing of the Ready Counter.

If the Host decides to terminate the Packet while in the inter-Burst state, a single word must be loaded in the FIFO with the accompanying PKTAV bit set to 0. While the data at the inputs of the S2020 will appear at the HIPPI Channel outputs, the inactive BURST signal will cause the Destination to ignore that data. The low PKTAV read from the FIFO will again vector the S2020 to the inter-packet {IDLE} state.

After the last Packet of the transmission is completed, the Source Host may terminate the connection by placing a logic low on the CNREQ input. The S2020 will deassert the REQUEST signal on the HIPPI Channel, enter the {TERMCON} state and remain there until the Destination deasserts the CONNECT signal. At that point the {IDLE} state will be re-entered.

As an alternative, the Host may issue a Mode 0 Reset command to terminate the Connection. The REQUEST signal will similarly be deasserted and the {INIT} state will be entered until the Destination deasserts CONNECT and the Host System deasserts CNREQ. It is recommended that the first method be used for graceful termination since the path through the {TERMCON} state allows the Host to monitor the CONNECT signal status via the CNOUT output.

The HIPPI Source device connect control State Machine (SM) controls the Connection state of the HIPPI channel to which it is attached. The Connect Control SM has inputs from the Source Host and form the HIPPI channel (remote Destination). Based on the current set of inputs and the last state of this circuit, the next Connect state is entered and a related set of outputs is generated to the Source Host and to the HIPPI channel (remote Destination).

For this discussion all external device signal names shall be CAPITALIZED and underlined, the SM input 'alphabet' or decode names shall be in double quotes ("), and all internal state names shall be enclosed in curly brackets '{}'.

CONNECT SM EXTERNAL INPUTS

MSEL2-0 Mode SELect lines 2-0 from the Source Host. Although there are eight possible modes for the Source device selected by these signals, only modes 0 (RESET), 2 (WAIT), and 3 (OPERATIONAL) are part of this discussion.

CNREQ CoNnect REQuest signal from the Source Host. A '1' on this signal indicates the Source Host's request to either initiate a connection or maintain the current connection on the HIPPI channel.

A '0' on this signal indicates the Source Host's request to either terminate the current connection or maintain a disconnected state on the HIPPI channel.

DSIC Destination to Source InterConnect signal from the HIPPI channel. A '0' on this signal indicates the presence of a functioning Destination on the HIPPI channel. A '1' on this signal indicates the absence of a functioning Destination on the HIPPI channel.

CON CONnect signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

RDY ReaDY signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

NOTE: The input signals from the HIPPI channel go through a digital 'filter' in the Source device. This filter circuit resolves metastability (of the asynchronous signals) and filters out any signal state changes which are less than two cycles in duration.

CONNECT SM INTERNAL STATES

The defined states and brief descriptions of each state follow.

{INIT} The INITialization state is the state from which the rest of the functional connect states are entered. The main entrance to this state is when the inputs specify "RST", i.e., modes 0 or 2 with DSIC = 0 (active). The "RST" input indicates that the HIPPI Destination is present and that the Source Host is holding this device in a RESET or WAIT mode. It is intended that the Source Host enter the OPERATIONAL mode (3) when DSIC becomes active and when the Source Host is ready to enter the operational* states of this CONNECT SM (for HIPPI connections).

{IDLE} The IDLE state: This is the first operational state entered from {INIT} (above). The main entrance to this state is when this circuit is in the {INIT} state and the inputs specify "I". While in this state, both Source and Destination are ready and waiting for a connection to be established.

{REQ} The REQuest state is entered from the {IDLE} state when the Source Host initiates a HIPPI connection by asserting CNREQ. This state is exited when the Source Host drops CNREQ (abort) or when CON goes active, indicating a Destination response to the connect request.

{CON1} The CONnect1 state is entered from the {REQ} state for one cycle when CON first goes active, indicating a Destination response to the connect request. From this state, the request may be aborted, or the response will continue to be processed.

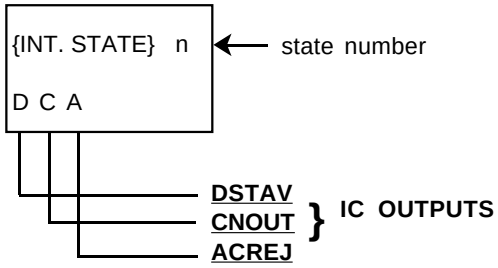
{CONn, 1<n<16} These 14 states differentiate between a CONNECT ACCEPT and a CONNECT REJECT response from the Destination. Being in one of these states implies that CON has been active (from the Destination) for 2 to 15 consecutive cycles. Receiving "CR" (inactive CON) in one of these states is a CONNECT REJECT. Receiving a "RDY" in one of these states indicates a CONNECT ACCEPT. Receiving "DR" in one of these states indicates that the Source Host wishes to abort the request.

{CON16} CONnect 16 state is entered for one cycle when the sixteenth consecutive cycle of an active CON from the Destination is received. Receiving "C" or "RDY" in this state constitutes a CONNECT ACCEPT. Receiving a "CR" in this state indicates a CONNECT REJECT response from the Destination. NOTE: The 'filter' circuit that the CON signal goes through effectively truncates the end of an active CONNECT signal, thereby allowing this state machine to wait 16 cycles (rather than 17) to determine if the Destination response is ACCEPT or REJECT. Receiving "DR" in this state indicates that the Source Host wishes to abort the connect requets operation.

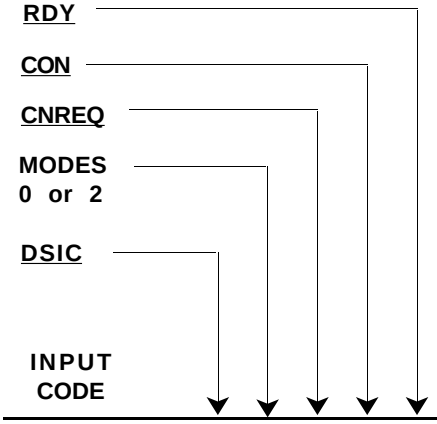
{CONNECTED} CONNECTED state is entered when a valid connection is established across the HIPPI channel between the Source and Destination. Receiving a "CR" in this state indicates an illegal termination, initiated by the Destination. Receiving a "DR" in this state results in a connection termination, initiated by the Source Host.

* The operational states of this CONNECT SM are all but {INIT}, {LOSTDEST}, and {NODEST}.

Figure 1. S2020 Connect SM Input Decode Alphabet

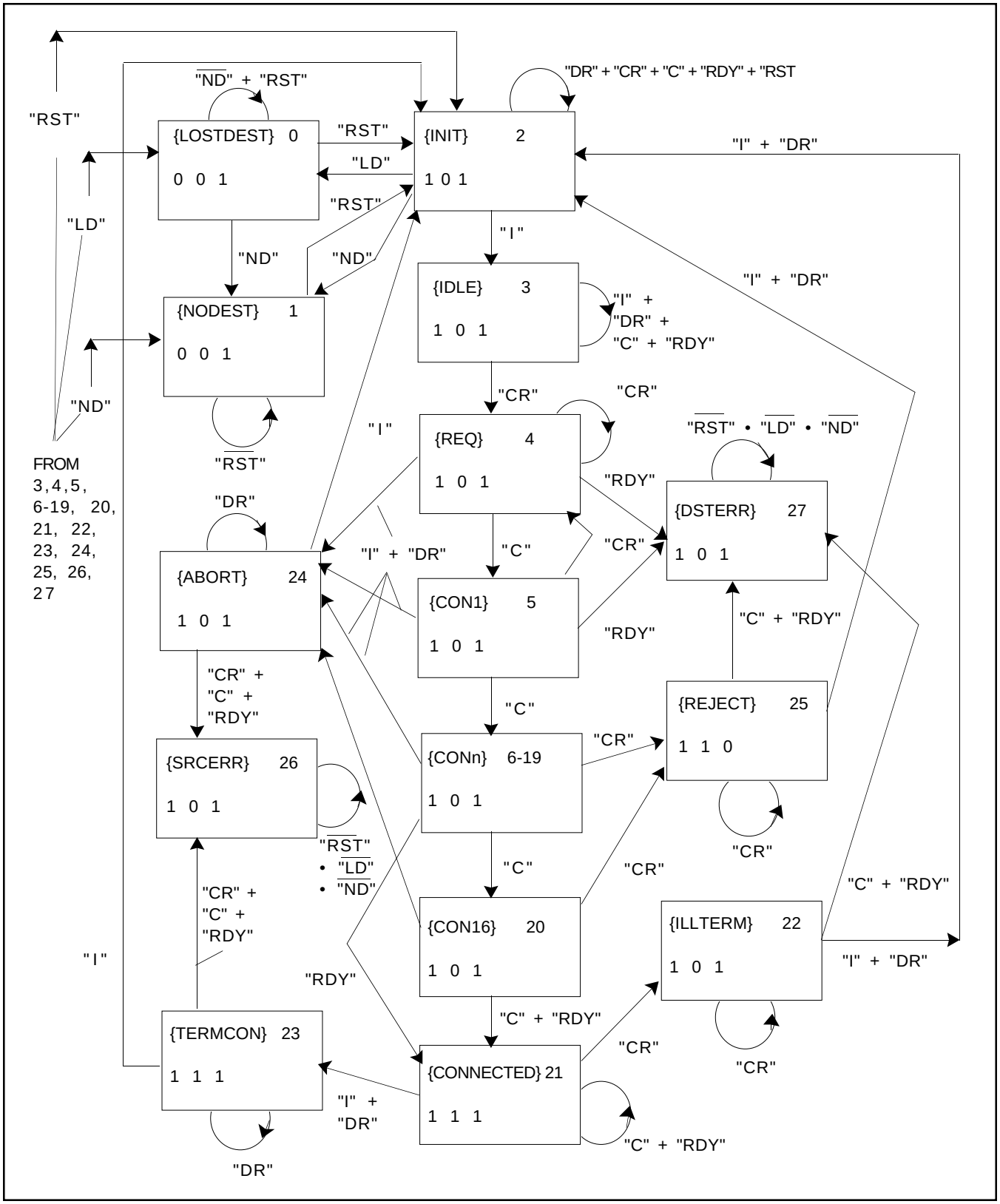


Key to S2020 Connect SM State Transition Diagram



INPUT CODE						DESCRIPTION
"I"	0	0	0	0	X	IDLE
"DR"	0	0	0	1	X	DISCONNECT REQUEST
"CR"	0	0	1	0	X	CONNECT REQUEST
"C"	0	0	1	1	0	CONNECTED
"RDY"	0	0	1	1	1	READY RECEIVED ReaDY
"RST"	0	1	X	X	X	NO DESTINATION ReSeT
"ND"	1	1	X	X	X	NO DESTINATION
"LD"	1	0	X	X	X	LOST DESTINATION

Figure 2. S2020 Connect SM State Transition Diagram



{ILLTERM} ILLegal TERMination state is entered when "CR" is received while in the {CONNECTED} state (i.e., the Destination drops CONNECT while a valid HIPPI connection exists). This state is exited when the Source Host drops CNREQ.

{TERMCON} TERMinate CONnection state is entered when "DR" is received while in the {CONNECTED} state (i.e., the Source Host drops CNREQ while a valid HIPPI connection exists). This circuit remains in this state until the Destination drops CONNECT.

{ABORT} The ABORT state is entered when "I" or "DR" are received while a connection is being requested (Source Host drops CNREQ before the HIPPI connection is established). This state is exited when the Destination drops CONNECT (if it was active).

{REJECT} The REJECT state is entered when the Destination's response to a connect request results in more than two (2) but less than 17 consecutive cycles of "C" (active CON). This state is exited when the Source Host drops CNREQ.

{LOSTDEST} The LOST DESTination state is non-operational, and is entered when the HIPPI Interconnect Destination-to-Source signal goes inactive during any of the operational states. This circuit remains in this state until the Source Host system forces a RESET or a WAIT mode (MSEL2-0 inputs).

{NODEST} The NO DESTination state is non-operational, and is entered anytime there is no Destination-to-Source Interconnect signal while the Source Host is forcing a RESET or WAIT mode via the MSEL2-0 inputs. This state is exited only by "RST" (the HIPPI Interconnect Destination-to-Source signal going active while still in the RESET or WAIT mode).

{SRCERR} The SouRCe ERRor state is entered when CNREQ goes active illegally. This is possible during the {ABORT} and {TERMCON} states, where this circuit is waiting for the channel to go idle after a Source initiated termination. While in this state, the Source device will report the error by asserting the SQERR output. The SeQuence ERRor will be further identified as a SouRCe ERRor by setting SRNDS to a '1'.

{DSTERR} The DeSTination ERRor state is entered when CON or RDY go active illegally; RDY should not be active during the {REQ} or {CON1} states, and neither CON or RDY should be active during the {ILLTERM} state. While in the {DSTERR} state, the Source device will report the error by asserting the SQERR output. The SeQuence ERRor will be further identified as a DeSTination ERRor by clearing SRNDS to a '0'.

CONNECT SM EXTERNAL OUTPUTS

In addition showing the state transitions resulting from external inputs to the Source chip, Figure 2 also shows the external output signals for each defined state.

DSTAV DeSTination AVailable signal to the Source Host. A '1' on this signal indicates the presence of a functioning Destination on the HIPPI channel. A '0' on this signal indicates the absence of a functioning Destination on the HIPPI channel.

CNOUT CoNnect OUT signal to the Source Host. This signal, along with the ACREJ signal (below), indicates the current connection state on the HIPPI Channel. During a Connect Request, a '1' on this signal indicates the receipt of a valid response to the Source (from the Destination) for the Connect Request. A '0' on this signal, during a Connect Request, indicates no response (yet) from the Destination.

After a connection is accepted, this signal shall be the same state as CONNECT on the HIPPI channel, and therefore will indicate to the Source Host an illegal termination (termination initiated by the Destination), or the acknowledgment by the Destination of a normal termination.

ACREJ ACcept/REJect signal to the Source Host. This signal, along with the CNOUT signal (above), indicates the Destination's response to the Source's Connect Request. A '1' on this signal when CNOUT goes active during a Connect Request indicates an ACCEPTed connection. A '0' on this signal when CNOUT goes active during a Connect Request indicates a REJECTed connection.

2.0 S2020 HIPPI DATA/FIFO CONTROL

The HIPPI Source device Host Data/FIFO State Machine (SM) is part of the Host Data/FIFO Control Block. The State Machine controls the flow of data and status from the Source Host FIFO to the S2020 Source device. The Data/FIFO SM also controls the generation of the HIPPI channel control signals to properly delimit the data and respond to the data transfer commands of the Source Host system.

The Host Data/FIFO SM has inputs from the Source Host system, the Connect Control State Machine and the internal Flow control circuit. Based on the current set of inputs and the last state of this state machine, the next Data/FIFO state is entered and a related set of outputs is generated to the Source Host and to the HIPPI channel.

As before, all external device signal names shall be CAPITALIZED and underlined, the SM input 'alphabet' or decode names shall be in double quotes ("), and all internal state names shall be enclosed in curly brackets '{}'. Signals internal to the Source device other than previously defined state names shall be in caret brackets '< >'.

HOST DATA/FIFO SM INPUTS

External Inputs

PKTAV PacKeT AVailable signal from the Source Host: Indicates the current delimiting of data across the HIPPI channel. A '1' on this signal indicates the Source Host's request to either initiate a Packet or maintain the current Packet on the HIPPI channel. A '0' on this signal indicates the Source Host's request to terminate the current Packet.

BSTAV BurST AVailable signal from the Source Host: Indicates the availability of other controls and data from the Source Host system. A '1' on this signal will enable the Source device to initiate a new read sequence from the Source Host FIFO. A '0' will disable the initiation of any new read sequences. This signal must not go active until at least one valid HIPPI Burst is available from the Source Host. If this signal goes inactive after a Burst read sequence has begun, the current burst will be completely read, but subsequent read operations will be disabled.

SHBST SHort BurST signal from the Source Host: Indicates the end of a HIPPI data Burst with a length shorter than 256 words. A '1' on this signal during an active Packet will terminate the current burst with the current word being the last word of the burst, and will initiate the completion and subsequent transmission of the LLRC word. A '0' on this signal will allow the Source device to transfer at least one more data word from the Source Host FIFO to the HIPPI channel unless the current word is the 256th word of the current Burst.

DATAV DATa AVailable signal from the Source Host: Indicates the availability of at least one more data word, or I-Field in the Source Host FIFO. A '1' on this signal will enable the Source device to advance any pending operation that requires more data from the Host. A '0' on this signal will prevent the advancement of any such operations, and will legally terminate the current data Burst being transferred across the HIPPI channel.

Internal Inputs

<FLOWON> Flow control signal from the READY/ BURST counter block: Indicates the current capacity of the HIPPI channel (Destination) to accept a HIPPI Burst. A '1' on this signal enables the transmission of one Burst to be initiated, if available from the Source Host system. A '0' on this signal allows the completion of any Burst that has been initiated, but disables any subsequent Bursts. The state of this signal is observable at the DTREQ (DaTa REQuest) output of the Source Device.

<CONREQ> Connect request signal from the Connect Control State Machine: This signal is active for any of the Connect SM states {REQ} thru {CON16} during a normal HIPPI channel Connection Request sequence. When active, this signal allows the Data/ FIFO SM to read the I-Field from the Source Host FIFO, and then present the I-Field data and the REQ signal to the HIPPI channel.

<CNNECTED> Connected signal from the Connect Control State Machine: This signal is active only for the {CONNECTED} state. A '1' on this signal enables all the HIPPI data delimiting and transfer functions. A '0' will disable all delimiting and transfer functions.

<256THWRD> The Terminal Count signal from the 8-bit word counter of the Host Data/FIFO Control Block: This signal indicates that the 256th word of the current Burst is being transferred from the FIFO to the Source device. A '1' on this signal will legally terminate the current Burst. A '0' will allow the Source device to transfer at least one more data word.

<RESET> The Reset signal from the Clock Control Block: This signal is the registered decode of the MSEL2-1 for the Mode = 0 state. A '1' on this signal indicates the Reset state for the entire Source device including the Host Data/FIFO SM. A '0' on this signal will enable all other inputs to the SM.

HOST DATA/FIFO SM INTERNAL STATES

The defined states are as follows:

{INIT} The INITialization state is the entry point of the Host Data/FIFO SM. This state is unconditionally entered by a "RST" decode of the inputs. The state is also entered by a "DSCN" decode representing the disconnected state of the HIPPI channel. This state remains active if a "CNRQ" decode is true while the "NODT" decode remains false, indicating a Connection request without Data available from the FIFO. The state is exited to the {RDIFL} state by the decode of "CNRQ" and "DTAV" both true. The decode of "CON" in this state is a Destination error and the {DESTERR} state is entered.

{RDIFL} The ReaD I-FieLd state is entered when a Connect request is is initiated by the Source Host system and there is data available from the Source Host. When in this state the FIFO read function is active resulting in an active low level on the NREN output. The read operations of the FIFO will continue until the "IFLD" decode is true, at which point the {PSTIFLD} state is entered. The decode of "RST" or "DSCN" will exit this state back to the {INIT}. The decode of "CON" in this state will force entry to the {DESTERR} state.

{PSTIFLD} The PoST I-FieLd state is entered when an I-Field is successfully read from the Source Host system. While in this state, the I-Field data is presented to the HIPPI channel and the REQ signal is asserted on the HIPPI channel. Although the NREN signal remains inactive, the internal data and parity pipeline remains active. If the I-Field was presented from the FIFO, the FIFO output register is stable with that data. If the FIFO data outputs were disabled, any other data applied to the Source device inputs (ie. via 3-state multiplexing) would appear at the HIPPI channel outputs two 25MHz clock cycles later. The decode of "DSCN" or "RST" will force entry to {INIT}. The decode of "CON" indicates successful connection to the HIPPI channel, and the {IDLE} state will be entered.

{IDLE} The IDLE state is maintained when there is a Connection established, but there is no Packet and no data to transmit. No read operations are performed on the FIFO in this state. When "DRDY" indicates that Data and Burst are available, the {WAITPKT} state is entered.

{WAITPKT} The WAIT PacKeT state is entered when there is no active Packet and the decode of "DRDY" is true, indicating that both BSTAV and DATAV were asserted from the Source Host system.

This state will read one word from the Source Host FIFO. If the "NPIF" decode is detected at the read (ie. PKTAV not asserted) then the {IDLE} state is entered. This loop of {IDLE}-{WAITPKT} will advance the FIFO up to the next valid Packet.

Any data words not delimited by PKTAV will appear at the HIPPI channel, but the PKT and BST signals on the HIPPI channel remain inactive. If the PKTAV is asserted at the read, the {PENDBST} state is entered.

{PENDBST} The PENDing BurST state is entered when the Source Host system has a Burst of data to send. No read operations are performed in this state. If the "FLOF" decode is true (indicating that the Destination is not Ready for a Burst), this state is maintained. When the "FLOF" decode is false then this state is exited. If the PKTAV signal is deasserted, the {SRCERR} state is entered. If the pending Burst has only one word either by the assertion of SHBST in the first word or by the deassertion of DATAV (the last word in the FIFO was read), then the {LSTWD} state is entered. If the Burst has more than one word, then the {BURST} state is entered.

{BURST} The BURST state is entered when everything is prepared for transmission; a valid connection is established on the HIPPI channel, the Source Host system has at least one Burst available, a Packet is currently active, and the Destination is capable of receiving at least one complete Burst. In this state, Source Host system read operations are performed continuously until the the Packet is terminated, the 256th word is read, the SHBST signal is asserted, or the Source Host FIFO runs out of data. When any of these terminating conditions occur, the {LSTWD} state is entered.

{LSTWD} The LaST WorD state is entered when the last word of the current Burst has been read from the Source Host system. No read operations are performed in this state. This state is only one cycle in duration, and except for error conditions, the {LLRC} state is next.

{LLRC} The LLRC state is entered after the {LSTWD} state. This state will deassert the BST signal on the HIPPI channel while completing and posting the LLRC word to the channel. If the current Packet has been terminated by the Source Host system (PKTAV was deasserted at the read of the last word of the Burst), then the {IDLE} state will be entered. If the "DRDY" decode is true (BSTAV and DATAV are both asserted), and the current Packet is to be continued, then the {WTBST} state is entered. If the current Packet is to be continued, but the "DRDY" decode is false, then this state is maintained. No read operations are performed in this state.

{WTBST} The WaiT BurST state is entered after one Burst is complete and the "DRDY" decode is true. One read operation is performed in this state. If PKTAV is asserted at that read operation, then the {PENDBST} state is entered. If PKTAV was deasserted at the read, then the {IDLE} state is entered.

{SRCERR} The SouRCe ERRor state is entered if the PKTAV changes from a "1" to a "0" and the "FLOF" decode is false during the {PNDBST} state.

This state is exited to the {INIT} state when the HIPPI Connection is broken or if the <RESET> signal is true. The state is exited to the {DSTERR} state if the "CNRQ" decode is true. This error state is reported to the Source Host system by setting both SQERR and SRNDS output to logical "1".

{DSTERR} The DeSTination ERRor state is entered if the <CONREQ> signal is received while a valid HIPPI Connection is already established. The most likely cause of this error is an unstable signal on the HIPPI channel from the Destination. This state is also entered if CON is asserted when not expected (during the {INIT} or {RDIFL} states). This state is exited by either the "RST" or "DSCN" decodes being true, either of which force the {INIT} state. This error state is reported to the Source Host system by setting the SQERR output to "1" and the SRNDS output to "0".

DATA/FIFO SM EXTERNAL OUTPUTS

REQ REQuest signal to the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

BRST BuRST signal to the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

PKT PacKeT signal to the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

NREN Not Read ENable signal to the Source Host system FIFO. This is an active low signal to be used to enable the FIFO to load a new data word into its output register. This signal is controlled not only by the state of the Data/FIFO SM, but also by the inputs PKTAV, SHBST, DATAV and BSTAV.

As an example, in the {RDIFL} state, the detection of the "IFLD" decode (PKTAV ='0', SHBST = '1') will asynchronously deassert (raise to logical '1') the NREN signal prior to the next rising edge of RDCLK such that the tagged data remains held in the FIFO's output buffer. Similarly, the "DRDY" decode asynchronously controls the assertion of NREN on the transition from the trapped {IDLE} state to the {WAITPKT} state.

Figure 3. Data/FIFO SM Input Decode Alphabet

		<RESET>	<CONREQ>	<CNNECTED>	PKTAV	SHBST	<256THWORD>	DATAV	BSTAV	<FLOWON>	INPUT DESCRIPTION
0	"FLOF"	X	X	X	X	X	X	X	X	0	FLOW OFF
1	"NODT"	X	X	X	X	X	X	0	X	X	NO DATA
2	"DRDY"	X	X	X	X	X	X	1	1	X	DATA READY
3	"DTAV"	X	X	X	X	X	X	1	0	X	DATA AVAILABLE
4	"256W"	X	X	X	X	X	1	X	X	X	256th WORD
5	"SBST"	X	X	X	1	1	X	X	X	X	SHORT BURST
6	"IFLD"	X	X	X	0	1	X	X	X	X	I-FIELD
7	"PKT"	X	X	X	1	0	X	X	X	X	PACKET
8	"NPKT"	X	X	X	0	0	X	X	X	X	NO PACKET
9	"NPIF"	X	X	X	0	X	X	X	X	X	NO PACKET OR I-FIELD
10	"CON"	0	0	1	X	X	X	X	X	X	CONNECTED
11	"CNRQ"	0	1	X	X	X	X	X	X	X	CONNECT REQUEST
12	"DSCN"	0	0	0	X	X	X	X	X	X	DISCONNECTED
13	"RST"	1	X	X	X	X	X	X	X	X	RESET

Figure 4. S2020 Data/FIFO Interface SM State Transition Diagram

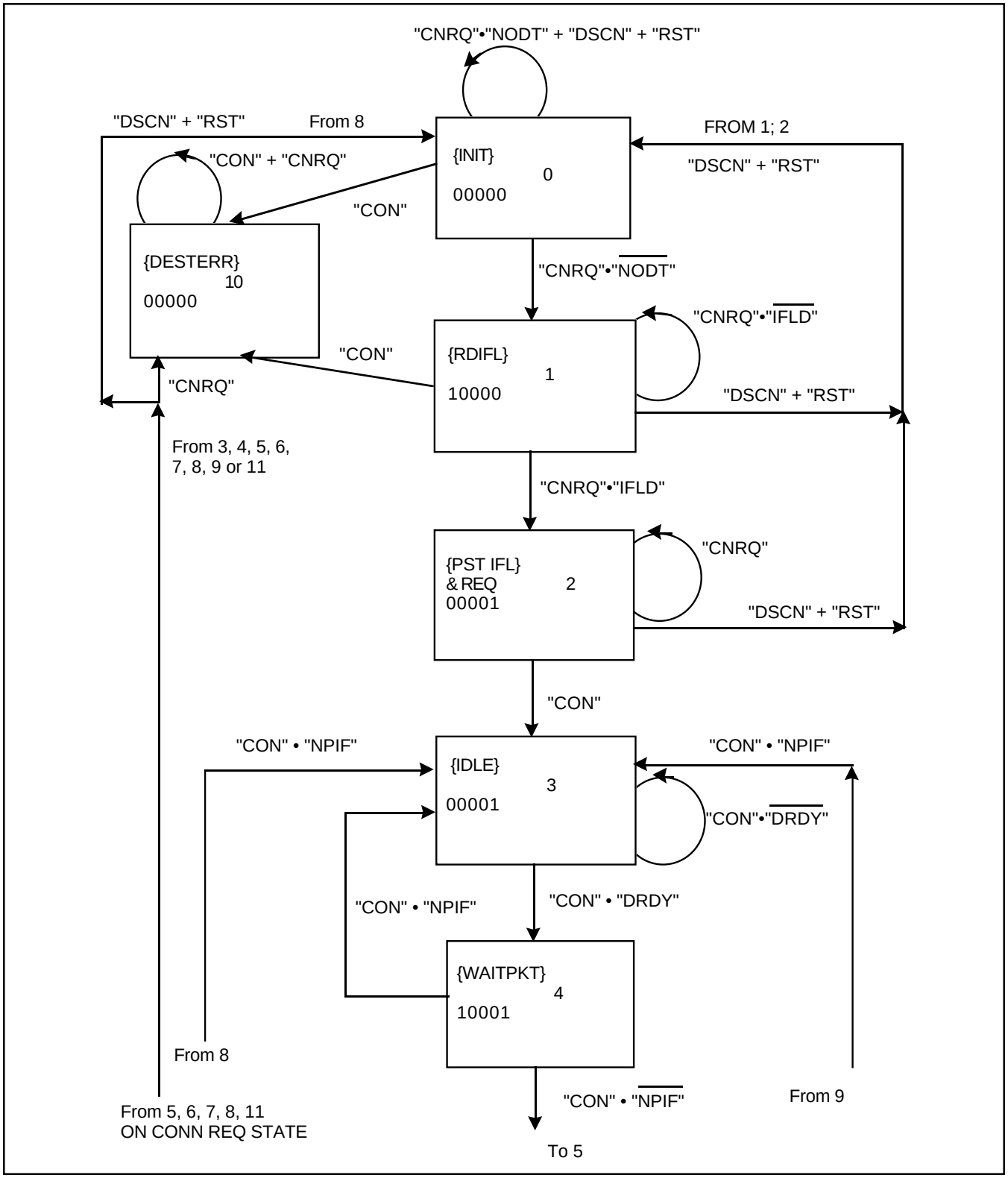
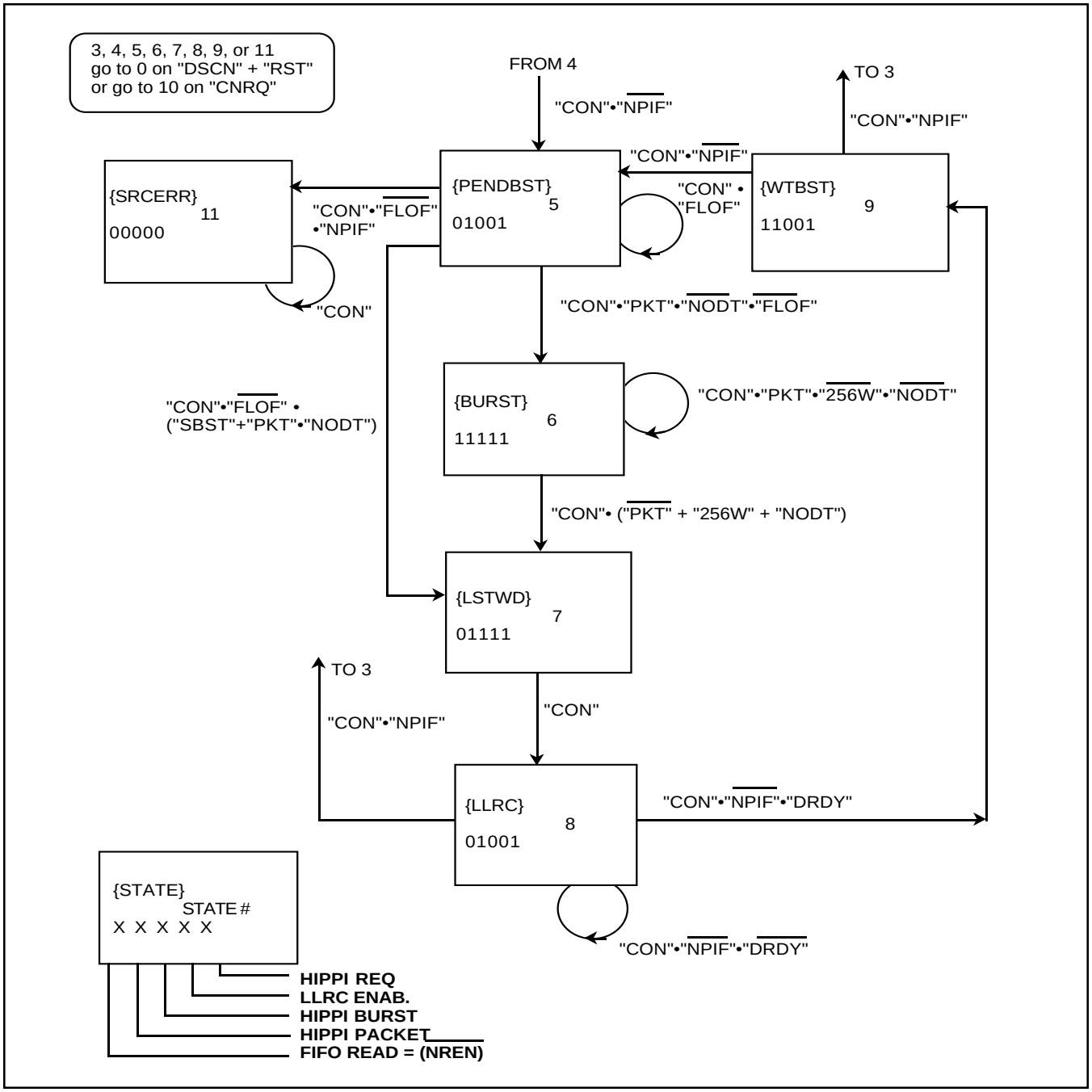


Figure 4. S2020 Data/FIFO Interface SM State Transition Diagram (continued)



S2021 HIPPI DESTINATION CONNECT CONTROL

S2021 HIPPI Destination Device Normal Functional Sequence

The S2021 Destination Device responds to Connection and data transfer requests received from the HIPPI Source.

The RESET Command (Mode 0) initializes all internal registers and state machines of the S2021. The Reset Command also places all Host side TTL outputs in the high-impedance state and the HIPPI Channel outputs (CONNECT and READY) in the deasserted state. The Destination to Source Interconnect output (DSIC) is also placed in the high logic low state. If the circuit recommended on page 19 of the S2020/S2021 Device Specification is used, this will result in a high inactive level on the HIPPI Channel DSIC signal.

After the RESET Command initialization is complete the Device should be placed in the operational state through the Mode 5 Command. The Host system should place a logic low signal on the CONIN input. The SRCAV output should then be monitored to determine the status of the Source Driving the HIPPI Channel.

If this signal is at a logic 0, either the Source to Destination Interconnect (SDIC) is inactive or one of the Channel Control signals (REQUEST, PACKET or BURST) from the Source is active. A logic 1 on the SRCAV output indicates the presence of a functional Source capable of initiating data transfers.

In the initialized but not connected condition, the S2021 cycles through the {DISCON0-2} state sequence. This is monitored by the host system by observing the 5,6,7 repeating sequence on the SELB(2:0) outputs and the appropriate internal status words on the data outputs.

At this point the Host system may initialize the internal Buffer Counter of the S2021 with the number of Burst-sized (256 word) buffer blocks available in the external FIFO and memory system. This is accomplished by placing a rising edge signal on the RDYIN input for each buffer block to be counted. Thus, if the available FIFO is 4K words deep, and the process that empties the FIFO is slower than the data rate of the HIPPI Channel, 16 pulses would be supplied to the RDYIN input.

During the disconnected condition, the state of the Buffer counter can be monitored by observing its contents in the lower half of the Flow status Word 2 which is presented to the outputs during the SELB=7 state. The Buffer Counter has a capacity of 2exp16 - 1 counts (65,535 buffers). Inputs to RDYIN greater than this will be ignored.

If the process that empties the FIFO is faster than the data rate of the HIPPI Channel, the RDYIN input may be driven by a free-running TTL signal at a frequency less than or equal to 12.5 MHz. In that configuration the Buffer counter will quickly fill to 65,535.

After a connection is accepted, the READY signals are continuously generated at the maximum rate allowed by the HIPPI Standard (160 ns asserted, 160 ns deasserted) and counted in the internal READY Counter until the two counters are equal. If a continuous toggling signal is applied to RDYIN, 65,535 READY pulses will be sent at the maximum rate. From that point on each received Burst will allow one and only one READY pulse to be generated.

When an active REQUEST is detected on the HIPPI Channel the {REQCON} state and the {IFIELD} state are entered. The data on the HIPPI Channel is presented at the outputs of the S2021 along with a logic high on the CONRQ output.

The SELB outputs assume the 001 code for the HIPPI I-Field. At this point the Host system must decide to either accept or reject the connection. The Host system must place a logic high on the CONIN input while holding the ACCRJ at logic high to accept the connection. If ACCRJ is held low when CONIN is asserted the connection will be rejected. For applications where all REQUESTs must be accepted, the CONRQ output may be connected directly to the CONIN input and the ACCRJ input held high.

If the REQUEST is rejected (CONIN =1, ACCRJ =0) the S2021 will assert the CONNECT signal on the HIPPI Channel for four clock cycles and then deassert the CONNECT signal for four cycles. If at the end of this sequence the Source has deasseted the REQUEST signal the S2021 will return to either the {IDLDSAB} state (CONIN=1) or the {IDLENAB} state (CONIN=0). When the {IDLENAB} state is reached the S2021 is able to process another Connection Request from the Source.

If the Host system has accepted the connection request (CONIN=1, ACCRJ=1) the S2021 will return to the {DISCON0-2} sequence until the CONNECT signal has been asserted for four clock cycles. At that point the S2021 enters the {IDLE} state (SELB=3) and remains there until the Source asserts the PACKET signal on the HIPPI Channel.

When the PACKET signal is detected from the Channel, the S2021 responds by placing a logic 1 on the PKOUT output and waits for a Burst data transfer to begin. The SELB bus remains in state 3. If the Source drops the PACKET on the Channel without beginning a Burst, i.e. attempts to form an “empty” Packet, the S2021 will detect a Sequence Error.

The detected Sequence Error will force the CONNECT to deassert, issue one Sequence Error word on the data outputs (SELB=4), and then return to the {DISCON0-2} sequence with its accompanying SELB5,6,7 sequence.

In the normal data transfer procedure, the Source will follow the asserted PACKET by asserting the BURST signal at least one clock cycle later. If the BURST is asserted at the same time as or before PACKET, the Sequence Error process described above will occur.

A legally asserted and detected Burst will cause the S2021 to place a logic 1 on the BROUT output, place the SELB bus to state 0, and place the received data and parity bits on the data and parity outputs as the first word of the Burst.

The S2021 will continue to place received data and parity on the outputs (with SELB=0) until the Source deasserts the BURST signal. The S2021 makes no distinction between short Bursts (less than 256 words), normal Bursts (exactly 256 words), or "extended" Bursts (greater than 256 words). As long as the Source provides an LLRC word calculated with a modulo 256 word count in accordance with the HIPPI Specification, the S2021 will process the Burst without error.

The Burst is ended when the S2021 detects that the Source has deasserted the BURST signal on the HIPPI Channel. The data and parity word received with the deasserted BURST are placed on the outputs as the LLRC word (SELB=2). The received LLRC word is compared with the LLRC internally calculated and any mismatch will set the RLLER output to logic 1 at the next clock cycle.

As each Burst is completed, the internal Burst Counter is incremented by one as described above. During the inter-Burst idle time the SELB bus is placed in state 3 and the general operational status word appears on the data outputs. That status word allows the comparison flags for the Flow Control circuit to be observed.

The ALLBSTS flag is 1 when the READY and BURST counters are equal. The 64KBFRS flag is 1 when the Last Burst and Buffer counters are equal. The ALLRDYS flag is one when the READY and Buffer counters are equal.

The S2021 will continue to process received Bursts until the Source deasserts the PACKET signal. The inter-Packet condition will also result in the general operational status word appearing at the outputs (with SELB=3).

At this point the Source may elect to start another Packet or end the Connection by deasserting the REQUEST signal. It should be noted that the Source may deassert the REQUEST signal at the same time as it deasserts the PACKET signal. In either case the S2021 returns to the SELB5,6,7 sequence (internal states {DISCON0-2}).

The value in the BURST Counter is loaded into the READY Counter, since the previous difference between these two counters represents the READYs that were "lost" or unanswered by the now disconnected Source.

Unless the Destination Host System resets the flow counters (NRRDY set to logic 0) or resets the S2021 (Mode 0 Reset) The available Buffer count is preserved for the next Connection.

The HIPPI Destination device Connect Control State Machine (SM) controls the Connection state of the HIPPI channel to which it it is attached. The Connect Control SM has inputs from the Destination Host and from the HIPPI channel (remote Source). Based on the current set of inputs and the last state of this circuit the next Connect state is entered and a related set of outputs is generated to the Destination Host and to the HIPPI channel (remote Source).

For this discussion, all external device signal names shall be CAPITALIZED and underlined, the SM input 'alphabet' or decode names shall be in double quotes (") and all internal state names shall be

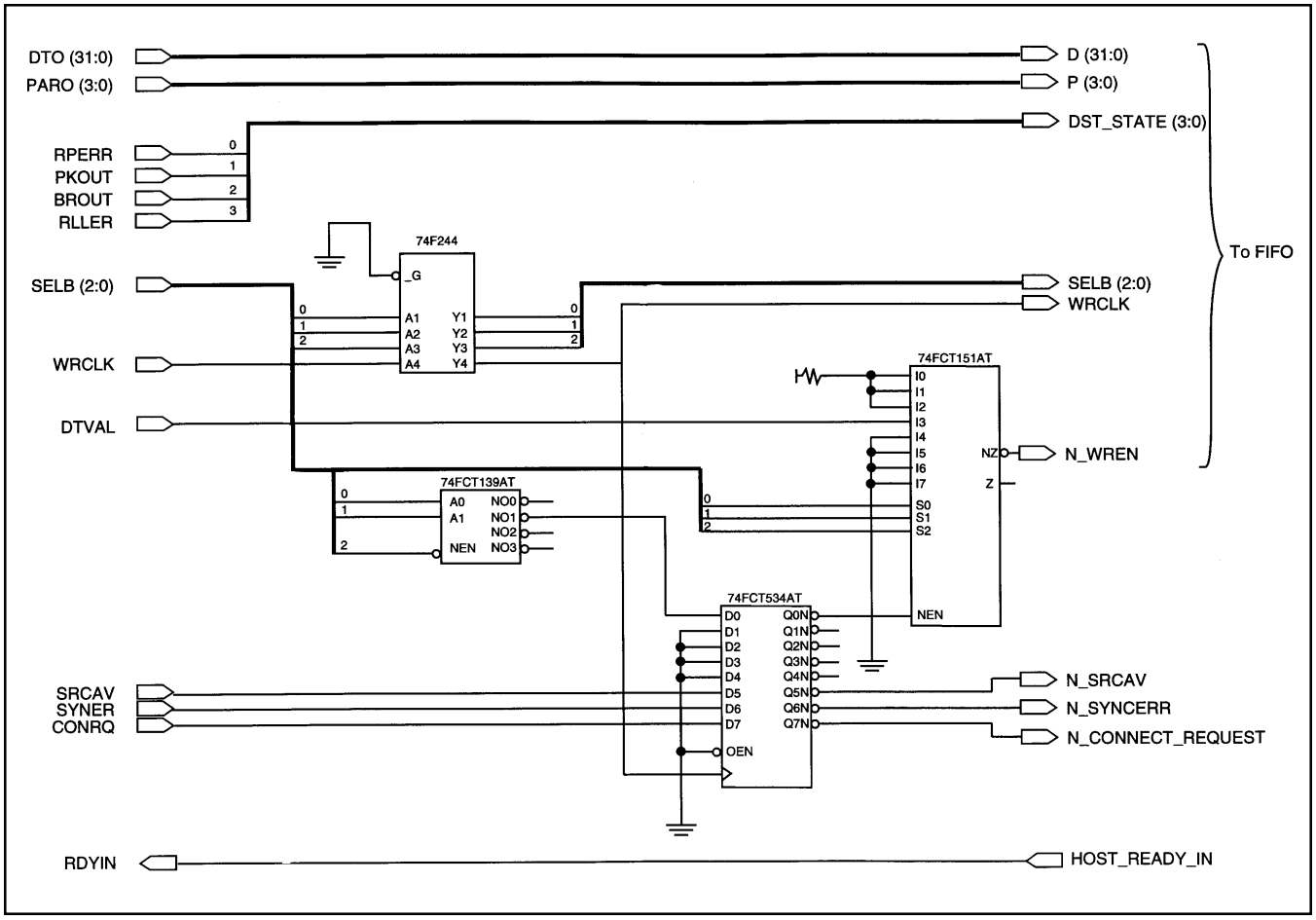
enclosed in curley brackets '{}'. Signals internal to the Destination device other than previously defined state names shall be in caret brackets '< >'.

CONNECT STATE MACHINE EXTERNAL INPUTS

MSEL2-0 Mode SELect lines 2 - 0 from the Destination Host system. Although there are eight possible modes for the Destination device selected by these signals, only modes 0 (RESET) and 5(OPERATIONAL) are part of this discussion.

SDIC Source to Destination InterConnect signal. A '0' on this signal indicates the presence of a functioning Source on the HIPPI channel. A '1' on this signal indicates the absence of a functioning Source on the HIPPI channel. This signal is debounced and inverted to form <NRAWSDIC> (active high). A '1' on this input (or '0' on the <NRAWSDIC> signal) is sufficient to force the internal "DSBL" decode independent of other inputs.

Figure 4B. S2021 Destination FIFO Interface



REQ REQuest signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec. When debounced and synchronized as <SYNCREQ> this signal is used in the input 'alphabet' decoder for the Connect Control SM.

CONIN CONnect IN signal from the Destination Host system. This signal when asserted during a Connection Request cycle, indicates an active response to the Request by the Destination Host system.

If this signal is asserted prior to the detection of a Connection Request cycle, the "IDSB" decode inhibits response to Requests from the HIPPI channel.

If this signal remains low after an asserted REQ from the HIPPI channel, the channel remains 'hung' in the Connection Request state until the Remote Source exercises a time-out of the unanswered request. The CONIN signal may be tied directly to the CONRQ output, and the ACCRJ used as the active Connection control by the Destination Host system.

ACCRJ ACCept/not ReJect signal from the Destination Host system. This signal together with the CONIN signal described above, control the Destination device's response to a Connection Request (asserted REQ) from the HIPPI channel remote Source. If a '1' is placed on this input, the accompanying active CONIN is considered as an acceptance response to the Connection Request. If a '0' is placed on this input, the asserted CONIN will result in an active Rejection of the Connection Request (the CON signal to the HIPPI channel will be asserted for four clock cycles only, then deasserted). The active Rejection avoids possible 'hung' conditions on the HIPPI channel.

CONNECT STATE MACHINE INTERNAL INPUTS

<RSTCON> ReSeT CONnection signal from the internal Data/FIFO Control SM. This signal is asserted during error states of the DATA/FIFO SM. When asserted, this signal is sufficient to force the internal "DSBL" decode independent of other inputs.

CONNECT SM INTERNAL STATES

{DISABLED} The DISABLED state of the Connect SM is forced by the decode of "DSBL" from the input 'alphabet'. "DSBL" will force this state from all other states of the Connect SM. While in this state the SRCAV output is held to '0'. This state is exited to the {IDLDSAB} state if the "IDSB" decode is true (CONIN asserted with no REQ active). The {IDLENAB} state will be entered if the "IENB" decode is true.

{IDLDSAB} THE IDLe DiSABled state is entered from the {DISABLED} state, the {IDLENAB} state, and from the {REJCOMPL} state when the "IDSB" decode is true. This state will persist until the "IDSB" decode is false. The normal exit from this state is to the {IDLENAB} state if the "IENB" decode is true. The "DSBL" decode will force exit to the {DISABLED} state. Any other decode forces the {HANGERR} state.

{IDLENAB} The IDLe ENABled state is entered from the {DISABLED} state, the {IDLENAB} state, and from the {REJCOMPL} state when the "IENB" decode is true. This state will persist until the "IENB" decode is false. This state is exited to the {REQCON} state if the "RQCN" decode is true, the {ACC0} state if the "CNAC" decode is true, the {REJ0} state if the "CNRJ" decode is true, and the {IDLDSAB} state if the "IDSB" decode is true.

{REQCON} The REQuest CONnection state is entered from the {IDLENAB} state at the detection of an asserted REQ from the HIPPI channel while CONIN is deasserted ("RQCN" decode is true). This state will persist while "RQCN" remains true. If the REQ is deasserted, this state is exited to the {IDLENAB} state. This state is exited to the {ACC0} state if the "CNAC" decode is true, the {REJ0} state if the "CNRJ" decode is true, the {IDLENAB} state if the "IENB" decode is true and the {IDLDSAB} state if the "IDSB" decode is true.

{ACC0-3} The ACCept 0 through ACCept 3 states are entered at {ACC0} from either {IDLENAB} or {REQCON} when the "CNAC" decode is true. These states are then sequenced in order unless overridden by a "DSBL" decode. The CON signal is asserted on the HIPPI channel for these states. This sequence is exited to the {CONNECTED} state if the "DSBL" decode remains false.

{CONNECTED} The CONNECTED state is entered when a valid Connection is established across the HIPPI channel between the Destination and the Source. This state enables the output of the RDY signals on the HIPPI channel to initiate the transfer of Burst data from the remote Source. This state will persist while either the "CNAC" or the "CNRJ" decodes are true and the "DSBL" decode remains false. The CON signal on the HIPPI channel remains asserted while in this state. This state is exited to the {REJCOMPL} state if the "RQCN" decode is true, the {DISCON0} state if the "IENB" decode is true, and the {INCOMPDCON} state if the "IDSB" decode is true.

Figure 5. S2021 Connect SM Input Decode Alphabet

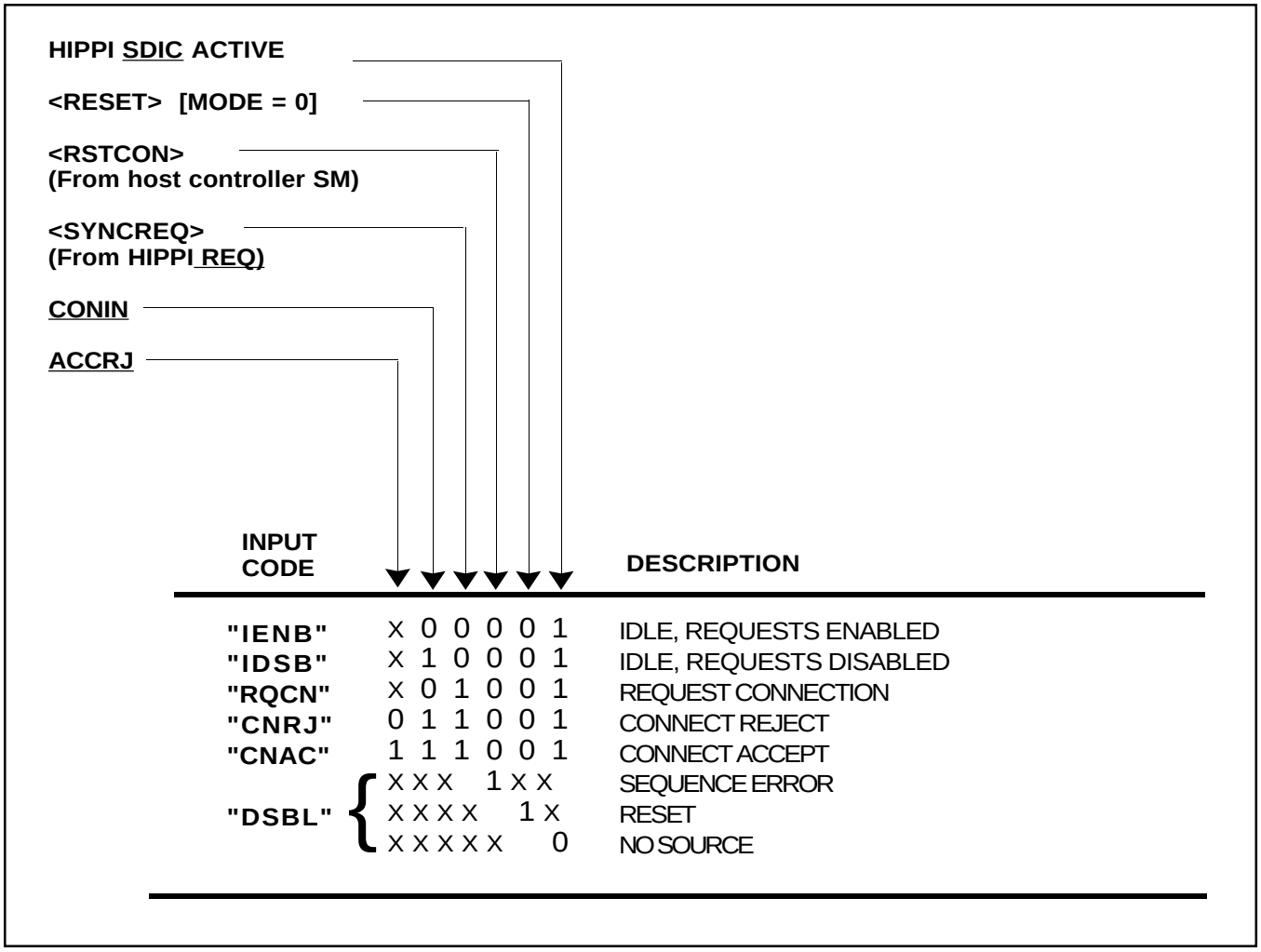


Figure 6. S2021 Connect SM State Transition Diagram

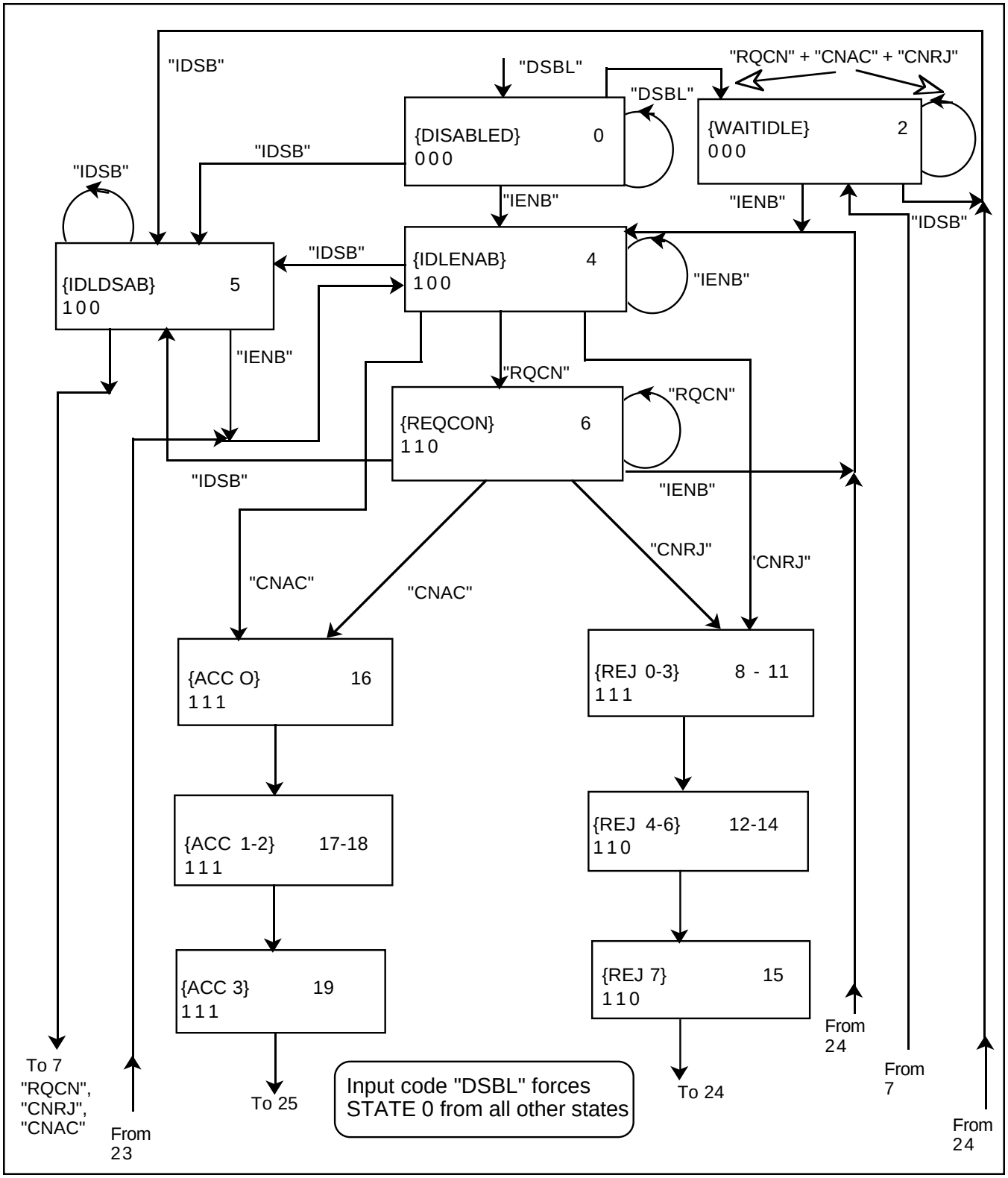
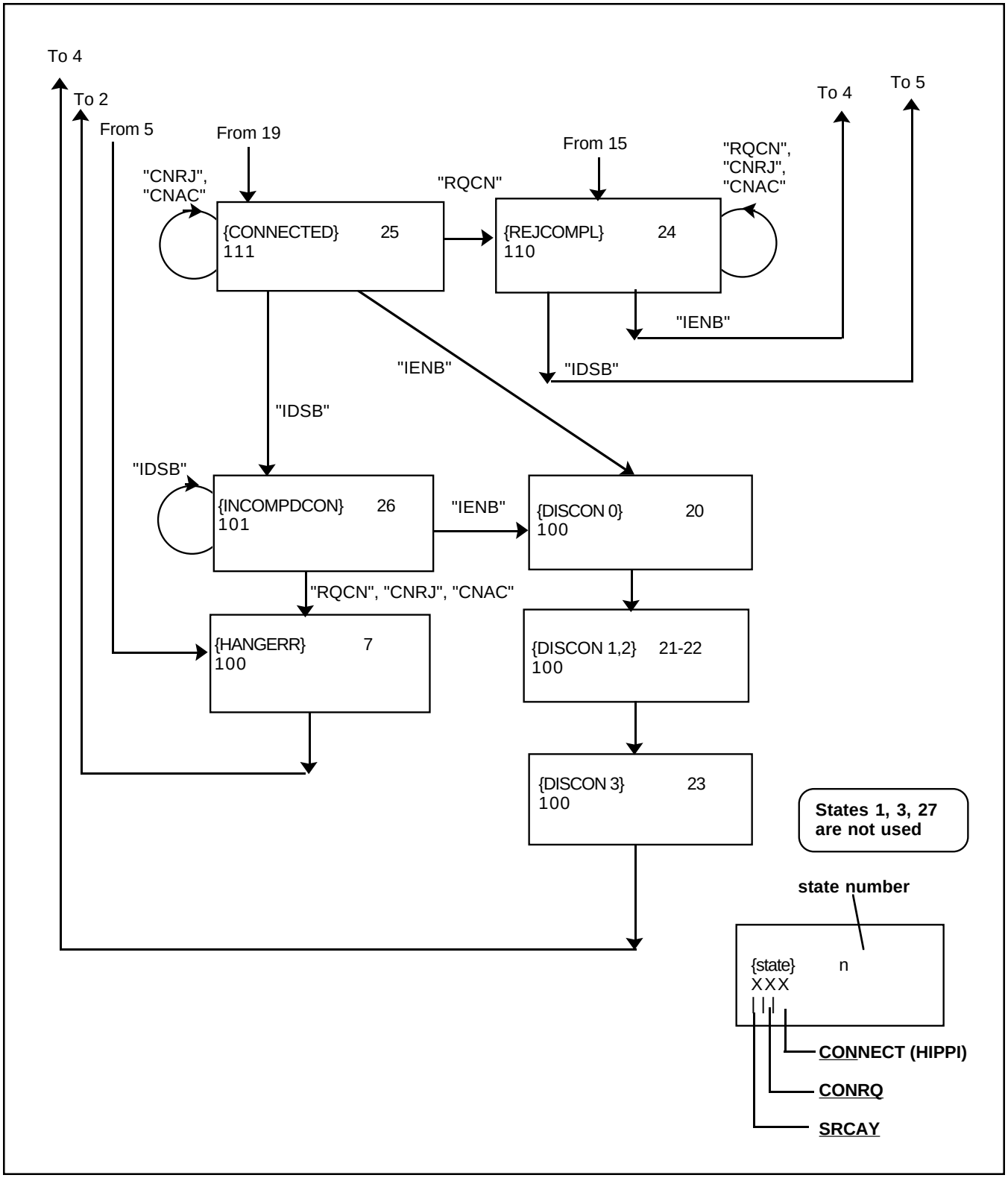


Figure 6. S2021 Connect SM State Transition Diagram (continued)



{REJ0-3} The REJect 0 through REJect 3 states are entered at {REJ0} from either {IDLENAB} or {REQCON} when the "CNRJ" decode is true. These states are sequenced in order unless overridden by a "DSBL" decode. The CON signal is asserted on the HIPPI channel for these states, providing the minimum four clock cycle response for an active Connection Reject. This sequence is exited to the {REJ4} state if "DSBL" remains false.

{REJ4-7} The REJect 4 through REJect 7 states are entered at {REJ4} from {REJ3}. These states are sequenced in order unless overridden by a "DSBL" decode. The CON signal is deasserted for these states, defining the active Connection Reject. This sequence is exited to the {REJCOMPL} state if "DSBL" remains false.

{REJCOMPL} The REJect COMPLete state is entered from the {REJ7} state if "DSBL" decode is false, or from the {CONNECTED} state if the "RQCN" decode is true. This state persists while "RQCN". "CNRJ" or "CNAC" are true. This state is exited to the {IDLENAB} state if the "IENB" decode is true, or to the {IDLDSAB} state if the "IDSB" decode is true.

{DISCON0-3} The DISCONnect 0 through DISCONnect 3 states are entered in sequence from the {CONNECTED} state or from the {INCOMPDCON} state when the "IENB" decode is true. These states are sequenced in order unless overridden by a "DSBL" decode.

The function of this sequence is to assure that at least four clock cycles of deasserted CON on the HIPPI channel to recognize the Disconnected condition of the channel. This sequence is exited to the {IDLENAB} state if the "IENB" decode is true.

{INCOMPDCON} The INCOMPlete DisCONnect state is entered from the {CONNECTED} state if the "IDSB" decode is true (REQ on the HIPPI channel is deasserted, but CONIN remains asserted). This state persists if the "IDSB" decoode remains true. This state is exited to the {DISCON0} state if the "IENB" decode is true, or to the {HANGERR} state if either the "RQCN", "CNAC" or "CNRJ" decodes are true.

{HANGERR} The HANG ERRor state is entered from from either the {IDLDSAB} or {INCOMPDCON} states if either the "RQCN", "CNAC" or "CNRJ" decodes are true. These decodes represent erroneous sequences of the Host or channel control signals. This state is exited after one clock cycle to the {WAITIDLE} state.

{WAITIDLE} The WAIT IDLE state is entered from the {HANGERR} state if the "DSBL" decode remains false. This state persists if either the "RQCN", "CNAC" or "CNRJ" decodes are true. This state is exited to the {IDLENAB} state if the "IENB" decode is true.

3.4 CONNECT SM EXTERNAL OUTPUTS

SRCAV SouRCe AVailable signal to the Destination Host sytem. A "1" on this signal indicates that the HIPPI channel, from the remote Source through the local Destination device is available.

A "0" on this signal indicates that either the SDIC is inactive, the Destination device is in a Reset or test mode, or that the Data/FIFO SM is in an Error state.

CONRQ CONNect ReQuest signal to the Destination Host system. A "1" on this signal indicates that the REQ signal from the HIPPI channel has been asserted and recognized by the Destination device. A "0" on this signal occurs when the REQ signal is deasserted.

This signal when active indicates the time during which the CONIN input may be used to actively accept or reject a Connection Request.

CON CONnect signal to the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

4.0 S2021 HIPPI DATA/FIFO CONTROL

The HIPPI Destination device Host Data/FIFO State Machine' (SM) is part of the Host Data/FIFO Control Block'. The State Machine controls the flow of data and status from the HIPPI channel, through the S2021 Destination device to the Destination Host FIFO and the associated status registers.

The Data/FIFO SM also provides addressing control to vector data and status words to their appropriate registers.

The Host Data/FIFO SM has inputs from the HIPPI channel and the Connect Control SM. Based on the current set of inputs and the last state of this state machine, the next Data/FIFO state is entered and a related set of outputs is generated to the Destination Host system.

As before, all external device signal names shall be CAPITALIZED and underlined, the SM input 'alphabet' or decode names shall be in double quotes ("), and all internal state names shall be enclosed in curly brackets '{}'. Signals internal to the Source device other than previously defined state names shall be in caret brackets '< >'.

HOST DATA/FIFO SM INPUTS

EXTERNAL INPUTS

BRST BuRST signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

PKT PacKeT signal from the HIPPI channel. The functions of this signal are defined in the HIPPI-PH spec.

4.1.2 INTERNAL INPUTS

<NXTST6> State 6 signal from the Connect Control SM: This signal is active when the Connect Control SM is in the {REQCON} state. This signal indicates the reception of an I-Field' from the HIPPI channel.

<NXTST25> State 25 signal from the Connect Control SM: This signal is active when the Connect Control SM is in the {CONNECTED} state. This signal allows the Data/FIFO SM to process Packet and Burst delimited data from the HIPPI channel.

4.2 HOST DATA/FIFO SM INTERNAL STATES

The defined states of the Data/FIFO SM are as follows:

{DISCON0-2} The DISCONnected 0 through DISCONnected 2 states are repetitively sequenced if the "DISC" input decode is true. This sequence is entered at {DISCON0} if the Mode 0 Reset is commanded via the MSEL0-2 inputs. While in this Sequence, the Idle/Disabled status word, the flow status word 1, and the flow status word 2 are presented in sequence on the data outputs of the Destination device. In addition to the standard transitions, this state sequence is exited to the {HSEQER} state if the "GLRC" or "DXFR" decodes are true, to the {IFIELD} state if the "HIFL" decode is true, or to the {IDLE} state if the "IDLG" decode is true.

{IFIELD} The I-FIELD state' is entered from the {DISCON0-2} state sequence if the "HIFL" decode is true. This state persists if the "HIFL" decode remains true. In addition to the standard transitions, this state is exited to {HSEQER} if the "GLRC" or "DXFR" decodes are true or to the {ILLINPT} state if the "IDLG" decode is true. The normal functional exit is the standard "DISC" to {DISCON0}. In this state the received I-Field from the HIPPI channel is presented on the data outputs of the Destination device.

{IDLE} The IDLE state is entered from the {DISCON0-2'} state sequence, the {INTRPKT} state or the {ENDBPKT} state if the "IDLG" decode is true. In addition to the standard transitions, this state is exited to the {HSEQER} state if the "DXFR" decode is true, to {ILLINPT} if the "HIFL" decode is true, and to the {BGNPKT} state if the "GLRC" decode is true. In this pre- and inter-packet state the general op status word is presented on the data outputs of the Destination device.

{BGNPKT} The BeGiN PacKeT state is entered from the {IDLE} state, the {INTRPKT} state or the {ENDBPKT} state if the "GLRC" decode is true. In addition to the standard transitions, this state is exited to the {HSEQER} if the "IDLG" decode is true, to the {ILLINPT} state if the "HIFL" decode is true, to the {PKTNBST} state if the "GLRC" decode is true, and to the {DTATRNSF} state if the "DXFR" decode is true. In this state the general op status word is presented on the data outputs of the Destination device.

{PKTNBST} The PacKeT No BurST state is entered from the {BGNPKT} state if the "GLRC" decode is true. This state persists if the "GLRC" decode remains true. In addition to the standard transitions, this state is exited to the {HSEQER} state if the "IDLG" decode is true, to the {ILLINPT} state if the "HIFL" decode is true, and to the {DTATRNSF} state if the "DXFR" decode is true. In this state the general op status word is presented on the data outputs of the Destination device.

{DTATRNSF} The DaTA TRaNSFer state is entered from the {BGNPKT} state, the {PKTNBST} state , or the {IBSTGP} state if the "DXFR" decode is true. this state persists if the "DXFR" decode remains true. In this state Burst data is received and presented to the data outputs of the Destination device. In addition to the standard transitions, this state is exited to the {HSEQER} state if the "IDLG" decode is true, to the {ILLINPT} state if the "HIFL" decode is true, or to the {LLRCCH} state if the "GLRC" decode is true.

{LLRCCH} The LLRC CHaracter state is entered from the {DTATRNSF} state if the "GLRC" decode is true. In this state the received LLRC character from the HIPPI channel is presented on the data outputs of the Destination device. During this state, the internally calculated LLRC character is compared to the received character and the result of this comparison is presented one clock cycle later on the RLLER output of the Destination device. In addition

Figure 7. S2021 Data/FIFO SM Input Decode Alphabet

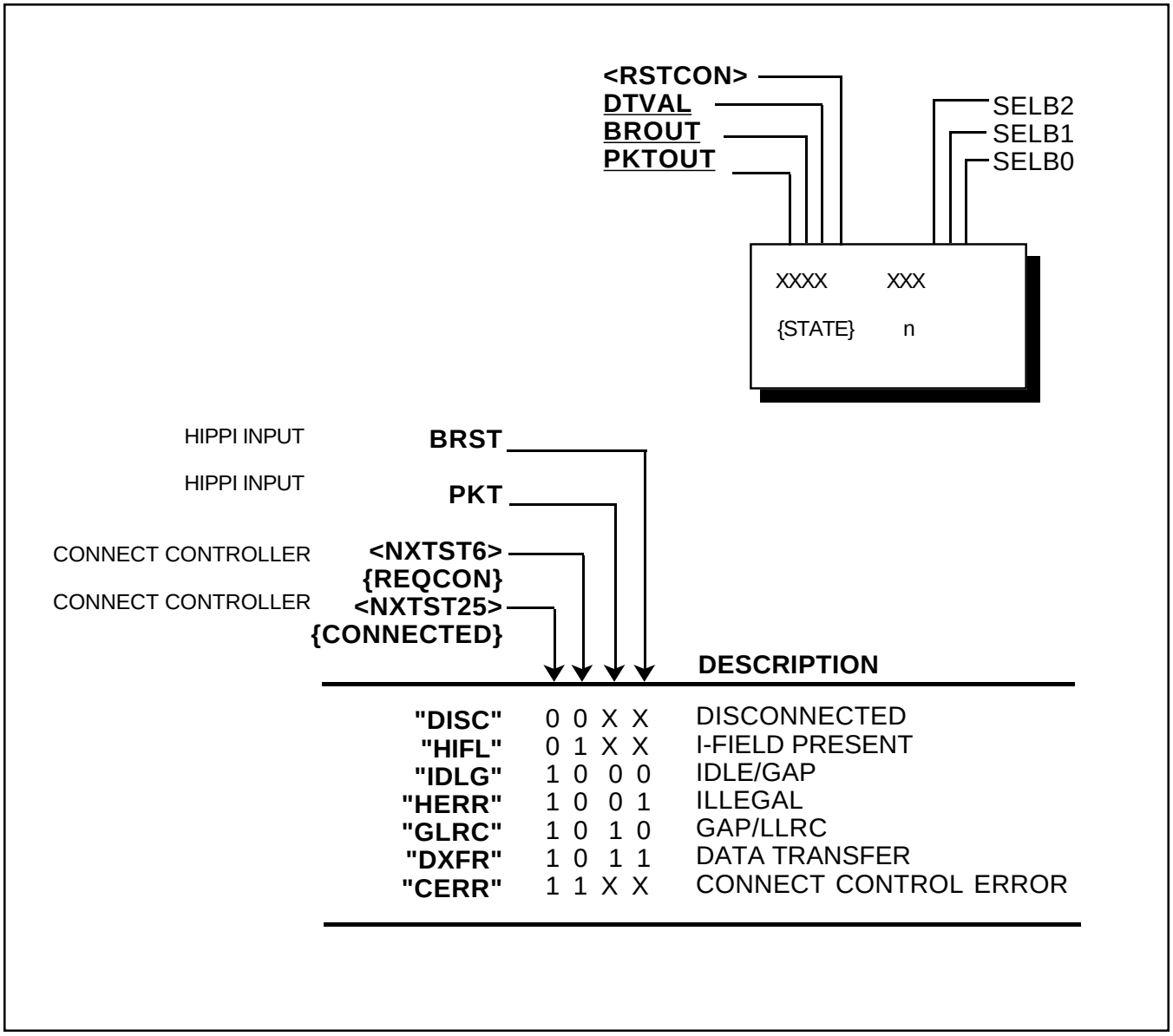


Figure 8. S2021 Host Data/FIFO SM State Transition Diagram

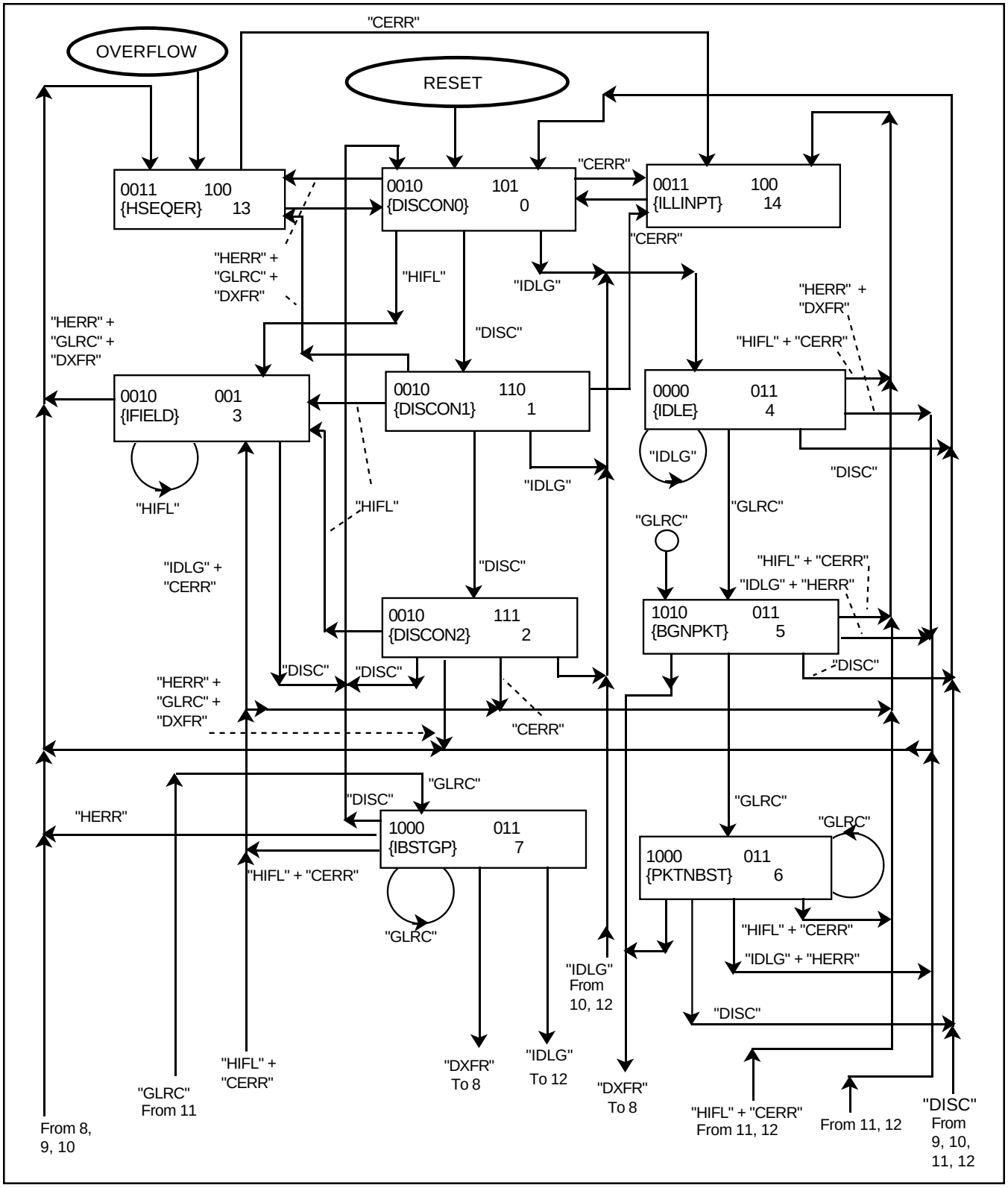
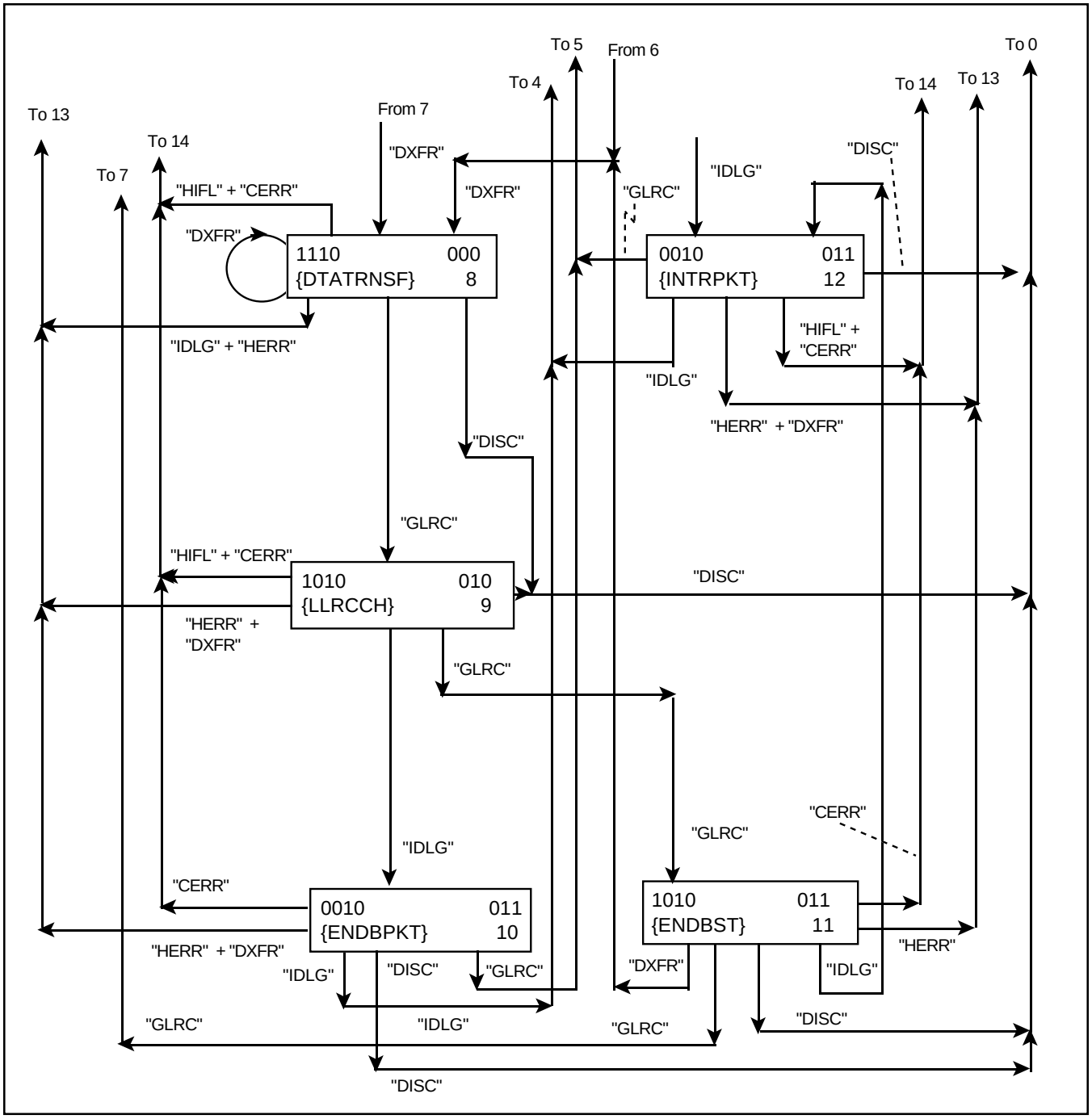


Figure 8. S2021 Host Data/FIFO SM State Transition Diagram (continued)



to the standard transitions, this state is exited to the {HSEQER} state if the “DXFR” decode is true, to the {ILLINPT} state if the “HIFL” decode is true, to the {ENDBPKT} state if the

“IDLG” decode is true, or to the {ENDBST} state if the “GLRC” decode is true.

{ENDBST} The END BurST state is entered from the {LLRCCH} state if the “GLRC” decode is true. In this state the general op status word is presented on the data outputs of the Destination device. In addition to the standard transitions, this state is exited to the {ILLINPT} state if the “HIFL” decode is true, to the {DTATRNSF} state if the “DXFR” decode is true, to the {IBSTGP} state if the “GLRC” decode is true, or to the {INTRPKT} state if the “IDLG” state is true.

{IBSTGP} The Inter BurST GaP state is entered from the {ENDBST} state if the “GLRC” decode is true. This state persists if the “GLRC” decode remains true. In this state the general op status word is presented on the data outputs of the Destination device. In addition to the standard transitions, this state is exited to the {ILLINPT} state if the “HIFL” decode is true, to the {DTATRNSF} state if the “DXFR” decode is true, or to the {INTRPKT} state if the “IDLG” decode is true.

{INTRPKT} The INTeR PacKeT state isentered from the {IBSTGP} state or from the {ENDBST} state if the “IDLG” decode is true. In this state the general op status word is presented on the data outputs of the Destination device. In addition to the standard transistions, this state is exited to the {HSEQER} state if the “DXFR” decode is true, to the {ILLINPT} state if the “HIFL” decode is true, to the {BGNPKT} state if the “GLRC” decode is true, or to the {IDLE} state if the “IDLG” decode is true.

{HSEQER} The HIPPI SEQuence ERror state is entered unconditionally if the OVERFLOW condition occurs (Burst received when Burst and Ready counters are equal). The {HSEQER} is also entered from all states except {ILLINPUT}. For specific states other decodes incorrect that state will also froce the {HSEQER} state. In this state the Sequence Error status word is presented to the data outputs of the Desination device. During this state the <RSTCON> signal is generated to force the reset of the Connect Control SM and abandon the compromised HIPPI Connection. This state is exited to the {DISCON0} state unconditionally on the next clock cycle.

{ILLINPT} The ILLegal INPuT signals state is entered from all other states except the {HSEQER} state if the “CERR” decode is true. For specific states other decodes incorrect that state will also force the {ILLINPT} state. In this state the Sequence Error status word is presented to the data outputs of the Desination device. During this state the <RSTCON> signal is generated to force the reset of the Connect Control SM and abandon the compromised HIPPI Connection. This state is exited to the {DISCON0} state unconditionally on the next clock cycle.

4.3 HOST DATA/FIFO SM EXTERNAL OUTPUTS

PKOUT PacKet OUT signal to the Destination Host system. A ‘1’ on this signal indicates the detection and sychronization of an asserted PKT signal from the HIPPI channel. A ‘0’ indicates the end of a HIPPI Packet.

BROUT BuRst OUT stignal to the Destination Host system. A ‘1’ on this signal indicates the detection and synchronization of an asserted BRST signal from the HIPPI channel. A ‘0’ indicats a deasserted BRST signal.

DTVAL DaTa VALid signal to the Destination Host system. This signal is at a ‘1’ when new data or status is available on the data outputs of the Destination device. This signal is at ‘0’ in the {IDLE}, {IBSTGP}, and {PKTNBST} states.

SELB0-2 SELect Bus 0, 1, 2 signals’ to the Destination Host system. These signals are intended to be the primary addressing delimiters of the various status and data words presented at the data outputs of the Destination device. The functions of these signals are described in the S2020/S2021 Preliminary Device Specification.

Figure A-1. Source Flow Diagram

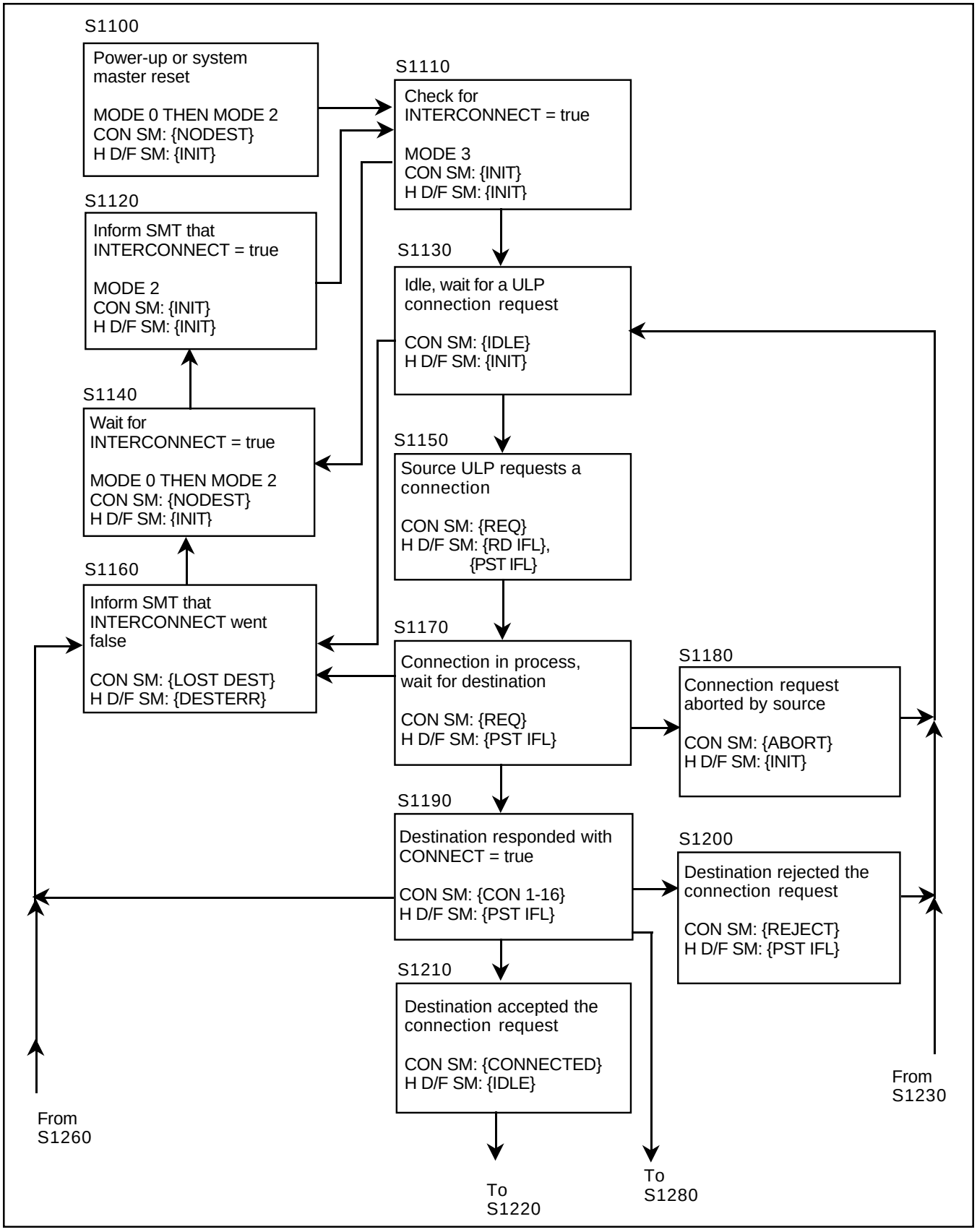


Figure A-1. Source Flow Diagram (continued)

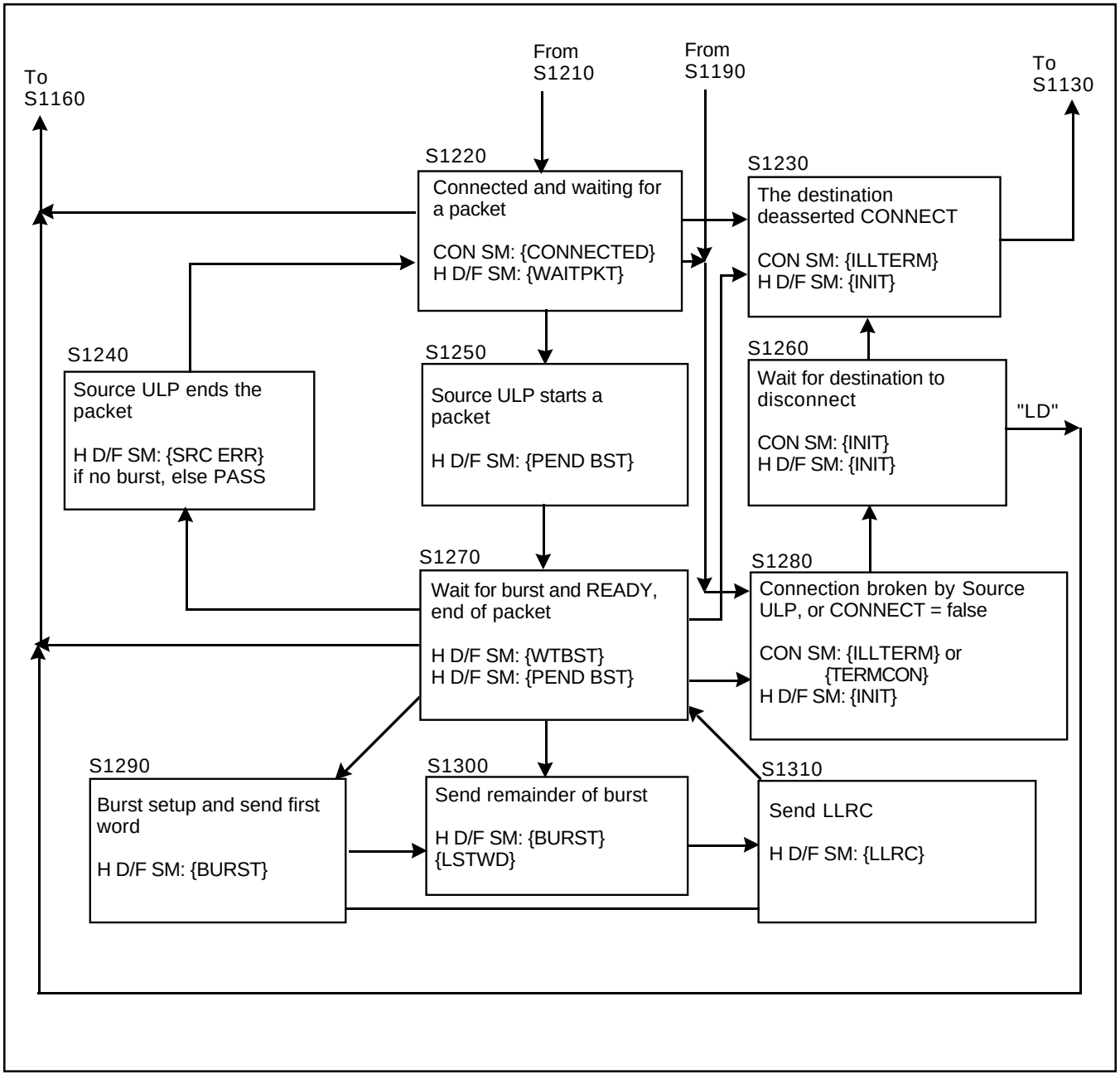


Figure A-2. Destination Flow Diagram

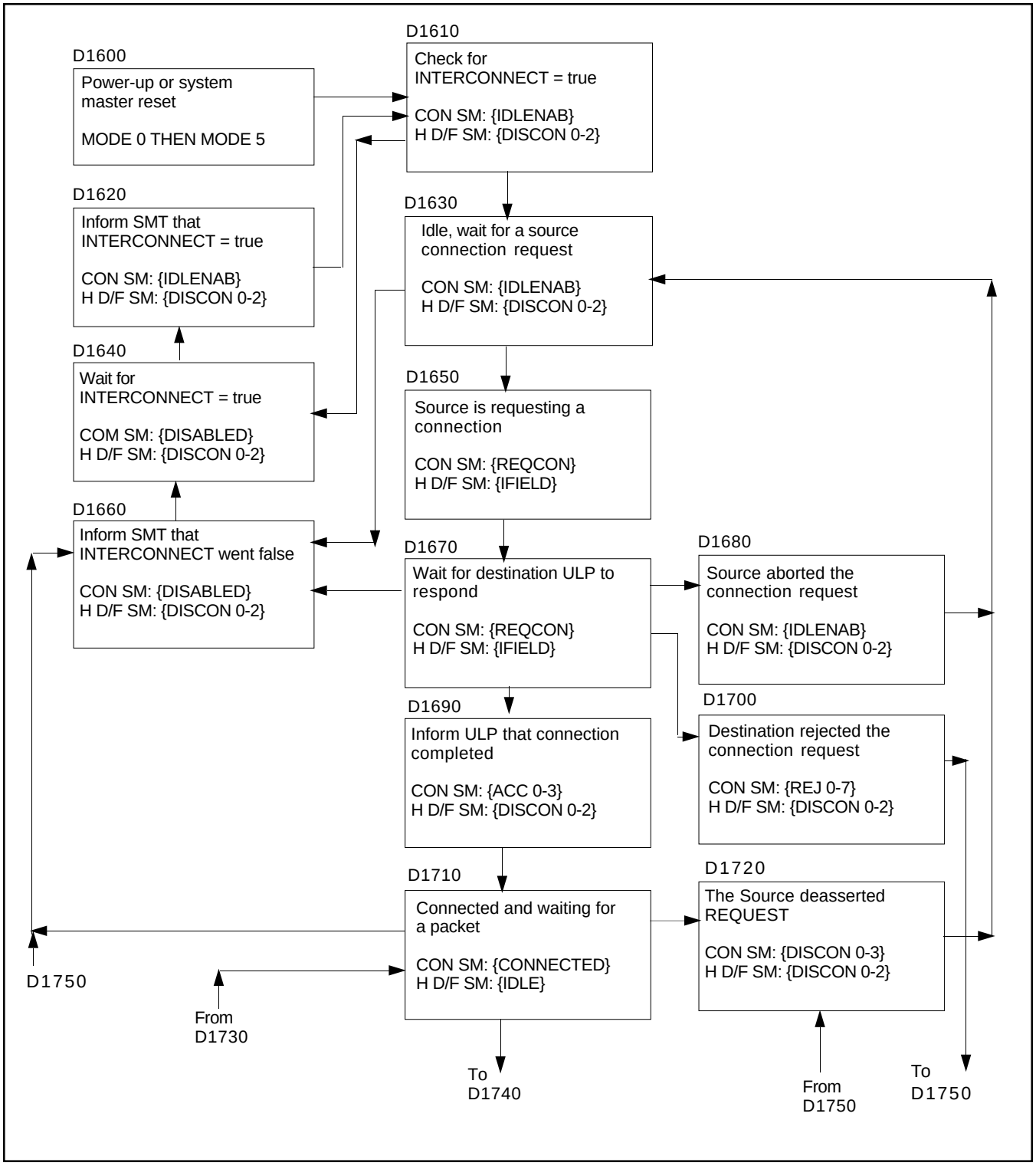
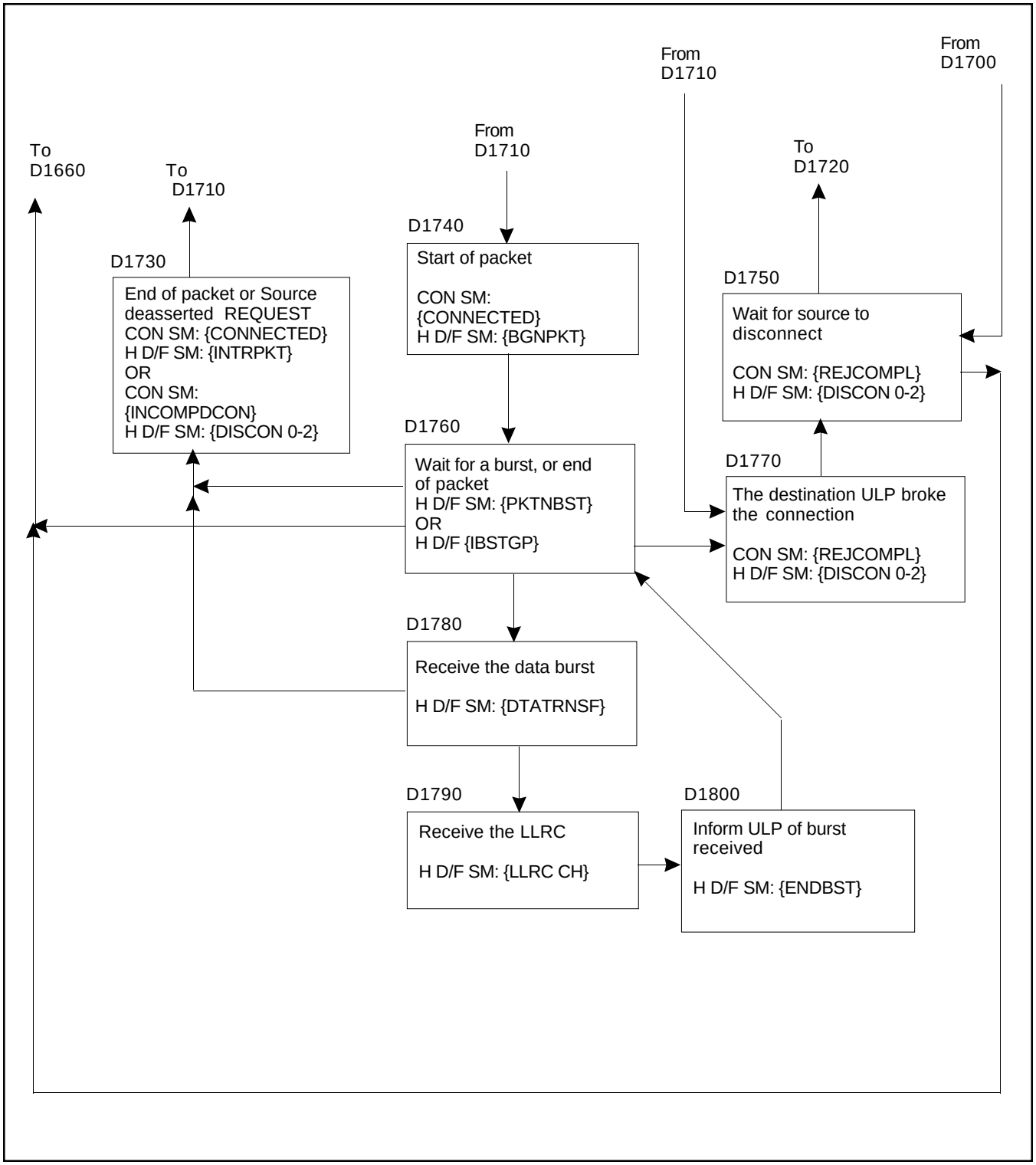


Figure A-2. Destination Flow Diagram (continued)



SELECT = 0: HIPPI CHANNEL DATA

DOUT0-31

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

BYTE 0								BYTE 1								BYTE 2								BYTE 3							
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT = 1: HIPPI I-FIELD

DOUT0-31

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

BYTE 0								BYTE 1								BYTE 2								BYTE 3							
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

HOST DATA BUS FORMAT IN FUNCTIONAL MODE

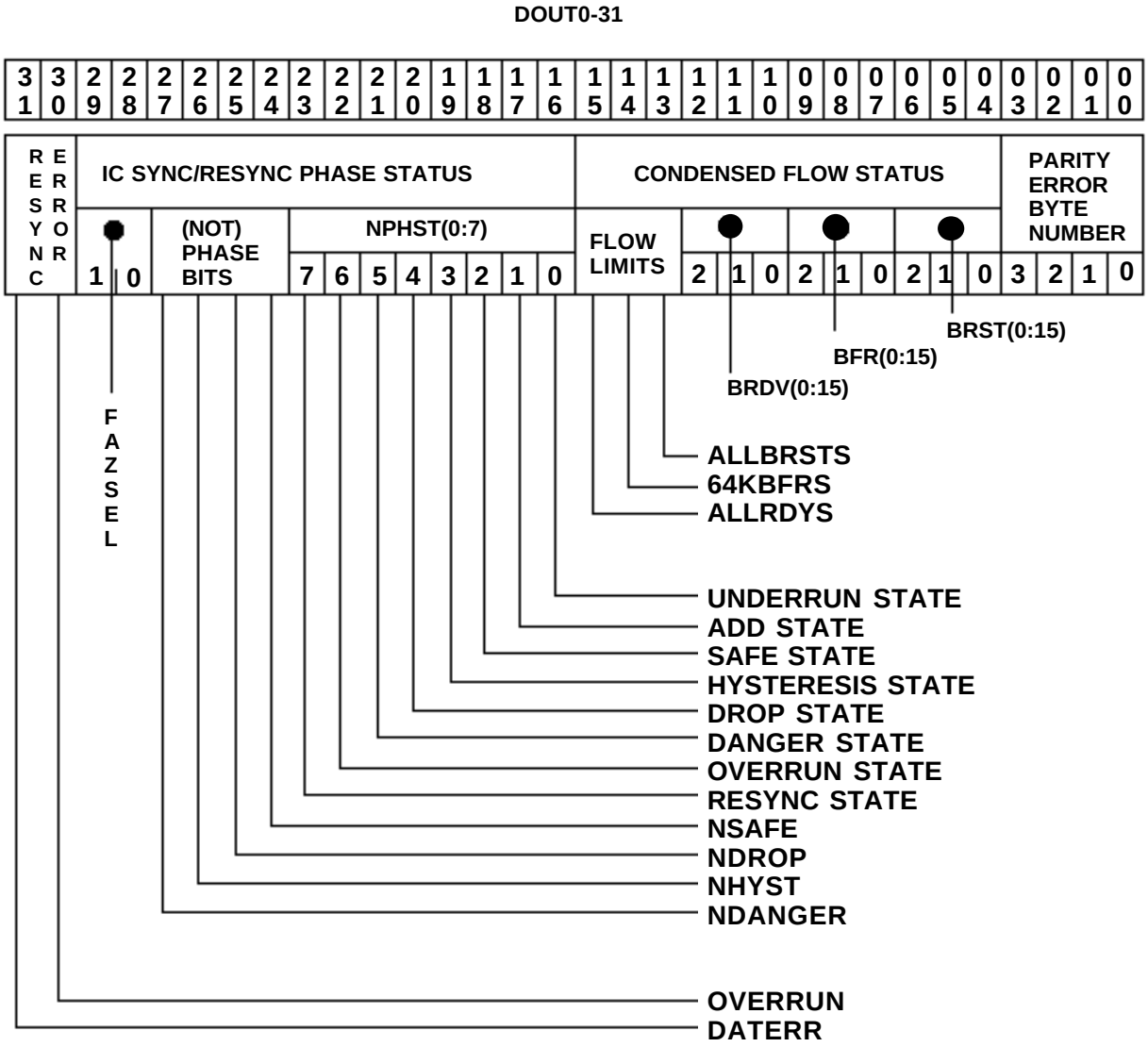
SELECT = 2: HIPPI BURST LLRC WORD

DOUT0-31

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BYTE 0								BYTE 1								BYTE 2								BYTE 3							
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

HOST DATA BUS FORMAT IN FUNCTIONAL MODE

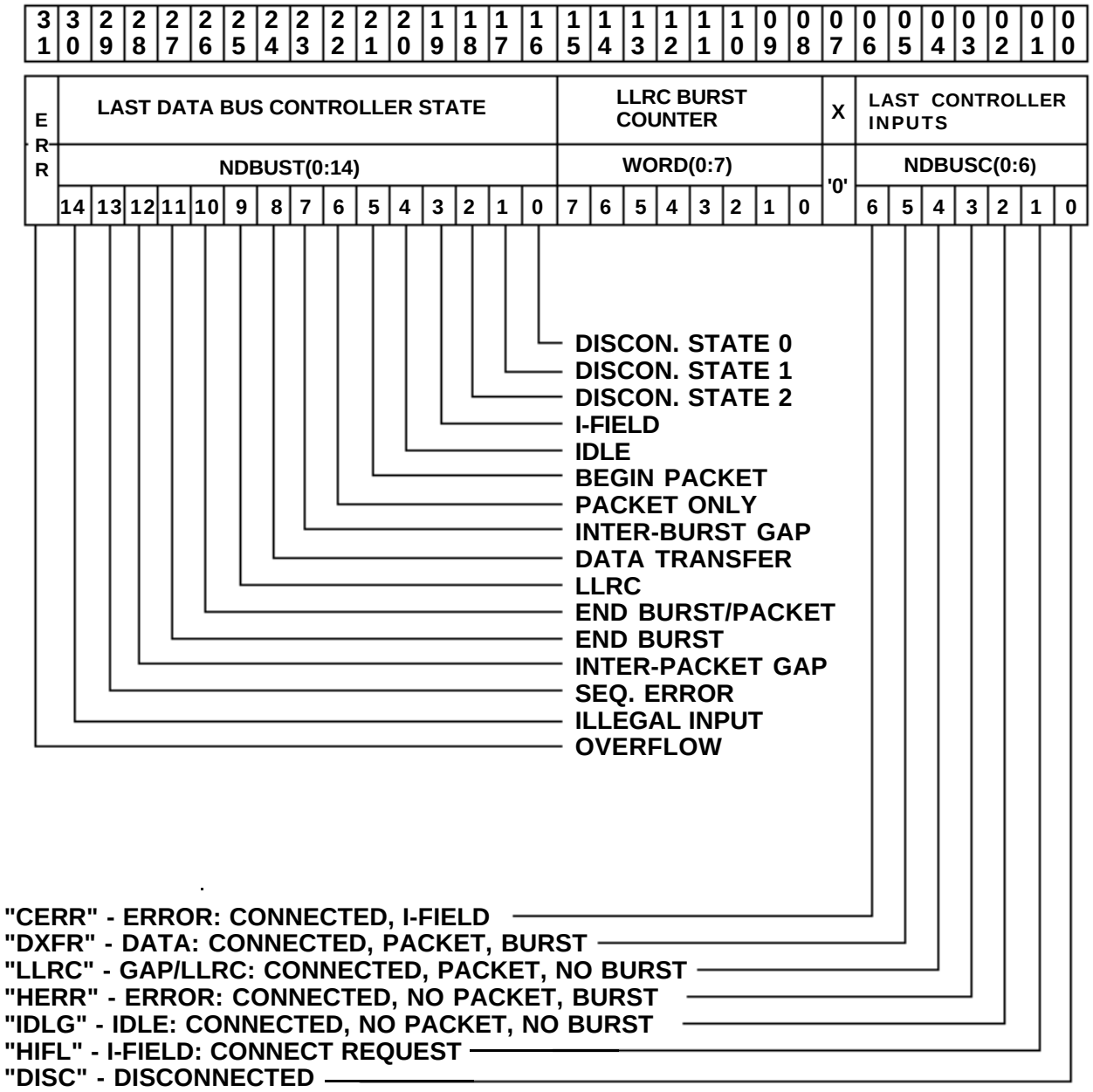
SELECT 3: GENERAL OPERATIONAL STATUS



HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT 4: SEQUENCE ERROR STATUS

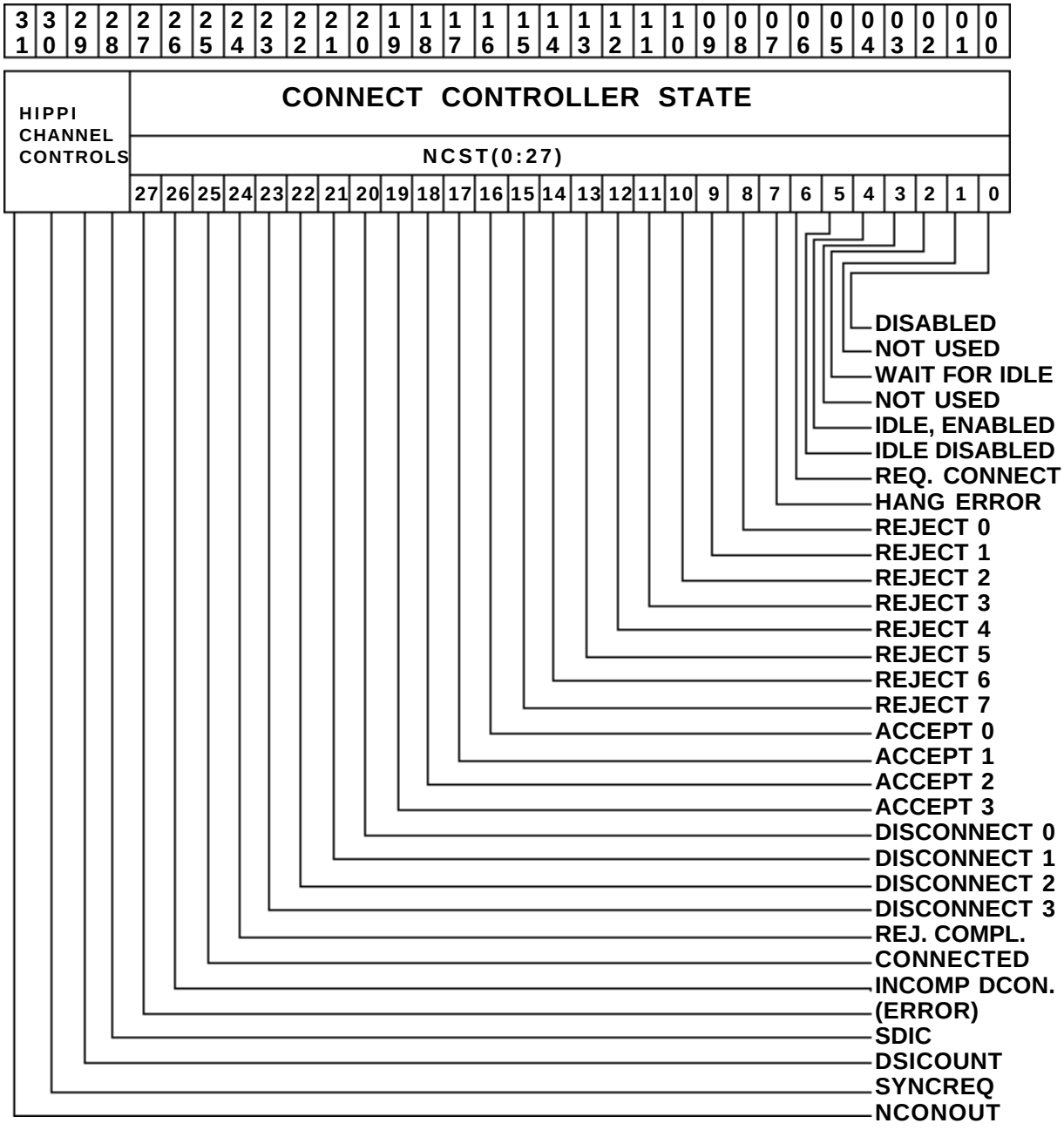
DOUT0-31



HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT 5: IDLE/DISABLED STATUS

DOUT0-31



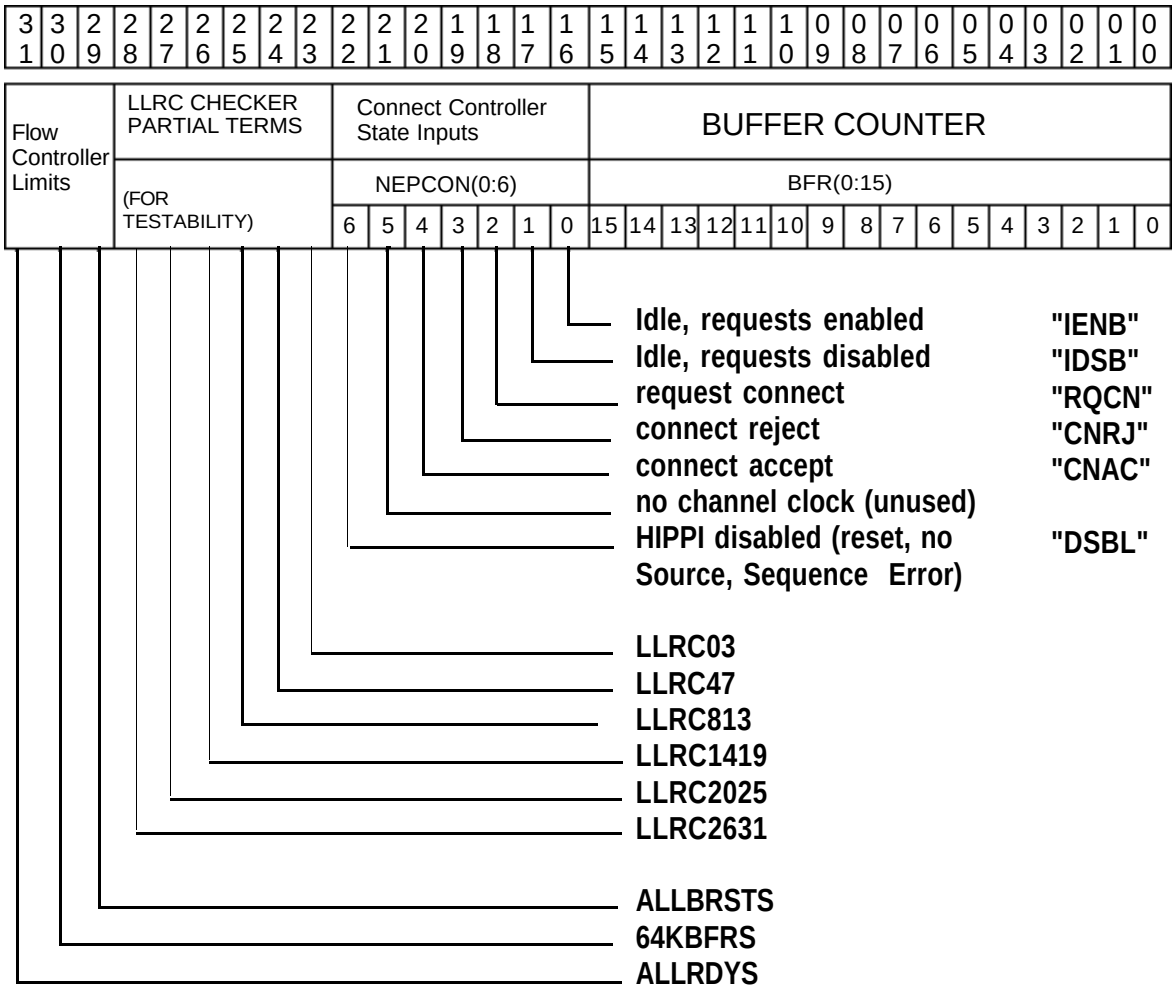
HOST DATA BUS FORMAT IN FUNCTIONAL MODE

SELECT = 6: FLOW STATUS WORD 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
READY COUNTER																BURST COUNTER															
RDY(0:15)																BRST(0:15)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SELECT 7: FLOW STATUS WORD 2

DOUT0-31



HOST DATA BUS FORMAT IN FUNCTIONAL MODE