E4 FRAMING CIRCUIT DESIGN

The S3005/S3006 parts can be used to implement serializer/deserializer CMI encode/decode and the clock synthesis/recovery functions for the CCITT PDH E4 standard. In E4 (CMI) mode, however, the framing of the 8-bit data bus is not performed in the logic of the S3006. This application note explains how this logic can be designed in the adjacent controller device. The logic functions and frequency of operation will allow the function to be implemented in a FPGA device or a CMOS ASIC.

Framing Pattern

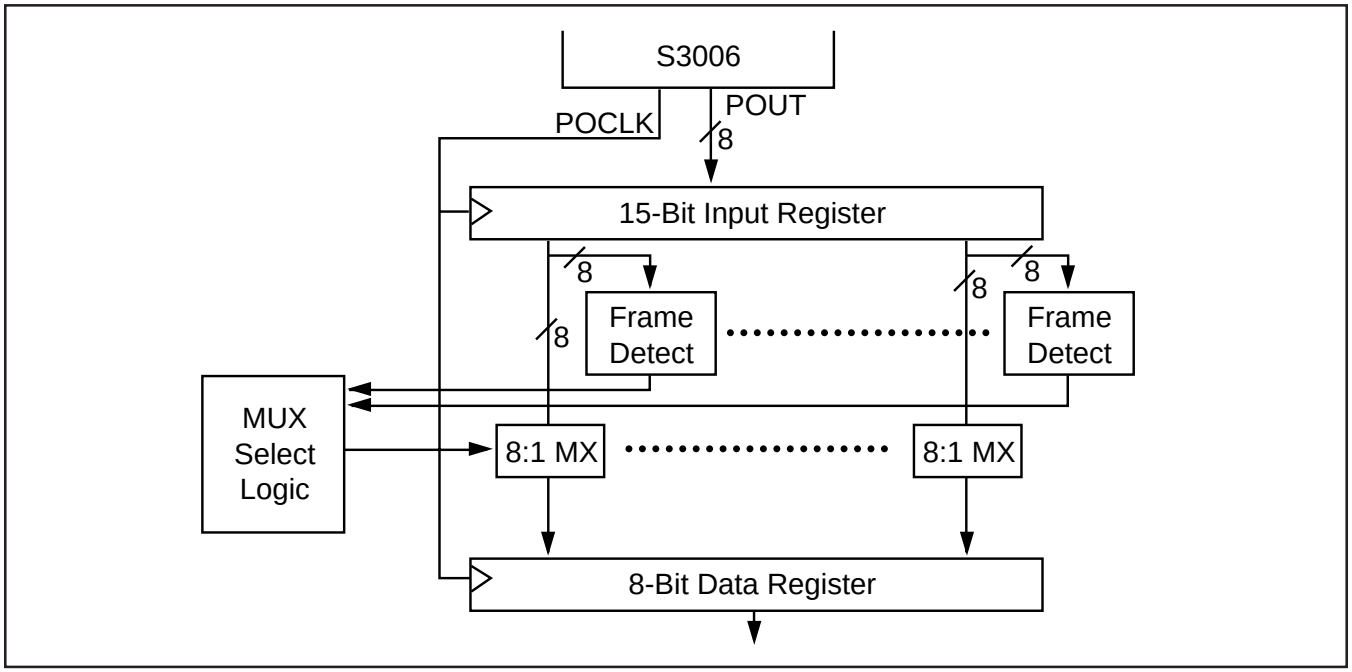
The E4 Frame Detect block decodes the 111110100000 pattern for compliance to the E4 standard.

General Design

The S3006 parallel output data is sampled in each of eight possible alignments until the correct framing pattern and sequence is seen. When the correct framing pattern is detected by the E4 frame detect block the 8:1 multiplexer selection is "frozen" and the correctly framed data will be presented in the frame register. This circuit will frame (assuming no bit errors) in a single frame. Additional filter logic can be added to look for 3 consecutive "correct" framing patterns before declaring frame sync. In addition, the frame detect logic should be monitored to verify that correct framing sequences are being seen after frame sync is achieved. If correct framing sequences are not detected then the frame search logic should be enabled again.

The circuit as shown in Figure 1 consists of an input register, eight 8:1 multiplexers, the multiplexer select logic, and the E4 frame pattern detect logic. The timing of the circuit is done using the S3006 POCLK which is operating at 17 MHz. Data is clocked into the input register from the POUT data lines of the S3006. The data is then routed to the 8:1 multiplexers which select the eight possible byte alignments. The frame register contains the data to be examined for correct frame alignment by the E4 frame detect logic. The frame detect logic detects all of the possible byte alignments of the E4 framing pattern. When the FA pattern is detected, the multiplexer selection is then "frozen" and the additional ØX pattern is checked before declaring frame sync. The detailed circuit design and timing diagrams are shown in Figures 2 and 3.

Figure 1. E4 Framing Block Diagram



BLOCK DESCRIPTIONS

Input Register: 15-bit register which holds all the possible positions of the unframed data. The bit position of the data in this register is dependent on the random alignment of the data outputs of the S3006.

8:1 Multiplexers: These eight multiplexers select the data alignment to be clocked into the data register.

Frame Detect: These are 8 wide decoders which decode the 111110100000 E4 framing pattern. The inputs are connected to each of the eight possible locations of the framing pattern.

Multiplexer Select Logic: This block takes in the results of all the decoder blocks and outputs the correct 8:1 multiplexer select values.

Data Register: This block contains the correctly framed data after frame alignment has occurred.

Figure 2. Detailed Schematics of E4 Framing Circuit

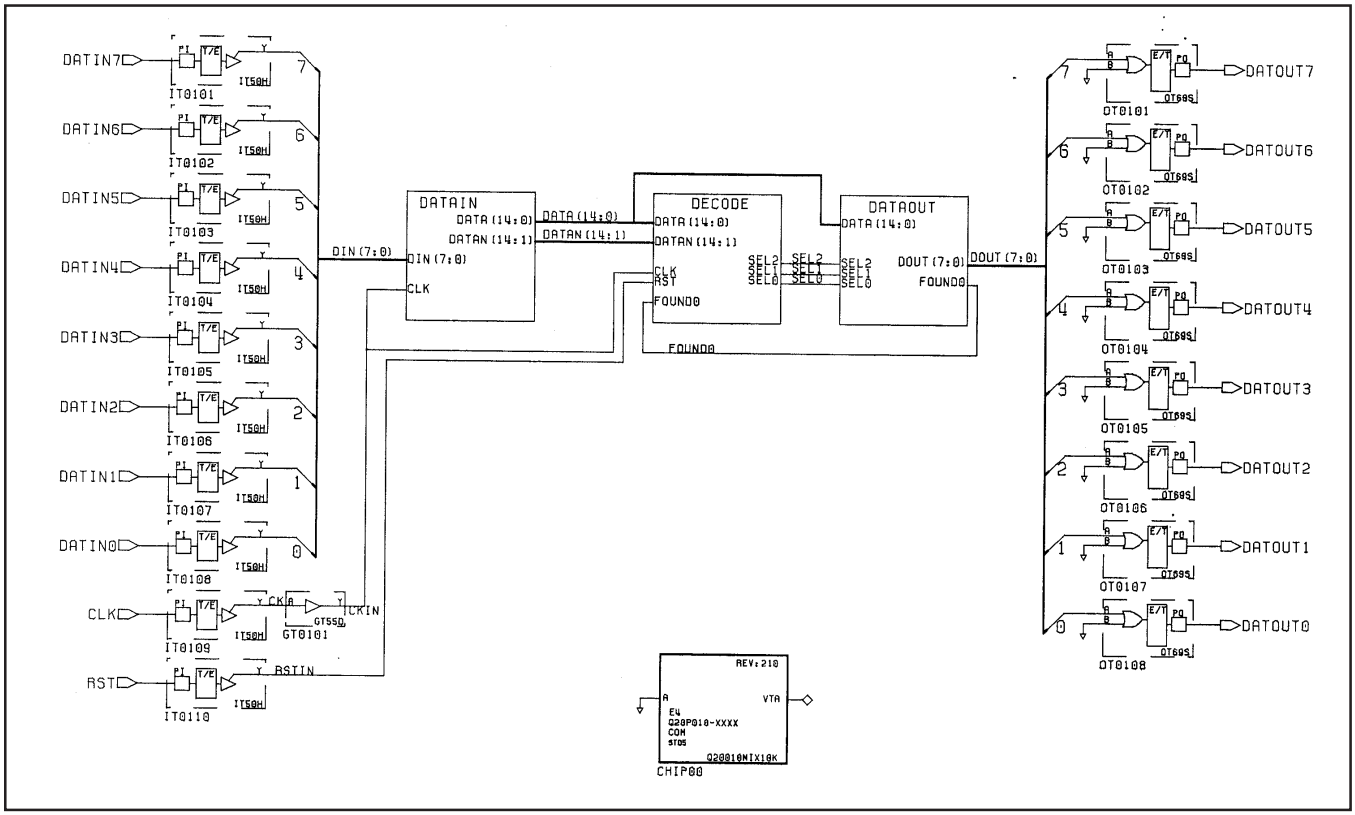


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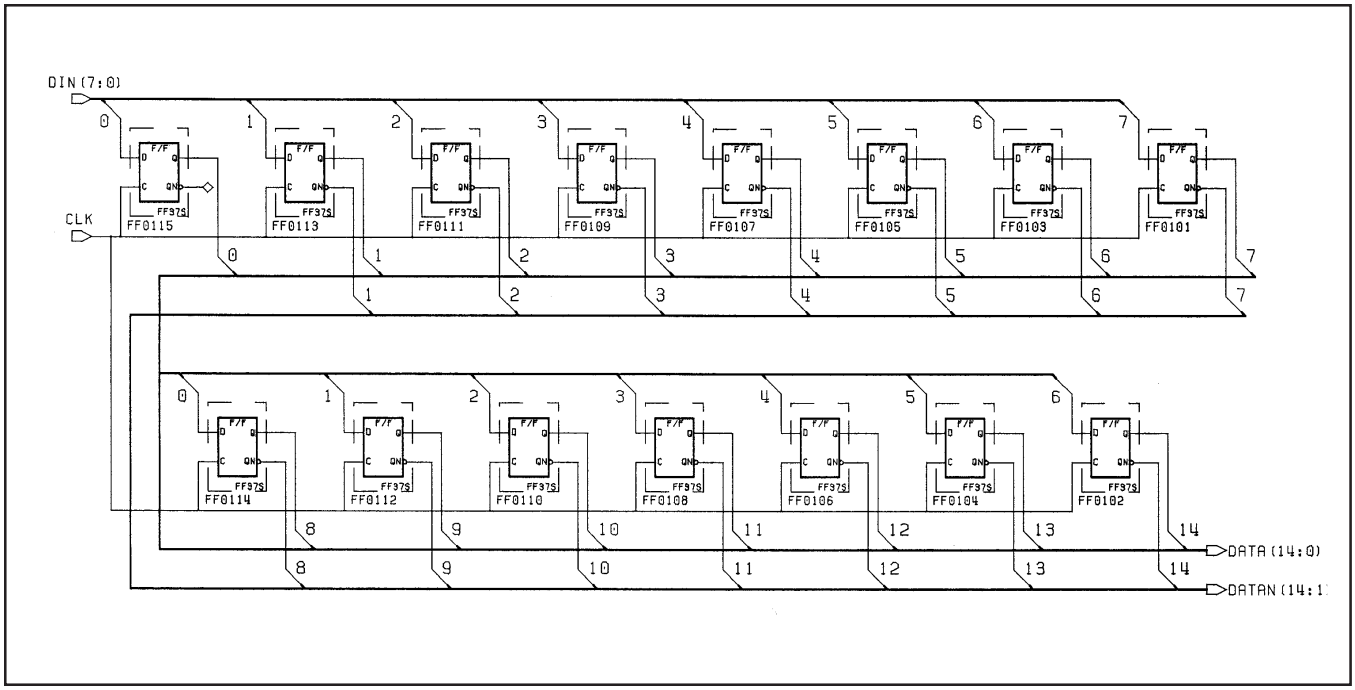
Figure 2. Detailed Schematics of E4 Framing Circuit (Con't.)



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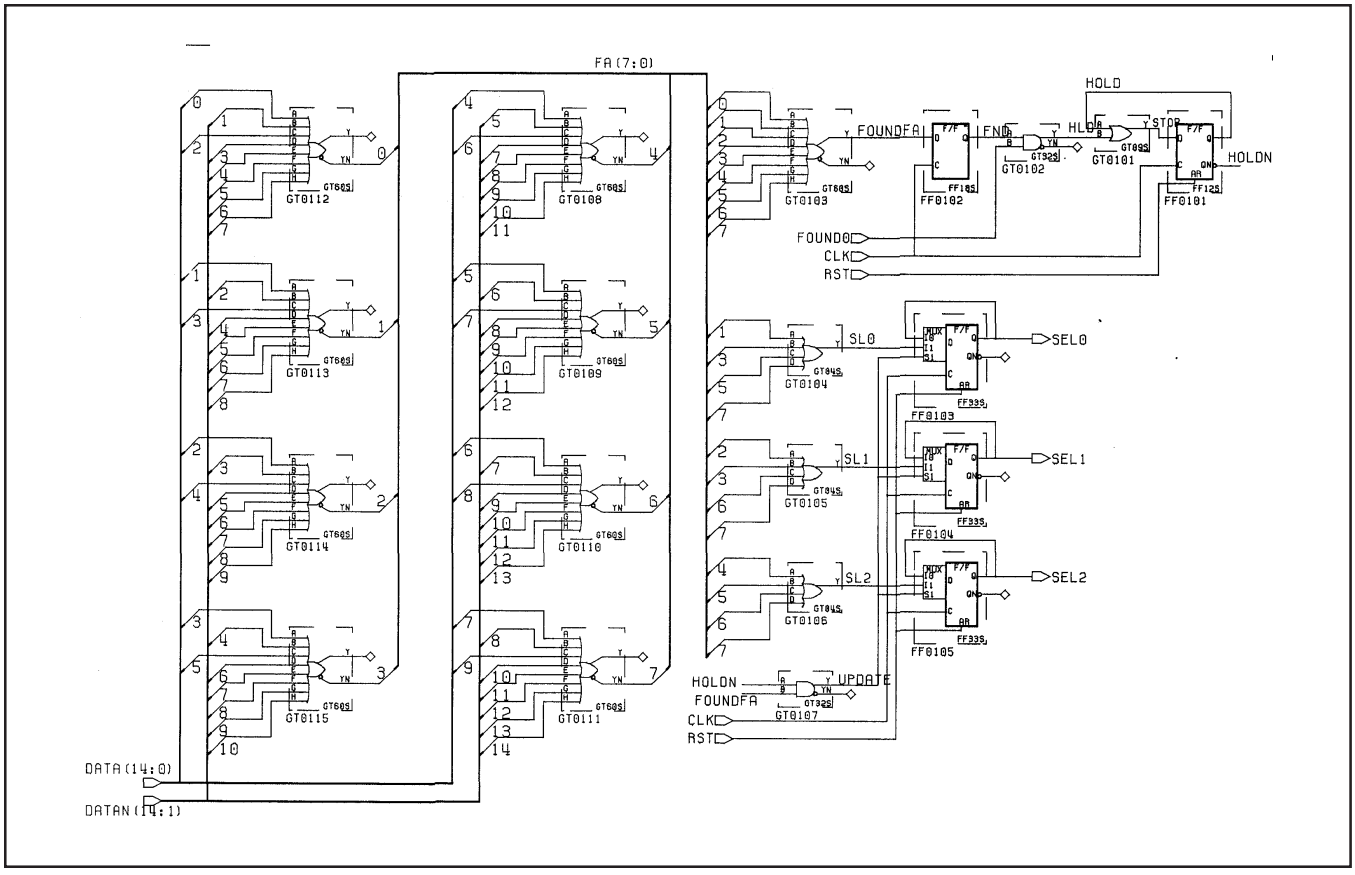

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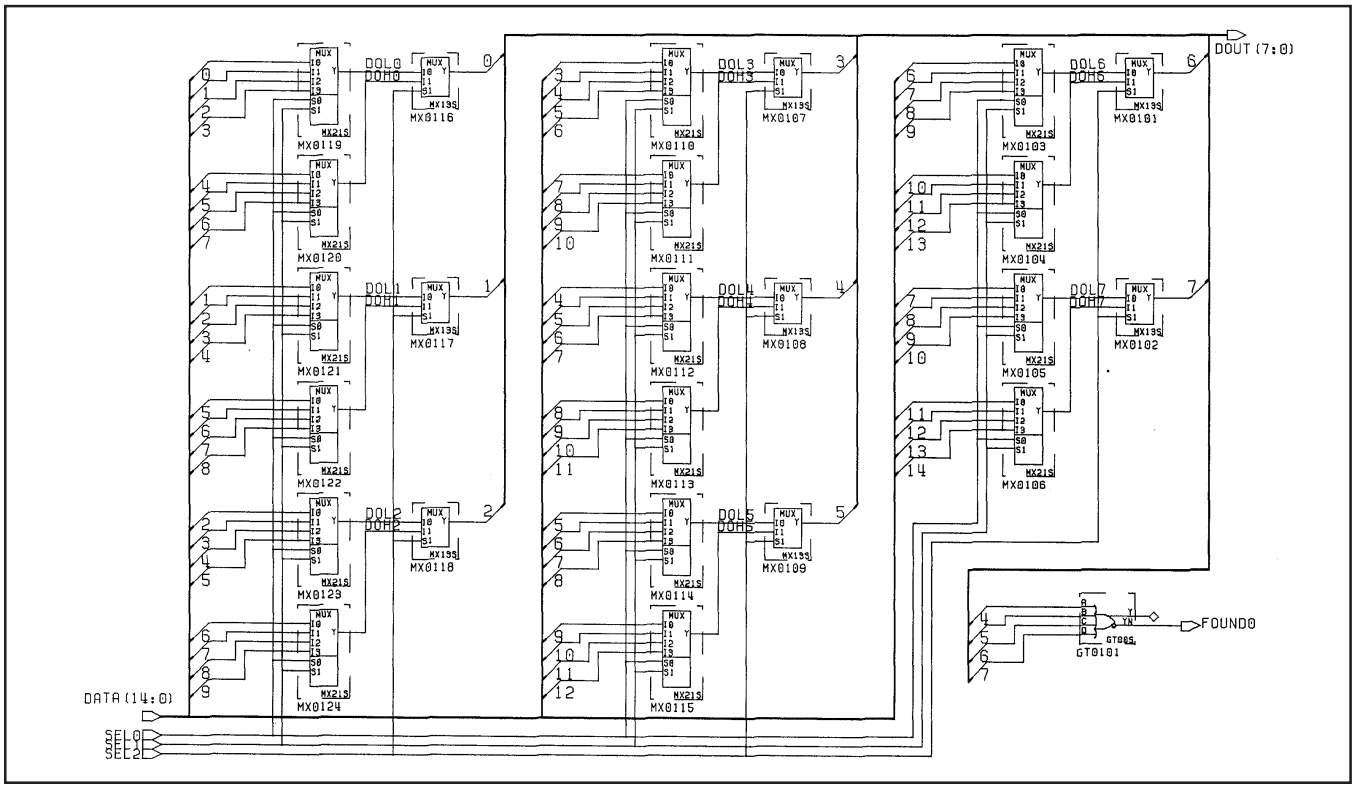
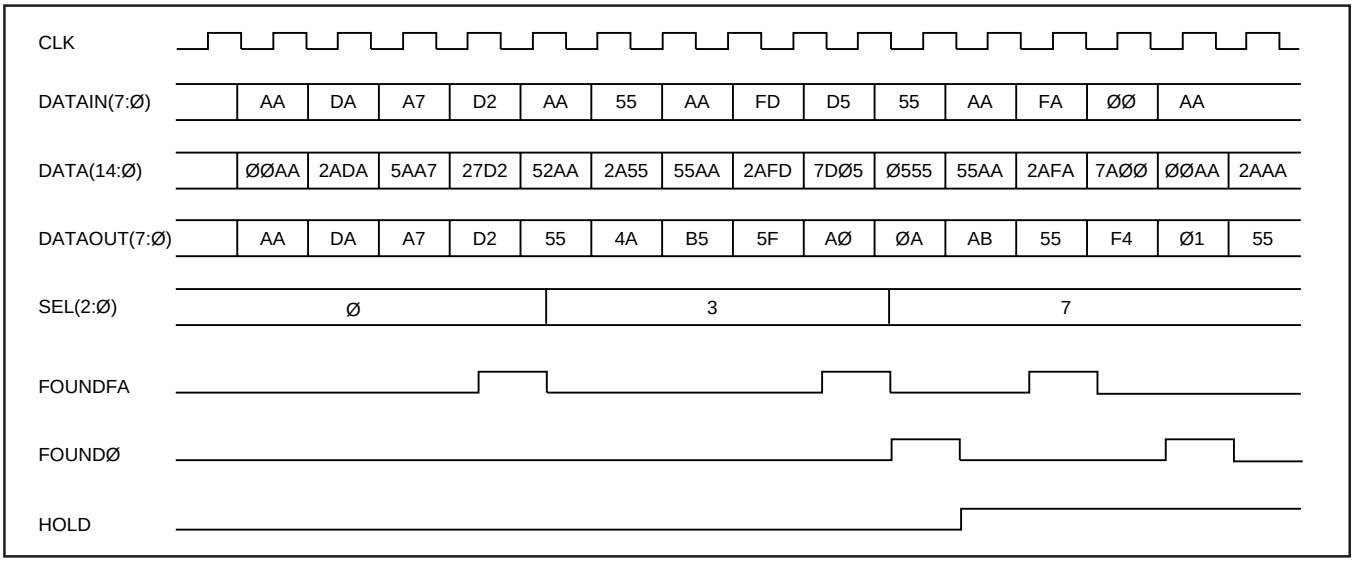


Figure 3. Timing Diagrams for E4 Framing Circuit



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