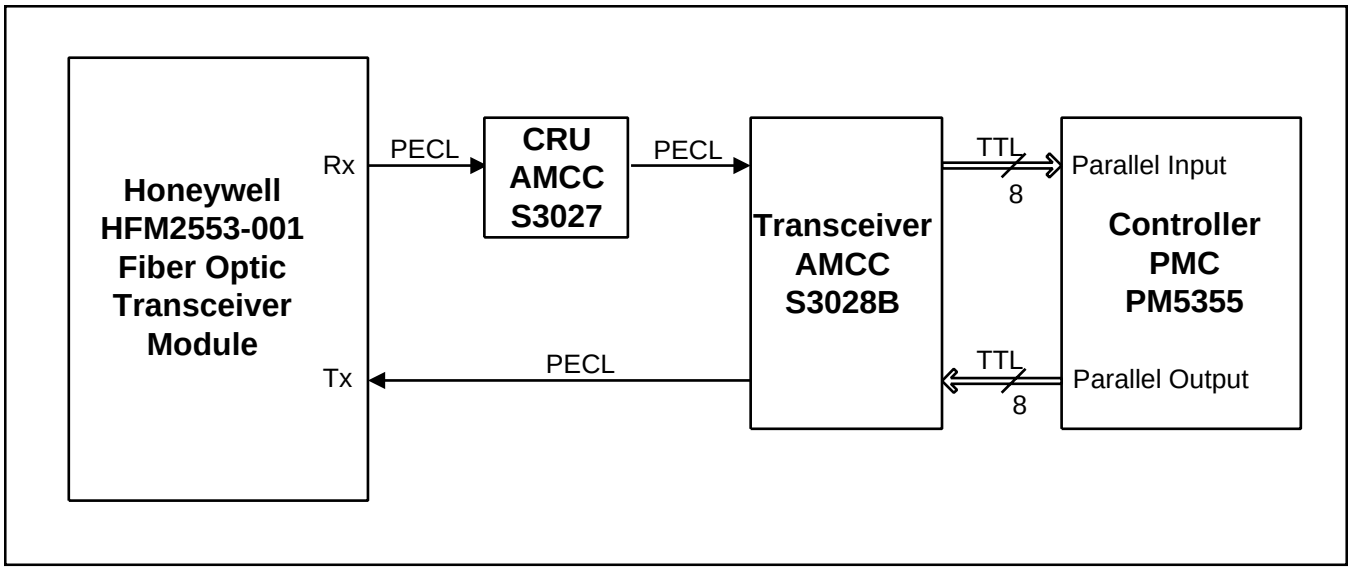
Purpose: This application note is to provide the designer with a short haul 850nm LAN application solution

INTRODUCTION

The AMCC S3028B SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET STS-12/STM-4 (622.08 Mbps) interface device. This device is suitable for SONET-based ATM applications and can be used in conjunction with AMCC's S3027 Clock Recovery Device. The AMCC S3028B transceiver chip provides the first stage of digital processing of a receive and a transmit SONET STS-12 bit-serial stream. In the receive path, it converts a bit-serial data stream into a byte-serial data (parallel data) format and in the transmit path, it converts byte-serial data (parallel data) into bit-serial data. Figure 1 shows an application block diagram with a AMCC S3028B, S3027, PMC PM5355 and a Honeywell HFM2553-001. Figure 2 shows specifically the design details. Combining these devices provides a Physical Media Dependent (PMD) layer for SONET/SDH/ ATM data transfer.

Figure 1. Typical Network Application Block Diagram

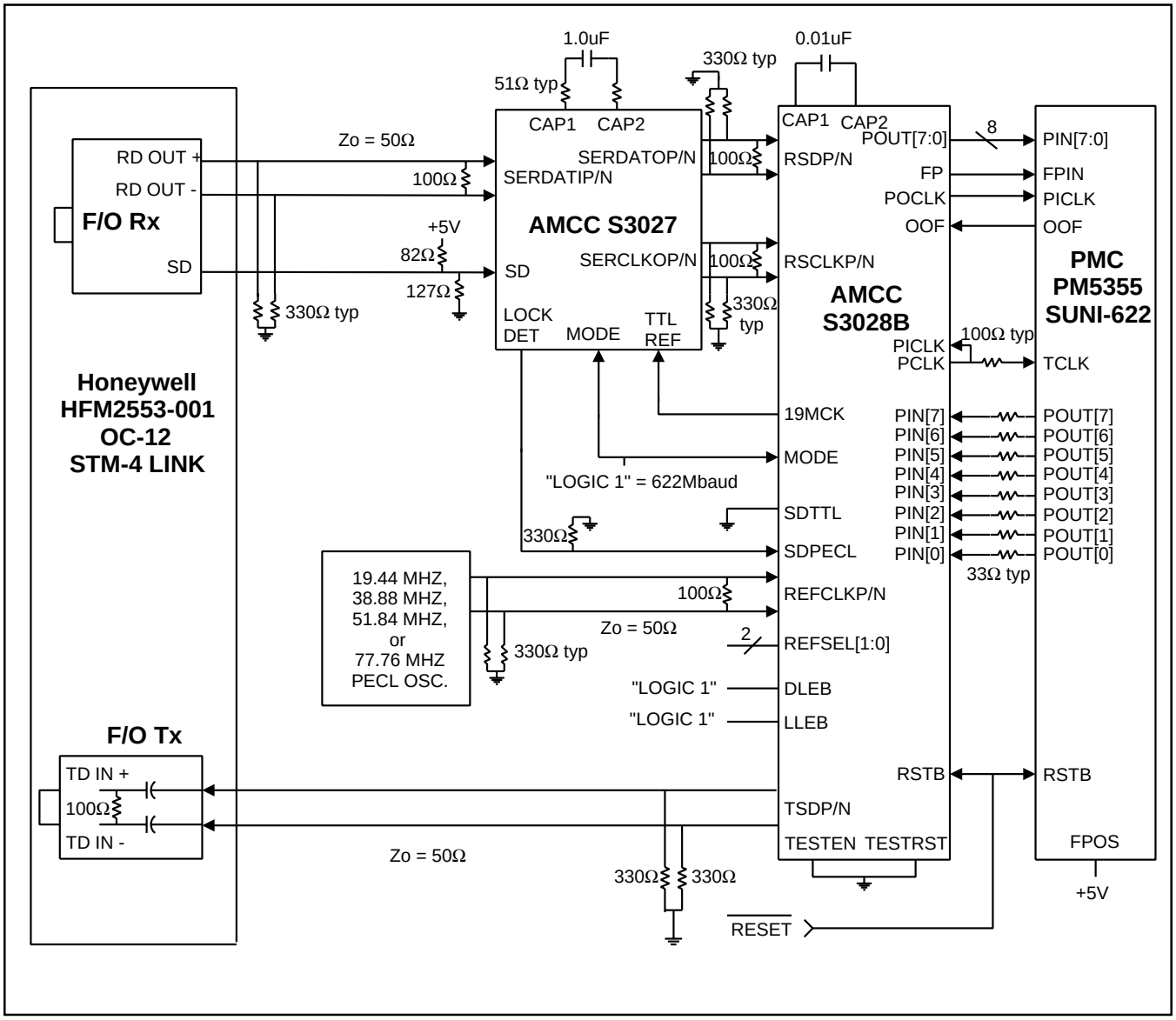


Signal Connect Description

Figure 1 shows the block diagram of this solution.

1. The Honeywell fiber optic transceiver interfaces to the AMCC S3027 Clock Recovery Unit (CRU) via a PECL bit-serial data stream.
2. After the clock is recovered from the bit-serial data stream the CRU transmits the PECL recovered clock and PECL re-timed data to the AMCC S3028B transceiver.
3. The AMCC S3028B searches the incoming serial data stream for the frame and byte boundaries.
4. The AMCC S3028B transmits the bit-serial data converted to byte-serial data to the PMC PM5355 via an 8-bit parallel TTL interface.
5. The PMC PM5355 transmits byte-serial data to the AMCC S3028B via an 8-bit parallel TTL interface.
6. The AMCC S3028B transmits the bit-serial data to the Honeywell fiber optic transceiver via a PECL interface.

Figure 2. AMCC S3028B, PMC PM5355, & Honeywell Optics HFM2553-001 Block Diagram



Notes:
1. The F/O Tx AC couples lines, terminates lines to 50Ω, and sets the DC bias internal to the part.
2. The F/O Rx SD line is terminated to 50Ω and DC biased to Vcc-2V by the 82 and 127Ω resistors.
3. SD PECL HI - Valid data at the input of fiber optic receiver, remains high as long as bit error rate is less than 10^9.
4. SD PECL LOW - No data at the input of fiber optic receiver.

Parts List

The following is a parts list that is a recommendation to the designer to implement the circuit in Figure 2.

QTY	Part # or equivalent	Description
1		Resistor, 127 W, 10%, 1/8W, 805 or 603 package size
1		Resistor, 82 W, 10%, 1/8W, 805 or 603 package size
2		Resistor, 51 W, 10%, 1/8W, 805 or 603 package size
5		Resistor, 100 W, 10%, 1/8W, 805 or 603 package size
11		Resistor, 330 W, 10%, 1/8W, 805 or 603 package size
8		Resistor, 33 W, 10%, 1/8W, 805 or 603 package size
1		Capacitor, 1.0 mf, 10%, X7R, 16V, Surface Mount package
1		Capacitor, 0.01 mf, 10%, X7R, 16V, Surface Mount package
1	S3028B	SONET/SDH/ATM OC-3/OC-12 Transceiver
1	S3027	SONET/SDH Clock Recovery Unit
1	PM5355	PMC SUNI-622
1	HFM2553-001	Honeywell 5V Fiber Optic 1 x 9 Transceiver
1		PECL Oscillator

Theory of Operation

1. The S3027 extracts the clock and re-times the data from the received differential PECL serial data input (SERDATIP/N) coming from the Honeywell Fiber Optic Receiver (F/O Rx) when the Signal Detect (SD) is a PECL high level. When Signal Detect (SD) is at a PECL Low level, the Phase Lock Loop (PLL) will be forced to lock to the TTL Reference (TTL REF).

2. The S3028B receives the OC-12/STM-4 (622.08 Mbps) scrambled NRZ data signals on the serial data stream (RSDP/N) PECL inputs. These inputs are clocked into the S3028B by the Receive Serial Clock (RSCLKP/N) PECL inputs. This clock is used by the receive section as the master clock to perform framing and deserialization functions.

3. After the data is received, the Frame and Byte Boundary Detection circuitry searches the incoming data for three consecutive A1 bytes followed by three consecutive A2 bytes. Framing pattern detection is enabled and disabled by the Out-of-Frame (OOF) TTL input of the S3028B and the output of the PMC PM5355. The frame boundary is reported on the Frame Pulse (FP) TTL output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream.

4. The serial-bit data stream is then converted into a byte-serial data format for output onto the TTL Parallel Output Data Bus (POUT[7:0]). The byte-serial data is clocked out of the S3028B and into the PMC PM5355 with the TTL Parallel Output Clock (POCLK) out of the S3028B.

5. The byte-serial data is output from the PMC PM5355 into the S3028B TTL Parallel Data Input Bus (PIN[7:0]) and is sampled by the TTL Parallel Input Clock (PICLK) of the S3028B. This clock is generated by the S3028B TTL Parallel Clock (PCLK) which is fed into the PM5355 as the Transmit Clock (TCLK) and then back into the PICLK input of the S3028B.

6. The byte-serial data is then converted to bit-serial data and output through the PECL transmit serial data (TSDP/N) connections to the Honeywell Fiber Optic Transmitter (F/O Tx).

7. If the incoming serial-bit data stream is lost (when SD is LOW), the Lock Detect circuit internal to the S3027 substitutes the external reference clock for the missing data stream clocking signal. This substitution of reference timing source is helpful to supply a continuous timing signal for the follow-on devices and system operation even though valid, received data does not exist. This switch over is a smooth transition with no noticeable phase shift.

Terminations

The following is a list of terminations that need to be added for this particular design.

1. The 100 Ohm line-to-line termination resistors should be as close to the termination points as possible.
2. The 330 Ohm pull down resistors should be as close to the sources as possible.
3. The high frequency traces should be designed as 50 Ohm transmission lines with the termination as depicted in Figure 2.
4. The 68 Ohm pull up resistors and the 191 Ohm pull down resistors set the DC bias at 3.7 Volts DC.
5. All the termination resistors should be placed at the end of the transmission line and the power supply decoupling should be placed as close as possible to the devices. Refer to the S3028B layout applications note for specific power and ground decoupling and isolation rules.
6. The PECL (differential pairs) traces should have equal length (allows both lines to arrive at the destination at the same time) and be run in parallel and in close proximity of one another. This allows the same noise to couple onto both of the lines and become common mode noise which is ignored by differential inputs.
7. The 33 Ohm series resistors between the PIN[7:0] parallel input data of the AMCC S3028B and the POUT[7:0] of the PMC PM5355 should be as close to the source (PM5355 outputs) as possible.

Conclusion

The AMCC S3028B/S3027 and Honeywell HFM2553-001 solution combine to make a complete STS-12/STM-4 Physical Media Dependent (PMD) layer able for SONET/SDH/ATM data transfer.

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March 27, 1998