FREQUENCY MONITORING APPLICATIONS NOTE S3015

Introduction

The AMCC S3015 was developed to provide the designer with a device offering a flexible and easy way to transmit E4/STM-1/OC-3 ATM data over copper or fiber optic cable. The S3015 transmitter provides the first stage of digital processing of a transmit SONET STS-3 or ITU-T E4 serial bit stream. If jitter or noise saturation exceeding the tolerance of the transmitter is applied to the input (usually at power up) of the Phase Lock Loop (PLL), it may track this noise, and "walk" out of the frequency recapture range, resulting in a failure of the clock recovery circuit when "good" data is initiated or restored.

The simplest way to avoid the S3015 VCO "walkout" when the incoming data signal is lost is to monitor the output recovered clock of the S3015 for the correct frequency with an external PLL frequency monitoring circuit. This can be accomplished using AMCC's latest STM-1/STM-4 CRU Clock Recovery Unit, the S3026, which includes the necessary frequency monitoring logic. This application note explains the implementation of this external frequency monitoring circuit.

Signal Connect Description

Figure 1-1 shows the implementation of this solution.

1. The 155.52 Mbit/s SERCLKOP/N recovered serial clock output of the S3015 is connected to the SERDATIP/N serial data inputs of the S3026.
2. The S3026 LOCKDET output is used as the S3015 Reset (RSTB) input. A PECL to TTL converter is required between the LOCKDET and RSTB to convert the single ended PECL output of the S3026 to the TTL input of RSTB on the S3015.

The S3026 used as an external PLL frequency monitoring circuit can have its digital and analog power and ground's tied together. This application of the S3026 does not need to recover the clock with minimum jitter, therefore there is no need to be concerned about adding all of the decoupling capacitors and inductors on the power and ground connections to the S3026.

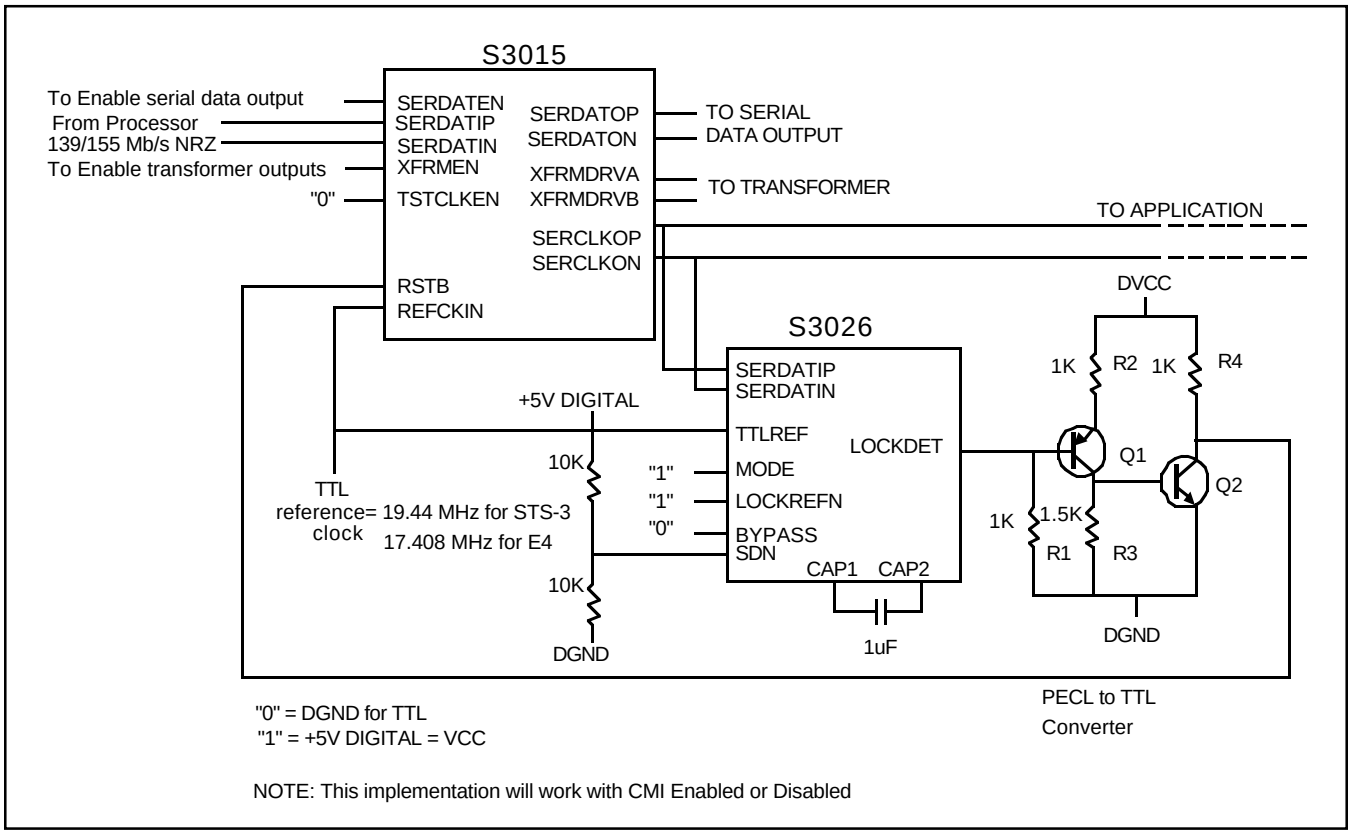
The S3015 and the S3026 should be placed as close together as possible.

Parts list

The following is a parts list that is a recommendation to the designer to implement the circuit in Figure 1.

QTY	Part # or equivalent	Description
3		Resistor, 1K, 10%, 1/8W, 805 or 603 package size
1		Resistor, 1.5K, 10%, 1/8W, 805 or 603 package size
2		Resistor, 10K, 10%, 1/8W, 805 or 603 package size
1		Capacitor, 1uf, 10%, X7R, 50V, Surface Mount package
1	MMBT3904LT1	NPN Transistor, 2N3904
1	MMBT3906LT1	PNP Transistor, 2N3906
1	S3026	SONET/SDH Clock Recovery Unit
1	S3015	E4/STM-1/OC-3 ATM Interface Circuits

Figure 1. S3015/S3026 Block Diagram



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Frequency Monitoring Mode of Operation

To monitor the S3015 recovered clock frequency the S3026 is setup in STM-4 mode (622.08 Mbit/s). This allows the S3026 to lock to a data stream whose bit rate is equal to or less than the clock frequency (622.08 Mbit/s), with a practical lower limit of 1/8 the clock frequency (12.5% edge transition density). In running the S3026 in STM-4 mode the S3015 SERCLKOP/N output clock looks like a 001100110011 data stream with enough edge density when examined with a STM-4 clock (622.08 Mbit/s) to recover the clock and compare it to the local reference clock. Note that the reference clock can be 19.44 MHz for STS-3 applications or 17.408 MHz for E4 applications. If the recovered clock frequency exceeds the specified limits (1000 ppm), the data is assumed to be corrupted and the reference clock is used to control the clock recovery circuit.

Loss of Signal Recovery Mode of Operation

The following is a description by a series of steps of how the circuit in Figure 1 operates.

1. In normal operation with a valid signal on the SERDATIP/N input of the S3015, the S3015 delivers a recovered clock very close to 155.52 Mbit/s on the SERCLKOP/N outputs.
2. If the recovered clock frequency drifts away (VCO drift “walkout”) more than a 1000 ppm (155.52 Kbit/s) from the local reference frequency, the S3026 locks its PLL to the TTLREF local reference and the LOCKDET output goes inactive (low).
3. The LOCKDET PECL output is then converted to interface with the RSTB TTL input of the S3015.
4. When the LOCKDET output goes inactive (low), the RSTB re-initializes the S3015 to a known state. This initializes the internal registers and re-starts the acquisition of the S3015 PLL. The S3015 PLL changes its reference from the serial data stream to the reference clock and synthesizes the SERCLKOP/N output to be 155.52 Mbit/s.
5. When the S3026 VCO comes back within less than 250 ppm from the local reference frequency, the S3026 drives the LOCKDET active high.
6. LOCKDET high changes the RSTB to high which switches the S3015 out of reset mode and tries to lock and recover the clock from the SERDATIP/N input data stream.

PECL to TTL Conversion

This circuit was designed so as to meet the level shifting requirements, the reliability requirements, the temperature requirements, and to implement the conversion with the minimum number of components. The

design task is to convert the PECL voltages and voltage swing of 1 volt to the proper TTL levels. Shown on Figure 1-1 the PECL to TTL conversion process is a two transistor solution. Q1 amplifies the 1V voltage swing out of LOCKDET (single ended PECL) output. When LOCKDET is low (~3.2V), Q2 is turned on and saturated. RSTB is low selecting to reset the S3015. When LOCKDET is high (~4.2V), there is a small voltage drop in R2 (around 100mv), and a voltage drop in R3 (around 150mv) to keep Q2 off. RSTB is pulled high by R4 to choose normal operation of the S3015.

Conclusion

This implementation offers a simple and safe Frequency Monitoring Circuit. This circuit is totally transparent at the system level. Whatever caused the signal interruption at the physical connection (ie. jitter, noise), the S3015 VCO always properly locks to the input data stream.

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